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In-circuit Signal Analysis in the Development of Digital Devices in Vivado 2018

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***Abstract*—Considered the implementation of in-circuit analysis of logical signals in digital devices synthesized in Xilinx Field-Programmable Gate Array. Designed a digital control device streaming analog-to-digital converter. An analysis of the results of the analog-digital conversion was carried out and measures were taken to smooth out the false results of the conversion.**

Keywords—analog-digital converter, Field-Programmable Gate Array, in-circuit debugging, Logic Analyzer, bus, clock signal .

I. INTRODUCTION

Xilinx is one of the world leaders in developing and selling Field-Programmable Gate Array (FPGA). The company produces several FPGA series, such as Spartan, Artix, Kintex. For the design of digital devices based on FPGA is available free software Vivado. Its current latest version is Vivado 2019. The process of developing a digital device consists of a number of mandatory steps: a description of the device in VHDL or Verilog, synthesis and simulation of the device, description of limitations, generation of the firmware file, firmware download and testing of the device. Built-in simulation tools allow you to analyze the work of synthesized timers, signal generators, etc. However, almost any digital device communicates with external sensors, RAM and flash memory, analog-digital and digital-analog converters. Therefore, analysis of the interface and internal digital signals in a working digital device is necessary. The in-circuit debugging capability of a digital device in the Vivado environment is provided by the IP core Integrated Logic Analyzer (ILA). It allows you to make a temporary sample of up to 1024 digital signals (single-bit or multi-bit). The depth of sampling of each of the signals is from 1024 to 131071 counts. Consider the capabilities and configuration of the IP core ILA on the example of high-speed analog-to-digital converter (ADC) control AD9235.

II. ADC AD9235 SPECIFICATIONS AND MANAGEMENT

ADC AD9235 is widely used to digitize: signals of digital radio receivers at intermediate frequency, signals of optical arrays, etc. The ADC has the following characteristics: conversion frequency up to 65MSPS, 12-bit conversion result width, parallel output bus, analog input voltage range up to 0.5 or up to 1V when using an internal voltage source. ADC refers to the conveyor type of converters. For each pulse of the clock signal at the CLK input on the output bus D0 ... D11, a conversion result is generated. The delay in establishing data on the D0 ... D11 bus is less then 6 ns relative to the rising edge of the clock signal. The conveyor delay of the output of the result of analog-to-digital conversion is equal to 7 periods of the clock signal. Figure 1 shows the working principle of the ADC.

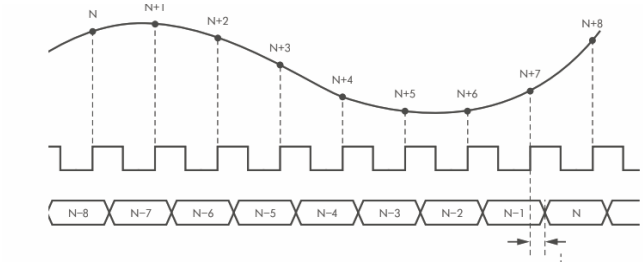

Fig. 1. Working principle of the ADC.

III. INTEGRATED LOGIC ANALYZER

To configure the ILA's IP core in the Vivado environment, use the Wizard, which allows you to configure the interface structure for connecting input and output signals. Customizable parameters include: the number of analyzed signals (probe), probe storage buffer depth, the resolution of using an external trigger, the use of an additional trigger. The ILA core can work in automatic mode and by trigger. Auto mode allows you to capture 1024-131071 samples of input signals on a command from the Vivado environment from the moment you receive the command. Figure 2 shows the ILA kernel settings.

The sampling frequency is determined by the frequency of the clock signal arriving at the clock input. This mode is effective for analyzing periodic signals with a sample time limit. For example, at a clock frequency of 100 MHz, the maximum analysis interval is 1.3 ms. When asynchronous interaction with external devices, the formation of signals of the interface VGA, etc. It is advisable to use the operation mode using the trigger trigger.

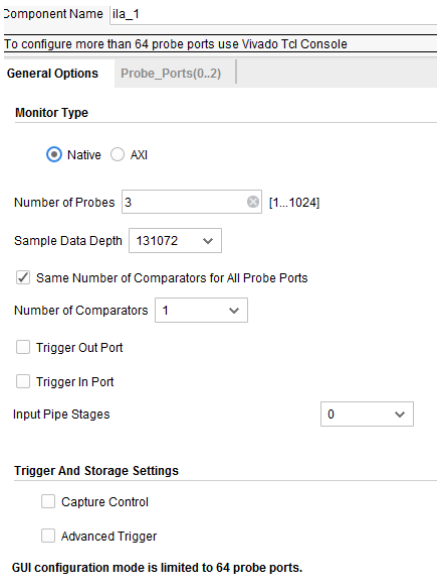

Fig. 2. ILA kernel settings.

After completing the configuration of the ILA core, a component description is generated that is embedded in the main program.

IV. In-circuit debugging of the control unit AD9235

For research work ADC was used Demo Board Nexys 4DDR. Based on the Artix7 FPGA, a 40 MHz clock frequency module was developed in VHDL. The generated clock frequency was applied to the clock input Clk AD9235. Reading the conversion results from the output data bus is performed on the falling edge of the clock signal. The delay between the launch of the ADC and the reading of the conversion result is 12.5 ns, which meets the requirements of the manufacturer of the ADC. For in-circuit debugging of the digital control device AD9235, the ILA core is built into the program. The core is configured to analyze three signals: the clock signal Clk, 12-bit data bus D0 ... D11, the signal over-range (OTD). The depth of sampling is 131071 counts. The ILA component description is shown below.

```
COMPONENT ila_0
PORT (clk : IN STD_LOGIC;
probe0 : IN STD_LOGIC_VECTOR(0 DOWNTO 0);
probe1 : IN STD_LOGIC_VECTOR(0 DOWNTO 0);
probe2 : IN STD_LOGIC_VECTOR(11 DOWNTO 0)
);
```

V. Simulation results

An analog input AD9235 from the signal generator was fed a sinusoidal signal with a frequency of 4 MHz. The amplitude of the signal is 1B. Figure 3 shows waveforms of analog-to-digital conversion results and interface signals of the AD9235.

Analysis of the conversion results shows that some samples may be distorted, as evidenced by setting the output of the OTR logical signal to “1”. The main causes of such distortions can be: interference in the power supply circuits and over-amplification of the input signal. The solution of such problems should be complex - hardware and software. To solve such phenomena, it is necessary to use a hardware power isolation between the digital and analog part of the circuit. The software part of the solution must contain an interpolating filter. The filter should interpolate an unreliable measurement result based on neighboring time samples of the signal being processed. Such a filter for the case of continuous input signal was developed by the authors in the language of VHDL.

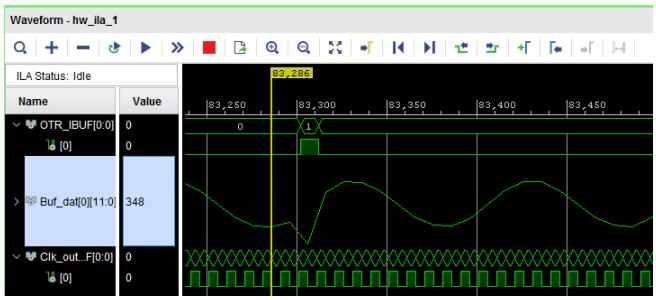

Fig. 3. Waveforms of analog-to-digital conversion results.

The filter module uses a buffer of seven 12-bit analog signal times, as well as a buffer of seven OTR signal samples. The quadratic interpolation method was implemented by software.

After applying the filter to the results of the analog-digital conversion, the probability of distortion decreased from from $3 \cdot 10^{-4}$ to $1.3 \cdot 10^{-8}$.

The residual error is due to cases where the OTR signal does not indicate the occurrence of distortion.

VI. Conclusion

Intracircuit debugging based on the ILA core allows you to identify the features of the digital nodes that the synthesized FPGA interacts with. Such features are almost impossible to model because of the random nature. Through the use of ILA, distortion of the result of converting an analog signal to digital form was detected using the ADC AD9235. The use of an interpolating filter made it possible to significantly reduce the effect of distortion.

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