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CONTENTS

A Black-Box-Oriented Test Methodology A. Benso, A. Bosio, P. Prinetto, A. Savino	11
Design and Optimization of Fault-Tolerant Distributed Real-Time Systems Peng Z., Izosimov V., Eles P., Pop P	16
Interconnect Yield Improvement for Networks on Chip Andre Ivanov	22
The Scaling Semiconductor World and Test Technology Yervant Zorian	22
A Unified HW/SW Interface Model to Remove Discontinuities Between HW and SW Design A. Jerraya	23
Background Cache for Improving Memory Fault Tolerance Michail F. Karavay, Vladimir V. Sinelnikov	24
Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective Daniel Foty	29
Hierarchical Silicon Aware Test and Repair IP: Development and Integration Flow Reducing Time to Market for Systems on Chip Samvel Shoukourian, Yervant Zorian	39
The Pivotal Role of Performance Management in IC Design Eyck Jentzsch	41
TEST METHODS AND TOOLS	
Analysis of a Test Method for Delay Faults in NoC Interconnects Tomas Bengtsson, Artur Jutman, Shashi Kumar, Raimund Ubar, Zebo Peng	42
Unified Framework for Logic Diagnosis A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel	47
Hierarchical Systems Testing based on Boundary Scan Technologies Hahanov V., Yeliseev V., Hahanova A., Melnik D	53
Testing the Hardware Implementation of a Distributed Clock Generation Algorithm for SoCs A. Steininger, T. Handl, G. Fuchs, F. Zangerl	59
Extended Boundary Scan Test Using Hybrid Test Vectors Jan Heiber	65
A March Test for Full Diagnosis of All Simple Static Faults in Random Access Memories G. Harutunyan, Valery A. Vardanian	68
Efficient Implementation of Physical Addressing for Testing and Diagnosis of Embedded SRAMs for Fault Coverage Improvement K. Aleksanyan, Valery A. Vardanian	72
High Level Models Based Functional Testing of Pipelined Processors Victor Belkin, Sergey Sharshunov	76

On Complexity of Checking of Cryptosystems Volodymyr G. Skobelev	82
Distributed Fault Simulation and Genetic Test Generation of Digital Circuits Skobtsov Y.A., El-Khatib A.I., Ivanov D.E	89
Hierarchical Evolutionary Approach to Test Generation Skobtsov V.Y. Skobtsov Y.A.	95
VERIFICATION	
Incremental ABV for TLtoRTL Design Refinement Nicola Bombieri, Franco Fummi, Graziano Pravadelli	100
RTL Compiler Templates Verification: Approach to Automation Lev Danielyan, Sergey Hakobyan	108
Verification of Implementation of Parallel Automata (Symbolic Approach) Andrei Karatkevich	112
SystemCFL: An Infrastructure for a TLM Formal Verification Proposal (with an overview on a tool set for practical formal verification of SystemC descriptions) K.L. Man, Andrea Fedeli, Michele Mercaldi, M.P. Schellekens	116
System Level Methodology for Functional Verification SoC Alexander Adamov, Sergey Zaychenko, Yaroslav Miroshnychenko, Olga Lukashenko	122
Path Sensitization at Functional Verification of HDL-Models Alexandr Shkil, Yevgeniya Syrevitch, Andrey Karasyov, Denis Cheglikov	126
Dynamic Register Transfer Level Queues Model for High-Performance Evaluation of the Linear Temporal Constraints Vladimir Hahanov, Oleg Zaharchenko, Sergiy Zaychenko	132
The Automation of Formal Verification of RTL Compilers Output Pavlush Margarian	140
LOGIC, SYSTEM AND PHYSICAL SYNTHESIS	
Congestion-Driven Analytical Placement Andrey Ayupov, Alexander Marchenko	143
Estimation of Finite State Machine Realization Based on PLD E. Lange, V. Chapenko, K. Boule	149
Encoding of Collections of Fragment of Variables Barkalov A.A., Ahmad Fuad Bader, Babakov R.M.	153
An Algorithm of Circuit Clustering for Logic Synthesis O. Venger, I. Afanasiev, Alexander Marchenko	156
CMOS Standard Cell Area Optimization by Transistors Resizing Vladimir Rozenfeld, Iouri Smirnov, Alexander Zhuravlev	163
Optimization of Address Circuit of Compositional Microprogram Unit Wisniewski R., Alexander A. Barkalov, Larysa A. Titarenko	167

Optimization of Circuit of Control Unit with Code Sharing Alexander Barkalov, Larysa Titarenko, Małgorzata Kołopieńczyk	171
Routing a Multi-Terminal Nets with Multiple Hard Pins by Obstacle-Avoiding Group Steiner Tree Construction J. D. Cho, A. I. Erzin, V. V. Zalyubovsky	175
Optimization for Electro- and Acousto-Optical Interactions in Low-Symmetric Anisotropic Materials Kajdan Mykola, Laba Hanna, Ostrovskij Igor, Demyanyshyn Nataliya, Andrushchak Anatolij, Mytsyk Bohdan	179
Force-Position Control of the Electric Drive of the Manipulator A.V. Zuev, V.F. Filaretov	184
FAULT TOLERANCE	
K-out-of-n and K(m,n) Systems and their Models Romankevych V., Potapova K., Hedayatollah Bakhtari	189
Fault Tolerant Systems with FPGA-based Reconfiguration Devices Vyacheslav S. Kharchenko, Julia M. Prokhorova	190
Fault-Tolerant Infrastructure IP-cores for SoC: Basic Variants and Realizations Ostroumov Sergii, Ushakov A. A., Vyacheslav S. Kharchenko	194
Fault-tolerant PLD-based Systems on Partially Correct Automaton Nataliya Yakymets, Vyacheslav Kharchenko	198
FME(C)A-Technique of Computer Network Reliability and Criticality Analysis Elyasi Komari Iraj, Anatoliy Gorbenko	202
TEST GENERATION AND TESTABILITY	
Scan Based Circuits with Low Power Consumption Ondřej Novák, Zdeněk Pliva	206
Memory Address Generation for Multiple Run March Tests with Different Average Hamming Distance S.V. Yarmolik, V.N. Yarmolik	212
Structural Method of Pseudorandom Fixed Weight Binary Pattern Sequences Generation Romankevych A., Grol V., Fallahi Ali	217
Test Pattern Generation for Bridge Faults Based on Continuous Approach N. Kascheev, F. Podyablonsky	222
Hierarchical Analysis of Testability for SoCs Maryna Kaminska, Vladimir Hahanov, Elvira Kulak, Olesya Guz	226
Embedded Remote Wired or Wireless Communication to Boundary-Scan Architectures Mick Austin, Ilkka Reis, Anthony Sparks	231
Economics Modeling the DFT of Mixed-Signal Circuits Sergey G. Mosin	236
CAD TOOLS AND DEVICES	
Optimal Electronic Circuits and Microsystems Designer A.I. Petrenko	239

Computer Aided Design Support of FSM Multiplicative Decomposition Alexander Sudnitson, Sergei Devadze	241
Complex Process Engineering of Projection of Electronic Devices by Means of Automized System SATURN D.V. Bagayev, A.C. Firuman	247
Hand-Held Mobile Data Collecting Terminal Armen Saatchyan, Oleg Chuvilo, Chaitanya Mehandru	252
Logic and Fault Simulation Based on Multi-Core Processors Volodymyr Obrizan, Valeriy Shipunov, Andiry Gavryushenko, Oleg Kashpur	255
HES-MV – A Method for Hardware Embedded Simulation Vladimir Hahanov, Anastasia Krasovskaya, Maryna Boichuk, Oleksandr Gorobets	257
Hierarchical Approach for Functional Verification of HW/SW System on Chip (SoC) Oleksandr Yegorov, Podkolzin N., Yegor Denisov, Andrey Yazik	264
Output Buffer Reconfiguration in Case of Non Uniform Traffic Vyacheslav Evgrafov	267
DESIGN METHODS AND MODELING	
Time-Sensitive Control-Flow Checking Monitoring for Multitask SoCs Fabian Vargas, Leonardo Picolli, Antonio A. de Alecrim Jr., Marlon Moraes, Márcio Gama	272
Development and Application of FSM-Models in Active-HDL Environment for Network Protocols Testing Anna.V. Babich, Oleksandr Parfentiy, Eugene Kamenuka, Karina Mostovaya	279
How to Emulate Network-on-Chip? Peeter Ellervee, Gert Jervan	282
Multistage Regular Structure of Binary Counter of ones Arbitrary Modulo Saposhnikov V. V., Saposhnikov VL. V., Urganskov D. I.	287
An Enhanced Analogue Current-Mode Structure of WP Control Circuit of Neural Networks Hossein Aghababa, Leyla S.Ghazanfari, Behjat Forouzandeh	291
One-Parameter Dynamic Programming Algorithm for Optimal Wire Selection Under Elmore Delay Model A.I. Erzin, V.V. Zalyubovsky	296
Analytical Model of Clock Skew in Buffered H-Trees Dominik Kasprowicz	301
High-Level Facilities for Modeling Wireless Sensor Networks Anatoliy Doroshenko, Ruslan Shevchenko, Konstantin Zhreb	305
Class E Power Amplifier for Bluetooth Applications Olga Antonova, George Angelov, Valentin Draganov	311
An Automation Method for Gate-Count Characterization of RTL Compilers Arik Ter-Galstyan	313
Algorithmic Method of The Tests Forming for Models Verification of Microcircuits Memory M.K. Almaid, V.A. Andrienko, V.G. Ryabtsev	317

SUM IP Core Generator – Means for Verification of Models–Formulas for Series Summation in RKHS Vladimir Hahanov, Svetlana Chumachenko, Olga Skvortsova, Olga Melnikova	322
Design of Wavelet Filter Bank for JPEG 2000 Standard Hahanova I.V., Hahanov V.I., Fomina E., Bykova V., Sorudeykin K.	327
Design of Effective Digital Filters in FPGA Pavel V. Plotnikov	332
POSTER SESSION	
Applications of Combinatorial Cyclic Codes for Images Scan and Recognition Vladimir Valkovskii, Dmitry Zerbino, Oleg Riznyk	335
Architecture of Internet Access to Distributed Logic Simulation System Ladyzhensky Y.V., Popoff Y.V.	339
Computer System Efficient Diagnostics with the Usage of Real-Time Expert Systems Gennady Krivoulya, Alexey Lipchansky, Olga Korobko	344
DASPUD: a Configurable Measurement Device Nikolay P. Molkov, Maxim A. Sokolov, Alexey L. Umnov, Dmitry V. Ragozin	348
Design Methods of Self-Testing Checker for Arbitrary Number of Code Words of (m,n) Code Yu. B. Burkatovskaya, N.B. Butorina, A. Yu. Matrosova	355
Dynamic Heat and Mass Transfer in Saline Water due to Natural Convection Flow over a Vertical Flat Plate Rebhi A. Damseh	361
Effect of Driving Forces On Cylindrical Viscoelastic Fluid Flow Problems A. F. Khadrawi, Salwa Mrayyan, Sameh Abu-Dalo	366
Evolutional Methods for Reduction of Diagnostic Information D. Speranskiy	371
Evolutionary Algorithms Design: State of the Art and Future Perspectives Yuri R. Tsoy	375
Functional properties of faults on fault-secure FSM design with observing only FSM outputs S. Ostanin	380
Hardware Methods to Increase Efficiency of Algorithms for Distributed Logic Simulation Ladyzhensky Y.V., Teslenko G.A.	385
Information Embedding and Watermarking for Multimedia and Communication Aleksandr V. Shishkin	386
Low Contrast Images Edge Detector I.V. Ruban, K.S. Smelyakov, A.S. Smelyakova, A.I. Tymochko	390
Minimization of Communication Wires in FSM Composition S.V. Zharikova, N.V. Yevtushenko	397
Neuro-Fuzzy Unit for Real-Time Signal Processing Ye. Bodyanskiy, S. Popov	403

On Decomposition of Petri Net by Means of Coloring Wegrzyn Agnieszka	407
Single-Argument Family of Continuous Effectively Computed Wavelet Transforms Oleg E. Plyatsek, Majed Omar Al-Dwairi	414
Synthesis Methods of Finite State Machines Implemented in Package ZUBR Valery Salauyou, Adam Klimowicz, Tomasz Grzes, Teodora Dimitrova-Grekow, Irena Bulatowa	420
Synthesis of Logic Circuits on Basis of Bit Transformations Yuri Plushch, Alexander Chemeris, Svetlana Reznikova	423
System of K-Value Simulation for Research Switching Processes in Digital Devices Dmitrienko V.D., Gladkikh T.V., Leonov S.Yu	428
Test Points Placement Method for Digital Devices Based on Genetic Algorithm Klimov A.V., Speranskiy D.V.	436
The Approach to Automation of Designing Knowledge Base in the Device-Making Industry O.V. Bisikalo	440
The Optimal Nonlinear Filtering of Discrete-Continuous Markovian Processes in Conditions of Aposteriori Uncertainty Victor V. Panteleev	443
The Realization of Modified Artificial Neural Network for Information Processing with the Selection of Essential Connections by the Program Meganeuro E.A. Engel	450
Web-system Interface Prototype Designing Globa L.S., Chekmez A. V., Kot T. N.	453
A Bio-Inspired Method for Embedded System Scheduling Problems Abbas Haddadi, Saeed Safari, Behjat Forouzandeh	456
Iterative Array Multiplier with On-Line Repair of Its Functions Drozd A., Lobachev M., Reza Kolahi, Drozd J.	461
Mathematical Modeling and Investigation of a Main SDH-Network Structural Reliability M.M. Klymash, I.M. Dronyuk, R.A. Burachok	464
Experimental Investigation of Two Phase Flow Pressure Drop and Contraction on Tee Junction Shannak Benbella, Al-Qudah Kalid, Al-Salaymeh Ahmed, Hammad Mahmoud, Alhusein Mahmoud	467
Application of Adaptive and New Planning Methods to Solve Computer-Aided Manufacturing Problems Nevludov I.Sh., Litvinova E.I., Evseev V.V., Ponomarjova A.V.	472
Petri Net Decomposition Algorithm based on Finding Deadlocks and Traps Agnieszka Wegrzyn, Marek Wegrzyn	477
Testing for Realistic Spot Defects in CMOS Technology: a Unified View Michel Renovell	482
AUTHORS INDEX	483

HES-MV – A Method for Hardware Embedded Simulation

Vladimir Hahanov, Anastasia Krasovskaya, Maryna Boichuk, Oleksandr Gorobets
Kharkiv National University of Radio Electronics, 14 Lenin Ave., 61166, Ukraine
E-mail: hahanov@kture.kharkov.ua

Abstract

Hardware implementation of triadic fault-free simulation method HES-MV – Hardware Embedded Simulation based on Multi-Valued alphabet is proposed. This method uses hardware gate and RTL models for large scale digital designs description. Structure solutions for logic elements models implementation are presented. Logic element has two bits for four values encoding for each input or output line of simulated device.

1. Introduction

Necessity for considerable increase of simulation performance for testing and verification purposes is well-known, it is defined by increasing complexity of digital system-on-chips with millions of gates. Existing simulation tools of leading companies: Cadence, Mentor Graphics, Synopsys, Aldec, spend several hours to analyze design with several millions of gates (PC with 500MHz microprocessor and 512MB RAM). Such costs are very important for end users. Aldec Inc. (www.aldec.com) proposes one of the possible solution: during system verification, separate design model on two parts (hardware H and software S): $M = \{H, S\}$, $H \gg S$. Moreover software model – a new one, unverified source code. Hardware part is tested IP –cores, implemented into HES (Hardware Embedded Simulator), based on Xilinx's FPGA, connected to the simulation kernel through PCI interface. Thus, Aldec proposed new design flow for world market, it gives possibility to reduce verification time in ten times. But hardware-based simulation excludes possibility for multi-valued simulation mode and transition analysis, hazard simulation, races analysis as well. Proposed approach, along with preserving hardware simulation advantages in performance, allows to simulate signal races and to solve set-up problem by extending hardware model with two-bit signals to identify four states of logic variable. Proposed bus-based primitive

and logic elements hardware models may be important on world market of electronic design automation tools for design and test of large scale digital devices.

Object of inquiry – digital circuit, implemented into ASIC of PLD, specified using VHDL language.

Goal of the research – considerable decrease digital device design time (which will be implemented into integrated circuit, containing millions of gates) and extend functional capabilities of fault-free simulation system by multi-valued models hardware implementation, high-performance simulation method for set-up problem solving, race analysis and timing verification of tests under synthesis.

Research problems: 1. Digital circuit models classification. 2. Multi-valued analysis model for hazard detection and set-up problem solving. 3. Creation of software/hardware tools structure to multi-valued fault-free simulation. 4. Software/hardware implementation of multi-valued fault-free simulation method. 5. Testing and verification of hardware/software HES-MV tool.

2. Digital circuit models classification

Several papers laid in the base of current research, which are related to digital devices simulation speed-up based on hardware acceleration [1,2], multi-valued model and circuits for races analysis [3-15], mathematic methods for simulation speed-up [16,17] and synchronous event-based simulation algorithms for digital systems [5-8,18-19]. At fig.1 it is represented improved model classification for fault-free simulation and race analysis.

On the macro-level, we introduce seven qualification characteristics <Form, Structuring, Time, Iterativity, Alphabet, Implementation, Hierarchy>

$M = \langle F = \{F^a, F^g, F^t\}, S = \{S^s, S^f\}, T = \{T^s, T^a\}, I = \{I^a, I^i\}, A = \{A^b, A^m\}, P = \{P^h, P^s\}, H = \{H^g, H^r, H^s\} \rangle$

Each characteristic includes several components (see fig.1).

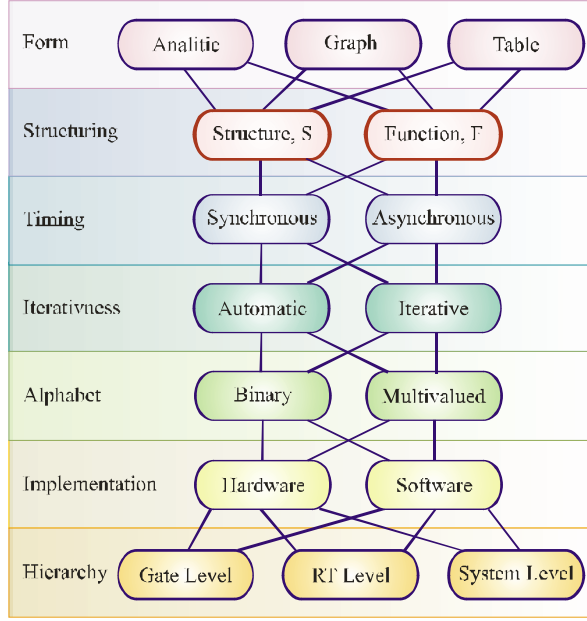


Figure 1. Digital system models

Main components are: *Structuring* specifies degree of details, which can be defined using the rest six classifiers. E.g. seven chosen components $M = \langle F^a, S^s, T^s, I^i, A^m, P^h, H^g \rangle$ defines analytic, structural, synchronous, iterative, multi-valued, hardware, gate-level model. In general, each specific seven of characteristics defines possible ways to synthesize, analyze and model adequacy, defines maximum computational complexity, precision and variety of forward and backward simulation. This implies urgency of proposed classification for electronic design automation tools developers. Totally, from presented classification (see fig.1), it exists minimum $|M| = |F| \times |S| \times |T| \times |I| \times |A| \times |P| \times |H| = 3 \times 2 \times 2 \times 2 \times 2 \times 2 \times 3 = 288$ different model implementations! But reality is more multiform, because some existing models are composed in form of vector of own characteristics subset, e.g.:

$$M = \langle F = \{F^a, F^t\}, S = \{S^s, S^f\}, T = \{T^s\},$$

$$I = \{I^a\}, A = \{A^m\}, P = \{P^h, P^s\}, H = \{H^r\} \rangle.$$

Boundary assessment of number of all possible models is defined as product of Booleans of each characteristic:

$$\begin{aligned} |M| &= (2^{|F|} - 1) \times (2^{|S|} - 1) \times (2^{|T|} - 1) \times (2^{|I|} - 1) \times \\ &\times (2^{|A|} - 1) \times (2^{|P|} - 1) \times (2^{|H|} - 1) = \\ &= 7 \times 3 \times 3 \times 3 \times 3 \times 3 \times 7 = 11907. \end{aligned}$$

Choosing of concept (subset of parameters of each characteristics) for digital system model creation depends on solving tasks. In case of hardware-based

fault-free simulation on gate level, it is necessary to consider model of minimal complexity and sufficient adequacy, which is defined as: analytical, structural, synchronous, iterative, multi-valued, hardware, gate-level:

$$M = \langle F^a, S^s, T^s, I^i, A^m, P^h, H^g \rangle. \quad (1)$$

This concept, being sufficient, will not be maximum exact, because it has no exact timing delay characteristics, which are peculiar to asynchronous models. Concept of asynchronism increases computational costs for device analysis in ten times.

3. Race analysis models

One may analyze design on the subject of race conditions using methods of synchronous and asynchronous digital systems simulation. Differences of these methods consist in used scale of quantification of time continuum and time delays within components. Specialized model of primitive of device, shown in fig. 2: $\mu = \langle \varphi, \tau, \lambda, \alpha \rangle$, considers synchronous-asynchronous nature of races and applies both to digital system and to separate components. Four parameters may be refined as follows:

$$\begin{aligned} \mu &= \langle \varphi = [t_i, t_{i+1}]; \tau = [\tau_{\min}, \tau_{\max}]; \\ \lambda &= [\lambda_{\min}, \lambda_{\max}], \alpha = \{0, 1, X, \emptyset\} \rangle. \end{aligned} \quad (2)$$

Here we got two types of delays, related to nominal parameters of elements, and dispersion of primary input stimuli applying. Parameter φ defines period of synchronization – timing interval between two consecutive input test or work stimuli, this parameter must be no less than delay of whole circuit's delay. Parameter τ defines nominal element's or circuit's delay dispersion, which identifies procedure of primitive's simulation during asynchronous simulation. Parameter λ defines primary input switch time dispersion, its value identifies algorithms of synchronous, asynchronous and delta-triadic simulation. Parameter α defines signal's alphabet for transition process analysis, at the same time, alphabet must contain three or more symbols.

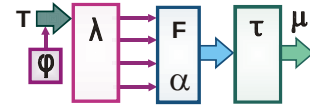


Figure 2. Timing model of element (device)

To simplify asynchronous circuit analysis, model time scale Δt is selected as greatest common divisor of nominal delays τ_i , due to this, all model delays r_i are

integer values. Model delays may be calculated using equation $r_i = \tau_i / \Delta t$. At the same time, all changes on the signals are happened only in time moments divisible by Δt : $0, \Delta t, 2\Delta t, \dots$ of simulated time. Signal's value on the output $Y_i = g_i(t - \tau_i)$ of element g_i in time t is defined by inputs' states in time $t - r_i$.

In the following, we will discuss several the most popular race analysis methods, based on variations of parameters of μ .

1. Synchronous races analysis:

$$\begin{aligned} t_{i+1} - t_i &= \text{const}; \quad \alpha = \{0, 1, X\}; \\ \tau_{\min} = \tau_{\max} &= 0; \quad \lambda_{\min} = \lambda_{\max} = \text{const}. \end{aligned} \quad (3)$$

It is described as: fixed and in advance defined interval between switching consecutive input stimuli, defined as $\Delta t = t_{i+1} - t_i$; necessity of keeping of correlation for circuit's delay τ and element τ_i : $\Delta t \gg \tau \gg \tau_i$; fixed value of nominal elements' delay $\lambda_{\min} = \lambda_{\max} = \text{const}$, and used three-valued alphabet $\alpha = \{0, 1, X\}$, where X – state of line, not identified neither as zero, nor as one, which oriented to exposure race conditions.

Synchronous analysis supposes, that time of race existence is considerably greater than circuit's nominal delay. The disadvantage of this method is false race condition identification. Synchronous simulation in $\{0, 1\}$ alphabet can't determine race.

2. Asynchronous race analysis:

$$\begin{aligned} t_{i+1} - t_i &\neq \text{const}; \quad \alpha = \{0, 1\}; \\ \tau_{\min} = \tau_{\max} &\neq 0; \quad \lambda_{\min} = \lambda_{\max} = 0 \end{aligned} \quad (4)$$

It is described as: not fixed interval between switching consecutive input stimuli; nominal (or model) delays of components are not equal to zero; absence of input's switching time dispersion; usually binary simulation alphabet. It is necessary to know exact components' delays for method's implementation, but this is unavailable sometimes.

3. Δ – triadic race analysis:

$$\begin{aligned} t_{i+1} - t_i &= \text{const}; \quad \tau_{\min} = \tau_{\max} \neq 0; \\ \lambda_{\min} = \lambda_{\max} &= q; \quad \alpha = \{0, 1, X, \emptyset\}. \end{aligned} \quad (5)$$

In comparison with asynchronous analysis, the parameters of Δ – triadic model are characterized by not fixed interval between switching of test sequences and input signals. The method eliminates disadvantages of binary asynchronous and triadic synchronous simulation. At the same time, in addition to nominal delay $\tau_i = r_i \Delta t$ of each primitive, input signal switching dispersion $q \Delta t$ is added, where q – natural

number. We obtain triadic synchronous simulation method, given $q \gg \tau$, where τ – maximum delay of the segment. We can increase or decrease adequacy of analysis by varying parameter q , at the same time by respective decreasing or increasing of processing time. But choosing parameter q – is a quite complex problem of expert analysis, related to consideration of wires length (board–chip).

4. Races analysis with growing ambiguity:

$$\begin{aligned} t_{i+1} - t_i &= \text{const}; \quad \tau_{\min} \neq \tau_{\max}; \\ \lambda_{\min} = \lambda_{\max} &= 0; \quad \alpha = \{0, 1, X, \emptyset\}. \end{aligned} \quad (6)$$

Method guarantees exact race identification, because of using nominal delays interval. Output value $Y_i = g_i(t - r_{\max}, t - r_{\min})$ in time t is defined by states of corresponding inputs in interval $[t - r_{\max}, t - r_{\min}]$. And vice versa, ambiguity exists in interval $[t + r_{\min}, t + r_{\max}]$ when input signal changes its value in time t . Simulation with growing ambiguity removes primitive's simulation delay determinism by including it into interval.

5. Δ – triadic race analysis with growing ambiguity combines advantages of the both methods. Active parameters:

$$\begin{aligned} t_{i+1} - t_i &= \text{const}; \quad \tau_{\min} \neq \tau_{\max}; \\ \lambda_{\min} &\neq \lambda_{\max}; \quad \alpha = \{0, 1, X, \emptyset\}. \end{aligned} \quad (7)$$

Method gives possibility to obtain previous methods by changing inputs' switch dispersion

$q = \{\Delta t, 2\Delta t, \dots\} \in [r_{\min} = \frac{\lambda_{\min}}{\Delta t}, r_{\max} = \frac{\lambda_{\max}}{\Delta t}]$ and interval of ambiguous nominal delays:

$$0 \leq \frac{\tau_{\min}}{\Delta t} \leq \frac{\tau_i}{\Delta t} \leq \frac{\tau_{\max}}{\Delta t}. \text{ But universality of such}$$

approach is related to complexity of its implementation and low performance. Because of this, weighty arguments must be provided to implement such model.

Presented general model of digital system (2), (7) is oriented to solving almost all tasks of timing verification on the all design stages. But software implementation of simulation algorithm based on (7) is related to considerable time consumptions, which can be a lot of hours. For example, XILINX library, based on VITAL standard [20], allows verifying digital designs after synthesis into ASIC (FPGA, CPLD) in interval from 3 to 8 hours, with chips complexity in 1 000 000 gates. One of the possible solutions to reduce simulation runtime is hardware implementation of models and methods of transition processes analysis and race conditions detection.

4. Hardware approach to race analysis

The main idea of hardware model for multi-valued transition process analysis is development of base elements or primitives, where input and output lines are represented as two-bits busses, able to code four logic states $\alpha = \{0, 1, X, \emptyset\}$, which are necessary to identify transition states, different of 0 and 1. Symbol X is able to identify race conditions, hazards [5-9], which lead to unpredicted or unspecified state of digital system. Moreover, symbol X includes all transition processes of more complex alphabets [6, 10], which oriented to combinational circuits simulation. But extension of alphabet gives almost no advantages for sequential circuits' analysis [5], which are taking the most part of modern designs. Thus, it is enough to use triadic logic for solving following tasks:

1. Identifying hazards and race condition on the circuit's lines.

2. Verification of test sequences for the purpose of set-up into determined binary or defined state from undefined triadic one.

Further we consider primitives' models and their hardware implementation into FPGA (CPLD).

FPGA is oriented to truth table implementation, containing 4, 8, 9, 10, 11, 12 inputs. Correspondingly, truth table may contain from $2^4 = 16$ up to $2^{12} = 4096$ one-bit lines. Thus, LUT of FPGA, containing 16 bit and four address inputs, can implement basic logic elements (AND, OR, NOT) using four-valued logic:

And =	$\wedge$	0	1	X	$\emptyset$	$\approx$	$\wedge$	01	10	11	00
	0	0	0	0	$\emptyset$		01	01	01	01	00
	1	0	1	X	$\emptyset$		10	01	10	10	00
	X	0	X	X	$\emptyset$		11	01	10	11	00
	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$		00	00	00	00	00
Or =	$\vee$	0	1	X	$\emptyset$	$\approx$	$\vee$	01	10	11	00
	0	0	1	X	$\emptyset$		01	01	10	11	00
	1	1	1	1	$\emptyset$		10	10	10	10	00
	X	X	1	X	$\emptyset$		11	11	10	11	00
	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$		00	00	00	00	00
Not =	$\overline{X_i}$	0	1	X	$\emptyset$	$\approx$	$\overline{X_i}$	01	10	11	00
	$\overline{\overline{X_i}}$	0	1	X	$\emptyset$		$\overline{\overline{X_i}}$	10	01	11	00

Generalized truth table for two-input primitives, where each input and output is represented by two-bit bus to encode four states, is as the following:

X_1	X_2	$X_1 \wedge X_2$	$X_1 \vee X_2$
00	00	00	00
00	01	00	00
00	10	00	00
00	11	00	00
01	00	00	00
01	01	01	01
01	10	01	10
01	11	01	11
10	00	00	00
10	01	01	10
10	10	10	10
10	11	11	10
11	00	00	00
11	01	01	11
11	10	11	10
11	11	11	11

According to VHDL description (AND, OR four-valued logic functions) [21], represented as listing 1, at fig. 3 post-synthesis implementation of two-input AND element is shown. It consists of 4 inputs, 2 outputs, 6 buffer elements and 2 functional logic blocks.

Listing 1. VHDL description of AND, OR triadic models.

```
-- Defines multi-value logic types and related functions
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.STD_LOGIC_misc.all;
package delta_type is
    type bit2 is array(1 downto 0) of std_logic;
    function "and"( l, r : bit2) RETURN bit2;
    function "not"( l: bit2) RETURN bit2;
    function "or" ( l, r : bit2) RETURN bit2;
    function "xor" ( l, r : bit2) RETURN bit2;
end delta_type;
package body delta_type is
    function "and"( l, r : bit2) RETURN bit2 is
        variable a1, a2, c:std_logic_vector(1 downto 0);
        variable res: bit2;
        begin
            a1(1):=l(1); a1(0):=l(0);
            a2(1):=r(1); a2(0):=r(0);
            c(1):= (a2(1)and a1(1)) or (not a2(0)and a1(1)and not a1(0))
            or (a2(1)and not a2(0)and not a1(0));
            c(0) := (not a2(1)and a2(0)) or (not a1(1)and a1(0)) or
            (a2(0)and a1(0));
            res(1):=c(1); res(0):=c(0);
            return res;
        end function;
    function "not"( l: bit2) RETURN bit2 is
        variable a1, c:std_logic_vector(1 downto 0);
        variable res: bit2;
        begin
            a1(1):=l(1); a1(0):=l(0);
```

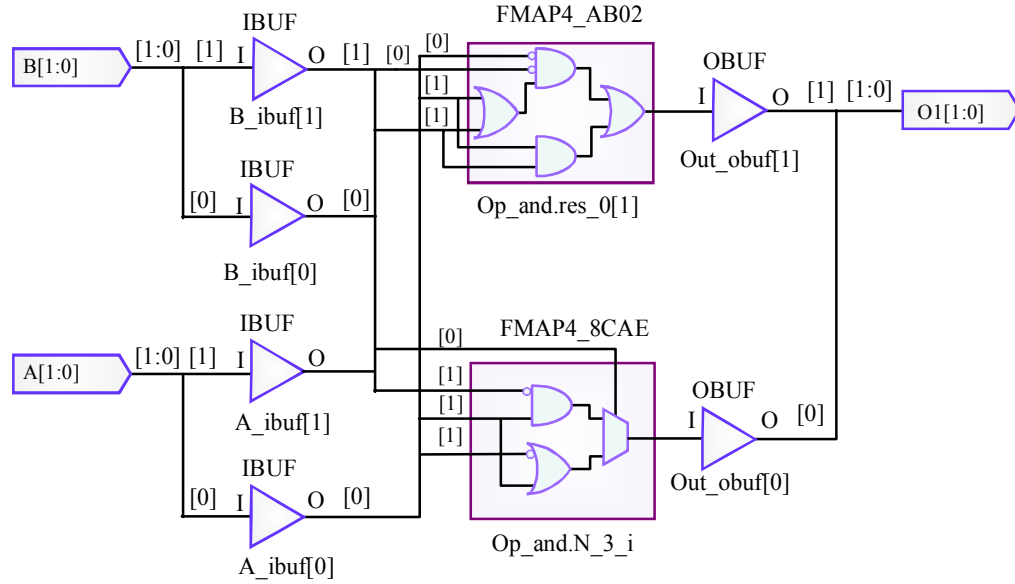


Figure 3. 2AND triadic hardware model

```

c(1):= a1(1);
c(0) := a1(1)xor a1(0);
res(1):=c(1); res(0):=c(0);
return res;
end function;
function "or"( l, r : bit2) RETURN bit2 is
variable a1, a2, c: std_logic_vector(1 downto 0);
variable res: bit2;
begin
a1(1):=l(1); a1(0):=l(0);
a2(1):=r(1); a2(0):=r(0);
c(1):= (a1(1)and a1(0)) or (a2(1)and a2(0)) or (a2(1) and
a1(1));
c(0) := (a2(1) and a2(0)) or (a1(0) and a1(1)) or (not a1(1) and
a1(0)) or (not a2(1) and a2(0));
res(1):=c(1); res(0):=c(0);
return res;
end function;
end delta_type;

```

Implementation of C17 circuit based on multi-valued functional elements is shown in listing 2.

Listing 2. VHDL description of C17 model
use work. delta type.all;

```

library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity c17 is
port (gat1, gat2, gat3, gat6, gat7: in bit2;
gat22, gat23: out bit2);
end c17;
architecture c17 of c17 is
signal gat10, gat11, gat16, gat19: bit2;
begin
gat10 <= not (gat1 and gat3);
gat11 <= not (gat3 and gat6);
gat16 <= not (gat2 and gat11);
gat19 <= not (gat11 and gat7);
gat22 <= not (gat10 and gat16);

```

```

gat23 <= not (gat16 and gat19);
end c17;

```

Post-synthesis implementation based on Xilinx Virtex2p has 24 LUT and 14 buffer elements. At the same time, primary input/output costs are in two times greater than in base variant ($14/7=2$); number of logic elements in use are in five times greater ($46/8=5,75$); Quine estimation shows hardware complexity: $115/14=8,2$. One test vector's simulation time for software model is 8 microseconds. For hardware quaternary model this characteristics is 6,236 nanoseconds. Thus, hardware model's performance gain is $\eta = 8 \times 10^{-6} / 6,236 \times 10^{-9} = 1283$ times greater than its software equivalent. This fact allows concluding, that using of multi-valued hardware models for verification of designed digital devices for the purpose of hazards and race conditions identification, is appropriate.

Verification and testing of multi-valued models was performed on tens digital designs. Testing results are shown in tables 1 and 2. First one illustrates hardware complexity of traditional binary logic and quaternary models for transition processes analysis. Estimation of hardware costs increase is no greater than 10 times. Second table shows comparative performance analysis of binary software and multi-valued hardware models during one test vector simulation. Performance gain is greater than three orders of magnitude. Simulation results were obtained using Sigetest simulation and test generation system [22] and Synplicity Synplify Pro 8.1 [23], Intel Pentium workstation, 2.4GHz CPU with 512 MB RAM. Comparative characteristics for basic circuit's parameters are shown in fig. 4 and 5.

Table 1.

Circuits ISCAS'85	Lines number	Inputs number	Binary project	Multiple project	Hardware overhead
c17	11	5	2	22	11
c432	398	36	74	640	8,6
c499	599	41	120	1028	8,56
c1355	1015	41	157	1129	7,19
c1908	1307	33	121	1194	9,86
c3540	2007	50	380	3095	8,14
c6288	4579	32	637	5422	8,5
c20000	19998	72	2045	16973	8,3
c30000	29995	40	3099	28510	9,2
c50000	49996	22	5121	45064	8,8

Table 2.

Circuits ISCAS'85	Lines number	Inputs number	SW time, mks x 1000	HW time, mks x 1000	Simulation overhead
c17	11	5	0,008	0,0000062	1290
c432	398	36	0,15	0,0000707	2121
c499	599	41	0,2	0,0000672	2976
c1355	1015	41	0,86	0,0000693	12409
c1908	1307	33	6,12	0,0000532	115037
c3540	2007	50	9,28	0,0000710	86197
c6288	4579	32	9,01	0,0001687	53408
C20000	19998	72	1,67	0,0002034	8210
C30000	29995	40	4,17	0,0003681	11328
C50000	49996	22	17	0,0005722	29709

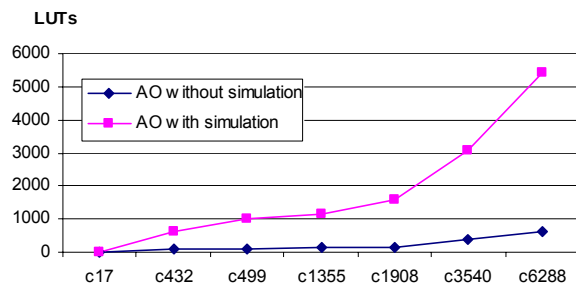


Figure 4. Models' hardware complexity

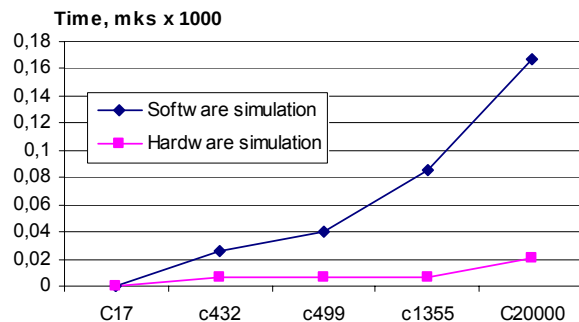


Figure 5. Models' simulation time

5. Conclusions

Scientific novelty of completed research consists in proposal of hardware model for digital devices and

primitives, which allows extending functionality of hardware simulation method for transition processes' analysis and solving set-up task during test synthesis.

Practical value is defined by considerable (in 2-3 orders of magnitude) increase of simulation performance and extension of functional capabilities, which gives reasons to implement obtained results into design tools of leading world companies.

Disadvantage of hardware simulation method is 8-10-fold increase of hardware complexity of digital device model, which gives research topic on the decreasing and minimization of multi-valued models' complexity by using cubic coverage of logic and functional primitives [6]. To process minimized truth tables (cubic coverage), it is necessary to add circuit for triadic coverage analysis based on procedure of intersection's union.

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AUTHORS INDEX

- Adamov Alexander 122
Afanasyev I. 156
Aghababa Hossein 291
Ahmad Fuad Bader 153
Aleksanyan K. 72
Alhusein Mahmoud 467
Almaid M.K. 317
Al-Qudah Kalid 467
Al-Salaymeh Ahmed 467
Andrienko V.A. 317
Andrushchak Anatolij 179
Angelov George 311
Antonio A. de Alecrim Jr. 272
Antonova Olga 311
Austin Mick 231
Ayupov Andrey 143
- Babakov R.M. 153
Babich Anna 278
Bagayev D.V. 247
Barkalov A.A. 153, 167, 171
Belkin Victor 76
Bengtsson Tomas 42
Benso A. 11
Bisikalo O.V. 440
Bodyanskiy Ye. 403
Boichuk Maryna 257
Bombieri Nicola 100
Bosio A. 11
Boule K. 149
Bulatowa Irena 420
Burachok R.A. 464
Burkatovskaya Yu. B. 355
Butorina N.B. 355
Bykova V. 327
- Chaitanya Mehandru 252
Chapenko V. 149
Cheglikov Denis 126
Chekmez A.V. 453
Chemeris Alexander 423
Cho J.D. 175
Chumachenko S. 322
Chuvilo Oleg 252
- Danielyan Lev 108
Demyanyshyn N. 179
Denisov Yegor 264
Devadze Sergei 241
Dimitrova-Grekow Teodora 420
Dmitrienko V.D. 428
Doroshenko Anatolij 305
Draganov Valentin 311
Dronyuk I.M. 464
Drozd A. 461
Drozd J. 461
Eles P. 16
- El-Khatib A.I. 89
Ellervee Peeter 282
Elyasi Komari Iraj 202
Engel E.A. 450
Erzin A.I. 175, 296
Evgrafov Vyacheslav 267
Evseev V.V. 472
Eyck Jentzsch 41
- Fallahi Ali 217
Fedeli Andrea 116
Filaretov V.F. 184
Firuman A.C. 247
Fomina E. 327
Forouzandeh Behjat 291, 456
Foty Daniel 29
Fuchs G. 59
Fummi Franco 100
- Gama Márcio 272
Gavryushenko Andiry 255
Ghazanfari Leyla S. 291
Girard P. 47
Gladkikh T.V. 428
Globa L.S. 453
Gorbenko Anatolij 202
Gorobets O. 257
Grol V. 217
Grzes Tomasz 420
Guz Olesya 226
- Haddadi Abbas 456
Hahanov Vladimir 53, 132, 226, 257, 322, 327
Hahanova A. 53
Hahanova I.V. 327
Hakobyan Sergey 108
Hammad Mahmoud 467
Handl T. 59
Hanna Laba 179
Harutunyan G. 68
Hedayatollah Bakhtari 189
Heiber Jan 59
- Ivanov Andre 22
Ivanov D.E. 89
Izosimov V. 16
- Jerraya Ahmed 23
Jervan Gert 282
Jutman Artur 42
- Kajdan Mykola 179
Kamenuka Eugene 278
Kaminska Maryna 226
Karasyov Andrey 126
Karatkevich Andrei 112
Karavay Michail F. 24
Kascheev N. 222
Kashpur Oleg 255
Kasprowicz Dominik 301
Khadrawi A. F. 366
Kharchenko V. 190, 194, 198
Klimov A.V. 436
Klimowicz Adam 420
Klymash M.M. 464
Kolopieńczyk Małgorzata 171
Korobko Olga 344
Kot T.N. 453
Krasovskaya A. 257
Krivoulya Gennady 344
Kulak Elvira 226
Kumar Shashi 42
- Ladyzhensky Y.V. 339, 385
Landraut C. 47
Lange E. 149
Leonov S.Yu. 428
Lipchansky Alexey 344
Litvinova E.I. 472
Lobachev M. 461
Lukashenko Olga 122
- Majed Omar Al-Dwairi 414
Man K.L. 116
Marchenko A. 143, 156
Margarian Pavlush 140
Matrosova A.Yu. 355
Melnik D. 53
Melnikova Olga 322
Mercaldi Michele 116
Molkov Nikolay P. 348
Moraes Marlon 272
Mosin Sergey 236
Mostovaya Karina 278
Miroshnychenko Yaroslav 122
Mytsyk Bohdan 179
- Novák Ondřej 206
Nevludov I.Sh. 472
- Obrizan Volodymyr 255
Ostanin S. 380
Ostroumov Sergii 194
Ostrovskij Igor 179
- Panteleev Victor V. 443
Paolo Prinetto 11
Parfentiy Oleksandr 278
Peng Zebo 16, 42
Petrenko A.I. 239
Picolli Leonardo 272
Plotnikov Pavel V. 332
Plushch Yuri 423
Plyatsek Oleg E. 414
Podkolzin N. 264
Podyablonsky F. 222
Ponomarjova A.V. 472
Pop P. 16
Popoff Y.V. 339
Popov S. 403
Potapova K. 189
Pravadelli Graziano 100
Pravossoudovitch S. 47
Prokhorova Julia 190
- Ragozin Dmitry V. 348
Rebhi A. Damseh 361
Reis Ilkka 231
Renovell Michel 482
Reza Kolahi 461
Reznikova Svetlana 423
Riznyk Oleg 335
Romankevych A. 217
Romankevych V. 189
Rousset A. 47
Rozenfeld Vladimir 163
Ruban I.V. 390
Ryabtsev V.G. 317
- Saatchyan Armen 252
Safari Saeed 456
Salauyou Valery 420
Salwa Mrayyan 366
Sameh Abu-Dalo 366
- Saposhnikov V.V. 287
Saposhnikov VL.V. 287
Samvel Shoukourian 39
Savino A. 11
Schellekens M.P. 116
Shannak Benbella 467
Sharshunov Sergey 76
Shevchenko Ruslan 305
Shipunov Valeriy 255
Shishkin Aleksandr V. 386
Shkil Alexandr 126
Sinelnikov V. 24
Skobelev Volodymyr 82
Skobtsov V.Y. 95
Skobtsov Y.A. 89, 95
Skvortsova Olga
Smelyakov K.S. 390
Smelyakova A.S. 390
Smirnov Iouri 163
Sokolov Maxim A. 348
Sorudeyin Kirill 327
Sparks Anthony 231
Speranskiy D. 371, 436
Steininger A. 59
Sudnitson Alexander 241
Syrevitch Yevgeniya 126
- Ter-Galstyan Arik 313
Teslenko G.A. 385
Titarenko Larysa, 167, 171
Tsoy Yuri R. 375
Tymochko A.I. 390
- Ubar Raimund 42
Umnov Alexey L. 348
Urganskov D.I. 287
Ushakov A.A. 194
- Valkovskii Vladimir 335
Vardanian Valery 68, 72
Vargas Fabian 272
Venger O. 156
Virazel A. 47
- Wegrzyn A. 407, 477
Wegrzyn M. 477
Wisniewski R. 167
- Yakymets Nataliya 198
Yeliseev V. 53
Yarmolik S.V. 212
Yarmolik V.N. 212
Yazik Andrey 264
Yegorov O Aleksandr 264
Yeliseev V. 53
Yevtushenko N.V. 397
- Zaharchenko Oleg 132
Zalyubovsky V.V. 175, 296
Zangerl F. 59
Zaychenko S. 122, 132
Zdeněk Pliva 206
Zerbino Dmitry 335
Zharikova S.V. 397
Zhereb Konstantin 305
Zhuravlev Alexander 163
Zorian Yervant 22, 39
Zuev A.V. 184