

MINISTRY OF EDUCATION AND SCIENCE OF UKRAINE  
KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

ISBN 966-659-113-8

# **Proceedings of IEEE East-West Design & Test Workshop (EWDTW'06)**

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**Sochi, Russia, September 15 – 19, 2006**

## CONTENTS

A Black-Box-Oriented Test Methodology <b>A. Benso, A. Bosio, P. Prinetto, A. Savino</b> .....	11
Design and Optimization of Fault-Tolerant Distributed Real-Time Systems <b>Peng Z., Izosimov V., Eles P., Pop P</b> .....	16
Interconnect Yield Improvement for Networks on Chip <b>Andre Ivanov</b> .....	22
The Scaling Semiconductor World and Test Technology <b>Yervant Zorian</b> .....	22
A Unified HW/SW Interface Model to Remove Discontinuities Between HW and SW Design <b>A. Jerraya</b> .....	23
Background Cache for Improving Memory Fault Tolerance <b>Michail F. Karavay, Vladimir V. Sinelnikov</b> .....	24
Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective <b>Daniel Foty</b> .....	29
Hierarchical Silicon Aware Test and Repair IP: Development and Integration Flow Reducing Time to Market for Systems on Chip <b>Samvel Shoukourian, Yervant Zorian</b> .....	39
The Pivotal Role of Performance Management in IC Design <b>Eyck Jentzsch</b> .....	41
<b>TEST METHODS AND TOOLS</b>	
Analysis of a Test Method for Delay Faults in NoC Interconnects <b>Tomas Bengtsson, Artur Jutman, Shashi Kumar, Raimund Ubar, Zebo Peng</b> .....	42
Unified Framework for Logic Diagnosis <b>A. Rousset, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel</b> .....	47
Hierarchical Systems Testing based on Boundary Scan Technologies <b>Hahanov V., Yeliseev V., Hahanova A., Melnik D</b> .....	53
Testing the Hardware Implementation of a Distributed Clock Generation Algorithm for SoCs <b>A. Steininger, T. Handl, G. Fuchs, F. Zangerl</b> .....	59
Extended Boundary Scan Test Using Hybrid Test Vectors <b>Jan Heiber</b> .....	65
A March Test for Full Diagnosis of All Simple Static Faults in Random Access Memories <b>G. Harutunyan, Valery A. Vardanian</b> .....	68
Efficient Implementation of Physical Addressing for Testing and Diagnosis of Embedded SRAMs for Fault Coverage Improvement <b>K. Aleksanyan, Valery A. Vardanian</b> .....	72
High Level Models Based Functional Testing of Pipelined Processors <b>Victor Belkin, Sergey Sharshunov</b> .....	76

On Complexity of Checking of Cryptosystems <b>Volodymyr G. Skobelev</b> .....	82
Distributed Fault Simulation and Genetic Test Generation of Digital Circuits <b>Skobtsov Y.A., El-Khatib A.I., Ivanov D.E</b> .....	89
Hierarchical Evolutionary Approach to Test Generation <b>Skobtsov V.Y. Skobtsov Y.A.</b> .....	95
<b>VERIFICATION</b>	
Incremental ABV for TLtoRTL Design Refinement <b>Nicola Bombieri, Franco Fummi, Graziano Pravadelli</b> .....	100
RTL Compiler Templates Verification: Approach to Automation <b>Lev Danielyan, Sergey Hakobyan</b> .....	108
Verification of Implementation of Parallel Automata (Symbolic Approach) <b>Andrei Karatkevich</b> .....	112
SystemCFL: An Infrastructure for a TLM Formal Verification Proposal (with an overview on a tool set for practical formal verification of SystemC descriptions) <b>K.L. Man, Andrea Fedeli, Michele Mercaldi, M.P. Schellekens</b> .....	116
System Level Methodology for Functional Verification SoC <b>Alexander Adamov, Sergey Zaychenko, Yaroslav Miroshnychenko, Olga Lukashenko</b> .....	122
Path Sensitization at Functional Verification of HDL-Models <b>Alexandr Shkil, Yevgeniya Syrevitch, Andrey Karasyov, Denis Cheglikov</b> .....	126
Dynamic Register Transfer Level Queues Model for High-Performance Evaluation of the Linear Temporal Constraints <b>Vladimir Hahanov, Oleg Zaharchenko, Sergiy Zaychenko</b> .....	132
The Automation of Formal Verification of RTL Compilers Output <b>Pavlush Margarian</b> .....	140
<b>LOGIC, SYSTEM AND PHYSICAL SYNTHESIS</b>	
Congestion-Driven Analytical Placement <b>Andrey Ayupov, Alexander Marchenko</b> .....	143
Estimation of Finite State Machine Realization Based on PLD <b>E. Lange, V. Chapenko, K. Boule</b> .....	149
Encoding of Collections of Fragment of Variables <b>Barkalov A.A., Ahmad Fuad Bader, Babakov R.M.</b> .....	153
An Algorithm of Circuit Clustering for Logic Synthesis <b>O. Venger, I. Afanasiev, Alexander Marchenko</b> .....	156
CMOS Standard Cell Area Optimization by Transistors Resizing <b>Vladimir Rozenfeld, Iouri Smirnov, Alexander Zhuravlev</b> .....	163
Optimization of Address Circuit of Compositional Microprogram Unit <b>Wisniewski R., Alexander A. Barkalov, Larysa A. Titarenko</b> .....	167

Optimization of Circuit of Control Unit with Code Sharing <b>Alexander Barkalov, Larysa Titarenko, Małgorzata Kołopieńczyk .....</b>	<b>171</b>
Routing a Multi-Terminal Nets with Multiple Hard Pins by Obstacle-Avoiding Group Steiner Tree Construction <b>J. D. Cho, A. I. Erzin, V. V. Zalyubovsky .....</b>	<b>175</b>
Optimization for Electro- and Acousto-Optical Interactions in Low-Symmetric Anisotropic Materials <b>Kajdan Mykola, Laba Hanna, Ostrovskij Igor, Demyanyshyn Nataliya, Andrushchak Anatolij, Mytsyk Bohdan.....</b>	<b>179</b>
Force-Position Control of the Electric Drive of the Manipulator <b>A.V. Zuev, V.F. Filaretov .....</b>	<b>184</b>
<b>FAULT TOLERANCE</b>	
K-out-of-n and K(m,n) Systems and their Models <b>Romankevych V., Potapova K., Hedayatollah Bakhtari .....</b>	<b>189</b>
Fault Tolerant Systems with FPGA-based Reconfiguration Devices <b>Vyacheslav S. Kharchenko, Julia M. Prokhorova.....</b>	<b>190</b>
Fault-Tolerant Infrastructure IP-cores for SoC: Basic Variants and Realizations <b>Ostroumov Sergii, Ushakov A. A., Vyacheslav S. Kharchenko.....</b>	<b>194</b>
Fault-tolerant PLD-based Systems on Partially Correct Automaton <b>Nataliya Yakymets, Vyacheslav Kharchenko.....</b>	<b>198</b>
FME(C)A-Technique of Computer Network Reliability and Criticality Analysis <b>Elyasi Komari Iraj, Anatoliy Gorbenko.....</b>	<b>202</b>
<b>TEST GENERATION AND TESTABILITY</b>	
Scan Based Circuits with Low Power Consumption <b>Ondřej Novák, Zdeněk Pliva.....</b>	<b>206</b>
Memory Address Generation for Multiple Run March Tests with Different Average Hemming Distance <b>S.V. Yarmolik, V.N. Yarmolik.....</b>	<b>212</b>
Structural Method of Pseudorandom Fixed Weight Binary Pattern Sequences Generation <b>Romankevych A., Grol V., Fallahi Ali .....</b>	<b>217</b>
Test Pattern Generation for Bridge Faults Based on Continuous Approach <b>N. Kascheev, F. Podyablonsky .....</b>	<b>222</b>
Hierarchical Analysis of Testability for SoCs <b>Maryna Kaminska, Vladimir Hahanov, Elvira Kulak, Olesya Guz.....</b>	<b>226</b>
Embedded Remote Wired or Wireless Communication to Boundary-Scan Architectures <b>Mick Austin, Ilkka Reis, Anthony Sparks.....</b>	<b>231</b>
Economics Modeling the DFT of Mixed-Signal Circuits <b>Sergey G. Mosin .....</b>	<b>236</b>
<b>CAD TOOLS AND DEVICES</b>	
Optimal Electronic Circuits and Microsystems Designer <b>A.I. Petrenko .....</b>	<b>239</b>

Computer Aided Design Support of FSM Multiplicative Decomposition <b>Alexander Sudnitson, Sergei Devadze .....</b>	<b>241</b>
Complex Process Engineering of Projection of Electronic Devices by Means of Automized System SATURN <b>D.V. Bagayev, A.C. Firuman .....</b>	<b>247</b>
Hand-Held Mobile Data Collecting Terminal <b>Armen Saatchyan, Oleg Chuvilo, Chaitanya Mehandru.....</b>	<b>252</b>
Logic and Fault Simulation Based on Multi-Core Processors <b>Volodymyr Obrizan, Valeriy Shipunov, Andiry Gavryushenko, Oleg Kashpur .....</b>	<b>255</b>
HES-MV – A Method for Hardware Embedded Simulation <b>Vladimir Hahanov, Anastasia Krasovskaya, Maryna Boichuk, Oleksandr Gorobets .....</b>	<b>257</b>
Hierarchical Approach for Functional Verification of HW/SW System on Chip (SoC) <b>Oleksandr Yegorov, Podkolzin N., Yegor Denisov, Andrey Yazik .....</b>	<b>264</b>
Output Buffer Reconfiguration in Case of Non Uniform Traffic <b>Vyacheslav Evgrafov .....</b>	<b>267</b>
<b>DESIGN METHODS AND MODELING</b>	
Time-Sensitive Control-Flow Checking Monitoring for Multitask SoCs <b>Fabian Vargas, Leonardo Picolli, Antonio A. de Alecrim Jr., Marlon Moraes, Márcio Gama.....</b>	<b>272</b>
Development and Application of FSM-Models in Active-HDL Environment for Network Protocols Testing <b>Anna.V. Babich, Oleksandr Parfentiy, Eugene Kamenuka, Karina Mostovaya .....</b>	<b>279</b>
How to Emulate Network-on-Chip? <b>Peeter Ellervee, Gert Jervan .....</b>	<b>282</b>
Multistage Regular Structure of Binary Counter of ones Arbitrary Modulo <b>Saposhnikov V. V., Saposhnikov VL. V., Urganskov D. I. ....</b>	<b>287</b>
An Enhanced Analogue Current-Mode Structure of WP Control Circuit of Neural Networks <b>Hossein Aghababa, Leyla S.Ghazanfari, Behjat Forouzandeh.....</b>	<b>291</b>
One-Parameter Dynamic Programming Algorithm for Optimal Wire Selection Under Elmore Delay Model <b>A.I. Erzin, V.V. Zalyubovsky .....</b>	<b>296</b>
Analytical Model of Clock Skew in Buffered H-Trees <b>Dominik Kasprowicz .....</b>	<b>301</b>
High-Level Facilities for Modeling Wireless Sensor Networks <b>Anatoliy Doroshenko, Ruslan Shevchenko, Konstantin Zhreb.....</b>	<b>305</b>
Class E Power Amplifier for Bluetooth Applications <b>Olga Antonova, George Angelov, Valentin Draganov.....</b>	<b>311</b>
An Automation Method for Gate-Count Characterization of RTL Compilers <b>Arik Ter-Galstyan .....</b>	<b>313</b>
Algorithmic Method of The Tests Forming for Models Verification of Microcircuits Memory <b>M.K. Almaid, V.A. Andrienko, V.G. Ryabtsev .....</b>	<b>317</b>

SUM IP Core Generator – Means for Verification of Models–Formulas for Series Summation in RKHS <b>Vladimir Hahanov, Svetlana Chumachenko, Olga Skvortsova, Olga Melnikova</b> .....	322
Design of Wavelet Filter Bank for JPEG 2000 Standard <b>Hahanova I.V., Hahanov V.I., Fomina E., Bykova V., Sorudeykin K.</b> .....	327
Design of Effective Digital Filters in FPGA <b>Pavel V. Plotnikov</b> .....	332
<b>POSTER SESSION</b>	
Applications of Combinatorial Cyclic Codes for Images Scan and Recognition <b>Vladimir Valkovskii, Dmitry Zerbino, Oleg Riznyk</b> .....	335
Architecture of Internet Access to Distributed Logic Simulation System <b>Ladyzhensky Y.V., Popoff Y.V.</b> .....	339
Computer System Efficient Diagnostics with the Usage of Real-Time Expert Systems <b>Gennady Krivoulya, Alexey Lipchansky, Olga Korobko</b> .....	344
DASPUD: a Configurable Measurement Device <b>Nikolay P. Molkov, Maxim A. Sokolov, Alexey L. Umnov, Dmitry V. Ragozin</b> .....	348
Design Methods of Self-Testing Checker for Arbitrary Number of Code Words of (m,n) Code <b>Yu. B. Burkatovskaya, N.B. Butorina, A. Yu. Matrosova</b> .....	355
Dynamic Heat and Mass Transfer in Saline Water due to Natural Convection Flow over a Vertical Flat Plate <b>Rebhi A. Damseh</b> .....	361
Effect of Driving Forces On Cylindrical Viscoelastic Fluid Flow Problems <b>A. F. Khadrawi, Salwa Mrayyan, Sameh Abu-Dalo</b> .....	366
Evolutional Methods for Reduction of Diagnostic Information <b>D. Speranskiy</b> .....	371
Evolutionary Algorithms Design: State of the Art and Future Perspectives <b>Yuri R. Tsoy</b> .....	375
Functional properties of faults on fault-secure FSM design with observing only FSM outputs <b>S. Ostanin</b> .....	380
Hardware Methods to Increase Efficiency of Algorithms for Distributed Logic Simulation <b>Ladyzhensky Y.V., Teslenko G.A.</b> .....	385
Information Embedding and Watermarking for Multimedia and Communication <b>Aleksandr V. Shishkin</b> .....	386
Low Contrast Images Edge Detector <b>I.V. Ruban, K.S. Smelyakov, A.S. Smelyakova, A.I. Tymochko</b> .....	390
Minimization of Communication Wires in FSM Composition <b>S.V. Zharikova, N.V. Yevtushenko</b> .....	397
Neuro-Fuzzy Unit for Real-Time Signal Processing <b>Ye. Bodyanskiy, S. Popov</b> .....	403

On Decomposition of Petri Net by Means of Coloring <b>Wegrzyn Agnieszka</b> .....	407
Single-Argument Family of Continuous Effectively Computed Wavelet Transforms <b>Oleg E. Plyatsek, Majed Omar Al-Dwairi</b> .....	414
Synthesis Methods of Finite State Machines Implemented in Package ZUBR <b>Valery Salauyou, Adam Klimowicz, Tomasz Grzes, Teodora Dimitrova-Grekow, Irena Bulatowa</b> .....	420
Synthesis of Logic Circuits on Basis of Bit Transformations <b>Yuri Plushch, Alexander Chemeris, Svetlana Reznikova</b> .....	423
System of K-Value Simulation for Research Switching Processes in Digital Devices <b>Dmitrienko V.D., Gladkikh T.V., Leonov S.Yu</b> .....	428
Test Points Placement Method for Digital Devices Based on Genetic Algorithm <b>Klimov A.V., Speranskiy D.V.</b> .....	436
The Approach to Automation of Designing Knowledge Base in the Device-Making Industry <b>O.V. Bisikalo</b> .....	440
The Optimal Nonlinear Filtering of Discrete-Continuous Markovian Processes in Conditions of Aposteriori Uncertainty <b>Victor V. Panteleev</b> .....	443
The Realization of Modified Artificial Neural Network for Information Processing with the Selection of Essential Connections by the Program Meganeuro <b>E.A. Engel</b> .....	450
Web-system Interface Prototype Designing <b>Globa L.S., Chekmez A. V., Kot T. N.</b> .....	453
A Bio-Inspired Method for Embedded System Scheduling Problems <b>Abbas Haddadi, Saeed Safari, Behjat Forouzandeh</b> .....	456
Iterative Array Multiplier with On-Line Repair of Its Functions <b>Drozd A., Lobachev M., Reza Kolahi, Drozd J.</b> .....	461
Mathematical Modeling and Investigation of a Main SDH-Network Structural Reliability <b>M.M. Klymash, I.M. Dronyuk, R.A. Burachok</b> .....	464
Experimental Investigation of Two Phase Flow Pressure Drop and Contraction on Tee Junction <b>Shannak Benbella, Al-Qudah Kalid, Al-Salaymeh Ahmed, Hammad Mahmoud, Alhusein Mahmoud</b> .....	467
Application of Adaptive and New Planning Methods to Solve Computer-Aided Manufacturing Problems <b>Nevludov I.Sh., Litvinova E.I., Evseev V.V., Ponomarjova A.V.</b> .....	472
Petri Net Decomposition Algorithm based on Finding Deadlocks and Traps <b>Agnieszka Wegrzyn, Marek Wegrzyn</b> .....	477
Testing for Realistic Spot Defects in CMOS Technology: a Unified View <b>Michel Renovell</b> .....	482
<b>AUTHORS INDEX</b> .....	483

# System Level Methodology for Functional Verification Soc

Alexander Adamov, Sergey Zaychenko, Yaroslav Myroshnychenko, Olga Lukashenko  
Design Automation Department, Kharkov National University of Radio Electronics,  
Lenin ave, 14, Kharkov, 61166 Ukraine  
E-mail: [adlex@onet.com.ua](mailto:adlex@onet.com.ua)

## Abstract

*Building a verification environment and the associated tests is a highly time-consuming process. Most project reports indicate that between 40% and 70% of the entire effort of a project is spent on verification, with 70% being much closer to the normal level for successful projects [1]. This high level of effort indicates that the potential gains to be made with successful re-use are significant. Most projects do not start with a complete set of hardware designs available for a functional verification. Usually a design comes together as smaller blocks. Then the blocks are integrated into larger blocks, which may eventually be integrated into a system. That is reason for performing functional verification at a system level. The paper describes the system-level modeling environment for a functional verification System-on-a-Chip models. System level allow design teams to rapidly create large system-on-a-chip designs (SOCs) by integrating premade blocks that do not require any design work or verification.*

**Keywords:** device simulation, verification, system level modeling, System-on-a-Chip.

## 1. Introduction

One of the hottest topics in embedded system design today is Electronic System Level (ESL) design. Although the idea of being able to describe a system at an abstract level has been around for a decade, only now are various parts of the design flow becoming available to make it practical. ESL describes a System-on-chip (SoC) design in an abstract enough and fast enough way to explore the design space and provide virtual prototypes for hardware and software implementation. It is becoming a fundamental part of the design flow because we can now use it throughout the iterative design process rather than just in the early system architecting phase.

ESL provides tools and methodologies that let designers describe and analyze chips on a high level of abstraction, easing the pain of designing electronic

systems which would otherwise be too costly, complex or time consuming to create.

The adoption of ESL can be seen in the same light as the transition to register transfer level (RTL) methodologies 10-15 years ago when complexity and time-to-market pressures obliged the industry to step up to another design level.

As designs become larger with more and more IP blocks, engineers will re-use more IP. ESL methodologies that enable platform-based design will be increasingly necessary to create and test a complete system.

For the most complex SoCs, IP reuse can only help up to a point. For a 40-million-gate SoC, filling even 75% of the device with existing IP leaves 10 million gates to design with original content. ESL methodologies which allow rapid creation of new blocks are likely to be leveraged by designers to quickly develop and verify original content to fill the 10 million gate void while meeting time-to-market requirements.

Among the 24% percent of respondents who have implemented some form of ESL design methodology an overwhelming 87% believe ESL provides an acceptable or greater return on investment (Figure 1).

ROI FOR IMPLEMENTING ESL

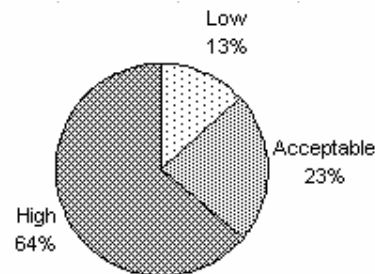


Figure 1. Return on investment for implementing ESL

This is an important statistic as it illustrates that ESL is succeeding in early deployments. Early success fosters positive references which can be a critical factor in mainstream designers' decision to investigate a new methodology [2].

Currently system level design is not well supported in industry [4]. This hinders verification and validation

of system properties and functionality. These activities should begin as early as possible in the development process.

*Goal of this paper* is to describe effectiveness of the system-level simulation on the base of available digital simulation system, development of the functional prototype of the verification environment software. The *main research topics* include:

- benefits of using system description at high level of abstraction;
- architectural and functional features for building system-level verification environment within experimental Integrated Verification System.

## 2. ESL Methodology Overview

ESL design is being enabled in three ways:

- constraints and parameters from the high level of abstraction can now pass down into different implementation tools;
- a tighter linking of system designs into the early verification process better justifies the engineering investment;
- bit-true and cycle-accurate versions of execution platforms early in the design cycle are enabling embedded software development and integration to start earlier.

The growth of the ESL is based on emerging standards for passing data and design constructs through the development process between different design tools. Early tools that tried to tackle ESL design imposed new, and often proprietary, design flows, languages and coding styles on the designer, and that was the major reason these tools failed to take hold in the late 1990s. Another reason was that the design world lacked the libraries of blocks of intellectual property (IP) and the models of functions that could be used to construct these systems.

Providing virtual prototypes means that software development can start much earlier. With the models of the hardware available, embedded software can be written and tested by multiple software engineering groups in parallel, and tested against a standard set of criteria on a virtual prototype. This saves time in the development and makes the hardware/software co-verification process a lot simpler.

Getting an early functional representation of the SoC is a key advantage to adopters of the ESL design process and it mirrors the way Register Transfer Level (RTL) design was originally adopted by designers in the 1980s.

Today, the ESL tools are being proven in the same way, being used initially for modeling, verification and validation, and then moving out into other parts of the

design flow where the automatic generation of hardware and software speeds up the design process. Block-assembly and configuration data flow from high level SystemC descriptions to RTL and then to the gate level has now been demonstrated, and standards for broad-based adoption of these techniques are emerging.

As more and more of the system is configurable, such as different processor cores, different bus widths, different memory sizes and configuration, different programmable engines, and many, many different mixes of peripherals, the ability to simulate the different options early on in the design is extremely valuable. This can be used to develop a platform of devices, ensuring that they will meet the requirements of the applications and allowing the ever increasing cost of custom designs – both in the development and mask costs – to be spread across a wider range of devices and customers.

There are three distinct approaches to ESL, and some of the tool vendors today are using the term in ways that confuse the three. At the highest level is the Algorithmic approach, while at the design and implementation level there is the Architectural exploration, and thirdly there is the Automatic generation phase.

Simulation is the key at this level of design abstraction. SystemC models provide the ability to simulate the functions of the system thousands or millions of times faster than at the RTL level, but the trade-off is the timing accuracy.

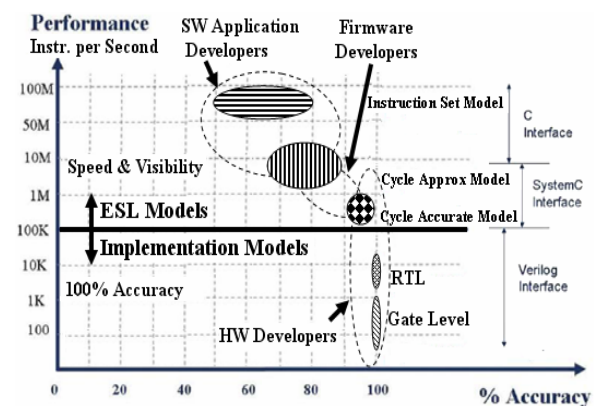


Figure 2. Where high level ESL models can be used

For example, functionally accurate (bit-true) models that are un-timed or cycle-count accurate can run from 10MIPS to multiple-100MIPS in system simulation, while the cycle accurate versions run in the 100KMIPS to megahertz range (Figure 2). These “benchmark simulations” are true to RTL timings with only a few noted timing exceptions and these can be used to check system-behavior down to the clock-cycle level.

The key to linking ESL design to the hardware and software tool chains is the definition of transaction level communication between abstract models and hardware implementation. A “transaction” is a collection of detailed signal data, such as a full memory read or write, which in a hardware simulation is spread over a number of specific input /output signals and clock-periods. These transactions can be used whether the block is SystemC, C code or RTL. To interface models to hardware simulations, transactions are decoded by a transactor, which transforms the transactions into signal values for hardware blocks, behaving like a data level translator with a buffering capability [3].

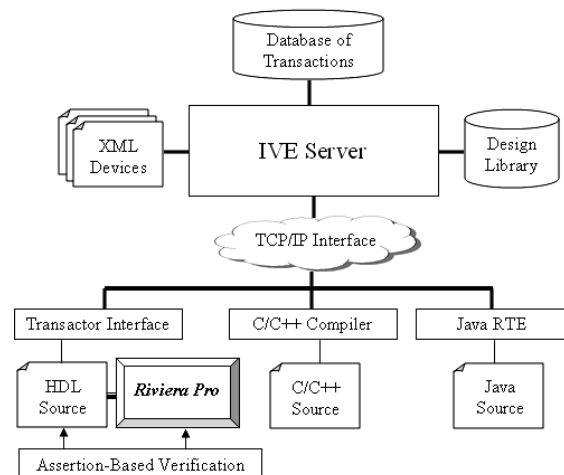


Figure 3. Verification Environment Architecture

### 3. Experimental Integrated Verification System

Heart of the verification environment is the server software, which controls the dataflow in the system. Devices are entered in the system by means of loading their interfaces in XML format. At the same time in a project library the prototype of the system component is created. Adding these devices we connect them with the corresponding prototype. The communication environment used for data transferring is TCP/IP network protocol. Handing on of packages is carried out with the help of Windows Sockets 2 mechanism. The information about simulation is saved within a transaction's database. Subsequently this information can be used for a static verification and revealing of the observed parameters violation.

Using the network interface given by specially developed communication library client models can be hooked up. How we can see from the picture it can be the HDL models connected with the help of transactors and simulated within hardware simulator. Also we can use prototypes and the testbenches written in high-level languages, such as C/C++, Java.

### 3.2 Functionality Overview

Despite of experimental character of the developed program system, implementation allows to present perspective functionalities of valuable implementation. The basic functions are:

- entering of SoC components in the simulation system, described in XML format;
- connecting simulated devices by means of network TCP/IP protocol;
- co-simulation of components at a different levels of abstraction.

As was mentioned before with help of Integrated Verification System we can simulate components described as RTL models. Figure 4 represent dataflow in case of RTL components simulation. For system-level modeling we need to transform data from RTL signals to more abstract implementation level. We can do that by means of involving transactor's layer, which allows us to make such conversion. Transformed data sends throw the Server of the system.

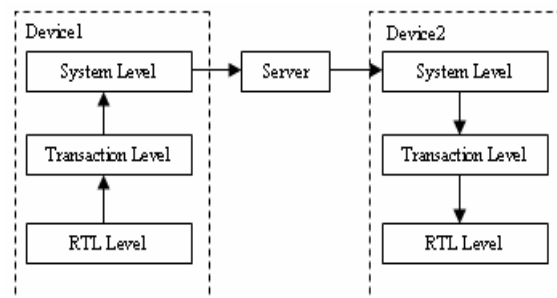


Figure 4. System Objects Interconnection

For the purpose of data transmitting within network environment we need to append additional information about transaction for packets' transmission (Figure 5). This information includes recipient address, instruction code and the data itself. After receiving the data corresponding signal values for hardware blocks will be established inside of transactor's method and then they will be delivered to HDL simulator.

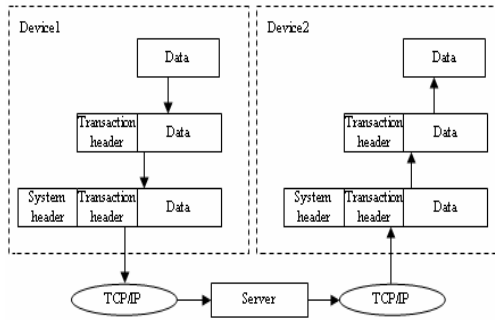


Figure 5. Data forwarding through the system

The designed system allows:

- engineering the virtual prototype of the system;
- early software validation of the system;
- performance analysis of the system;
- transaction-level verification of the project;
- architectural analysis of SoC;
- power analysis of a chip;
- searching hardware/software tradeoffs.

Thus the system enables to speed up the process of simulation going up to higher level of abstraction.

### 3.3 Graphical User Interface

Figure 6 shows a graphical user interface of the system. On the background we can see Riviera Verification Solution, which is integrated to simulation environment. The top application is a server part, which contains three panels. In the left upper panel we can see the list of loaded devices with a pointing of their interfaces. In the right panel there are graphics representations of the components, and also their current state is shown. Below there is a console that print out information about modeling and the transmitted data, which can be saved to the appropriate log-file.

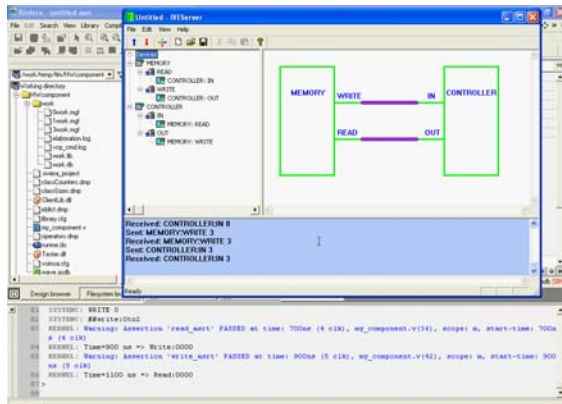


Figure 6. Graphical User Interface

### 4. Conclusion

The nowadays trends of using system-level simulation for SoC models was presented in this paper. The prototype of the mixed-level verification

environment with support of TCP/IP communication interface, transaction-level modeling and assertion-based verification on the base of existing digital simulation tool – Aldec Riviera has been developed.

The following tasks have been solved: 1) Defined basic mixed-level simulation software architecture; 2) Suggested new technique for interconnection of SoC components; 3) Considered possibility of implementing ESL methodology for functional verification SoC models; 4) Showed potential of using different kinds of verification within SoC model; 5) Implemented results of the research within experimental software system.

Using ESL methodology in design and verification tasks that traditionally took weeks or months can now be done in minutes. It will provide a reliable way to get tens of millions of gates and hundreds of thousands of lines of embedded code written and validated quickly to meet the ever increasing customer demand. Tools in this area come from companies such as CoWare with ConvergenSC for Architectural ESL, Synopsys with its CoCentric System Studio, Prosilog's Magillem and ARM's RealView MaxSim. All these target the early design exploration, which indicates a maturing of the market for ESL tools. For instance, Samsung has reported savings of approximately 40% in design time through the use of ESL tools [3].

A large Japanese printer company adopted ESL design methodology because its RTL-based methodology could no longer cope with the architectural modifications required by each generation of printers. The company uses the same basic algorithms for its whole product range, from low-end home printers to high-end network printers. However, major variations in data communications, processing and storage requirements between the different printer types mandate different implementations of those algorithms, including different memory and communications bus architectures [5]. Qualcomm Inc.'s experience demonstrates improved HW/SW co-verification at the system level over that at the C/RTL implementation level. A Viterbi decoder design executed a packet in 20ms, but took 6hrs to simulate at C/RTL level. Qualcomm estimates that 1,000 packets must be simulated to achieve a reasonable confidence level, but considers the necessary 6,000 hours of simulation time to be impractical. Co-verification of 1,000 packets with a ESL would have taken 6 hours or less [5].

Further research will be done in the area of developing methods for simulation results analyzing with help of statistical and data mining approaches.

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## AUTHORS INDEX

- Adamov Alexander 122  
Afanasyev I. 156  
Aghababa Hossein 291  
Ahmad Fuad Bader 153  
Aleksanyan K. 72  
Alhusein Mahmoud 467  
Almaid M.K. 317  
Al-Qudah Kalid 467  
Al-Salaymeh Ahmed 467  
Andrienko V.A. 317  
Andrushchak Anatolij 179  
Angelov George 311  
Antonio A. de Alecrim Jr. 272  
Antonova Olga 311  
Austin Mick 231  
Ayupov Andrey 143
- Babakov R.M. 153  
Babich Anna 278  
Bagayev D.V. 247  
Barkalov A.A. 153, 167, 171  
Belkin Victor 76  
Bengtsson Tomas 42  
Benso A. 11  
Bisikalo O.V. 440  
Bodyanskiy Ye. 403  
Boichuk Maryna 257  
Bombieri Nicola 100  
Bosio A. 11  
Boule K. 149  
Bulatowa Irena 420  
Burachok R.A. 464  
Burkatovskaya Yu. B. 355  
Butorina N.B. 355  
Bykova V. 327
- Chaitanya Mehandru 252  
Chapenko V. 149  
Cheglikov Denis 126  
Chekmez A.V. 453  
Chemeris Alexander 423  
Cho J.D. 175  
Chumachenko S. 322  
Chuvilo Oleg 252
- Danielyan Lev 108  
Demyanyshyn N. 179  
Denisov Yegor 264  
Devadze Sergei 241  
Dimitrova-Grekow Teodora 420  
Dmitrienko V.D. 428  
Doroshenko Anatolij 305  
Draganov Valentin 311  
Dronyuk I.M. 464  
Drozd A. 461  
Drozd J. 461  
Eles P. 16
- El-Khatib A.I. 89  
Ellervee Peeter 282  
Elyasi Komari Iraj 202  
Engel E.A. 450  
Erzin A.I. 175, 296  
Evgrafov Vyacheslav 267  
Evseev V.V. 472  
Eyck Jentzsch 41
- Fallahi Ali 217  
Fedeli Andrea 116  
Filaretov V.F. 184  
Firuman A.C. 247  
Fomina E. 327  
Forouzandeh Behjat 291, 456  
Foty Daniel 29  
Fuchs G. 59  
Fummi Franco 100
- Gama Márcio 272  
Gavryushenko Andiry 255  
Ghazanfari Leyla S. 291  
Girard P. 47  
Gladkikh T.V. 428  
Globa L.S. 453  
Gorbenko Anatolij 202  
Gorobets O. 257  
Grol V. 217  
Grzes Tomasz 420  
Guz Olesya 226
- Haddadi Abbas 456  
Hahanov Vladimir 53, 132, 226, 257, 322, 327  
Hahanova A. 53  
Hahanova I.V. 327  
Hakobyan Sergey 108  
Hammad Mahmoud 467  
Handl T. 59  
Hanna Laba 179  
Harutunyan G. 68  
Hedayatollah Bakhtari 189  
Heiber Jan 59
- Ivanov Andre 22  
Ivanov D.E. 89  
Izosimov V. 16
- Jerraya Ahmed 23  
Jervan Gert 282  
Jutman Artur 42
- Kajdan Mykola 179  
Kamenuka Eugene 278  
Kaminska Maryna 226  
Karasyov Andrey 126  
Karatkevich Andrei 112  
Karavay Michail F. 24  
Kascheev N. 222  
Kashpur Oleg 255  
Kasprowicz Dominik 301  
Khadrawi A. F. 366  
Kharchenko V. 190, 194, 198  
Klimov A.V. 436  
Klimowicz Adam 420  
Klymash M.M. 464  
Kolopieńczyk Małgorzata 171  
Korobko Olga 344  
Kot T.N. 453  
Krasovskaya A. 257  
Krivoulya Gennady 344  
Kulak Elvira 226  
Kumar Shashi 42
- Ladyzhensky Y.V. 339, 385  
Landrault C. 47  
Lange E. 149  
Leonov S.Yu. 428  
Lipchansky Alexey 344  
Litvinova E.I. 472  
Lobachev M. 461  
Lukashenko Olga 122
- Majed Omar Al-Dwairi 414  
Man K.L. 116  
Marchenko A. 143, 156  
Margarian Pavlush 140  
Matrosova A.Yu. 355  
Melnik D. 53  
Melnikova Olga 322  
Mercaldi Michele 116  
Molkov Nikolay P. 348  
Moraes Marlon 272  
Mosin Sergey 236  
Mostovaya Karina 278  
Miroshnychenko Yaroslav 122  
Mytsyk Bohdan 179
- Novák Ondřej 206  
Nevludov I.Sh. 472
- Obrizan Volodymyr 255  
Ostanin S. 380  
Ostroumov Sergii 194  
Ostrovskij Igor 179
- Panteleev Victor V. 443  
Paolo Prinetto 11  
Parfentiy Oлександр 278  
Peng Zebo 16, 42  
Petrenko A.I. 239  
Picolli Leonardo 272  
Plotnikov Pavel V. 332  
Plushch Yuri 423  
Plyatsek Oleg E. 414  
Podkolzin N. 264  
Podyablonsky F. 222  
Ponomarjova A.V. 472  
Pop P. 16  
Popoff Y.V. 339  
Popov S. 403  
Potapova K. 189  
Pravadelli Graziano 100  
Pravossoudovitch S. 47  
Prokhorova Julia 190
- Ragozin Dmitry V. 348  
Rebhi A. Damseh 361  
Reis Ilkka 231  
Renovell Michel 482  
Reza Kolahi 461  
Reznikova Svetlana 423  
Riznyk Oleg 335  
Romankevych A. 217  
Romankevych V. 189  
Rousset A. 47  
Rozenfeld Vladimir 163  
Ruban I.V. 390  
Ryabtsev V.G. 317
- Saatchyan Armen 252  
Safari Saeed 456  
Salauyou Valery 420  
Salwa Mrayyan 366  
Sameh Abu-Dalo 366
- Saposhnikov V.V. 287  
Saposhnikov VL.V. 287  
Samvel Shoukourian 39  
Savino A. 11  
Schellekens M.P. 116  
Shannak Benbella 467  
Sharshunov Sergey 76  
Shevchenko Ruslan 305  
Shipunov Valeriy 255  
Shishkin Aleksandr V. 386  
Shkil Alexandr 126  
Sinelnikov V. 24  
Skobelev Volodymyr 82  
Skobtsov V.Y. 95  
Skobtsov Y.A. 89, 95  
Skvortsova Olga  
Smelyakov K.S. 390  
Smelyakova A.S. 390  
Smirnov Iouri 163  
Sokolov Maxim A. 348  
Sorudeyin Kirill 327  
Sparks Anthony 231  
Speranskiy D. 371, 436  
Steininger A. 59  
Sudnitson Alexander 241  
Syrevitch Yevgeniya 126
- Ter-Galstyan Arik 313  
Teslenko G.A. 385  
Titarenko Larysa, 167, 171  
Tsoy Yuri R. 375  
Tymochko A.I. 390
- Ubar Raimund 42  
Umnov Alexey L. 348  
Urganskov D.I. 287  
Ushakov A.A. 194
- Valkovskii Vladimir 335  
Vardanian Valery 68, 72  
Vargas Fabian 272  
Venger O. 156  
Virazel A. 47
- Wegrzyn A. 407, 477  
Wegrzyn M. 477  
Wisniewski R. 167
- Yakymets Nataliya 198  
Yeliseev V. 53  
Yarmolik S.V. 212  
Yarmolik V.N. 212  
Yazik Andrey 264  
Yegorov Oлександр 264  
Yeliseev V. 53  
Yevtushenko N.V. 397
- Zaharchenko Oleg 132  
Zalyubovsky V.V. 175, 296  
Zangerl F. 59  
Zaychenko S. 122, 132  
Zdeněk Pliva 206  
Zerbino Dmitry 335  
Zharikova S.V. 397  
Zhereb Konstantin 305  
Zhuravlev Alexander 163  
Zorian Yervant 22, 39  
Zuev A.V. 184