

KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012)

Copyright © 2012 by the Institute of Electrical and Electronics Engineers, Inc.



Technically Co-Sponsored by



Kharkov, Ukraine, September 14 – 17, 2012

IEEE EAST-WEST DESIGN AND TEST SYMPOSIUM 2012 COMMITTEE

General Chairs

V. Hahanov – Ukraine
Y. Zorian – USA

General Vice-Chairs

R. Ubar - Estonia
P. Prinetto - Italy

Program Chairs

S. Shoukourian – Armenia
D. Speranskiy – Russia

Program Vice-Chairs

Z. Navabi – Iran
M. Renovell – France

Publicity Chair's

G. Markosyan - Armenia
S. Mosin - Russia

Public Relation Chair

V. Djigan - Russia

Program Committee

E. J. Aas - Norway
J. Abraham - USA
M. Adamski - Poland
A.E.Mohamed Mohamed - Egypt
A . Barkalov - Poland
R. Bazylevych - Ukraine
A. Chaterjee - USA
V. Djigan - Russia

A. Drozd - Ukraine
E. Evdokimov - Ukraine
E. Gramatova - Slovakia
A. Ivanov - Canada
M. Karavay - Russia
V. Kharchenko - Ukraine
K. Kuchukjan - Armenia
W. Kuzmich - Poland
A. Matrosova - Russia
V. Melikyan - Armenia
L. Miklea - Romania
O. Novak - Czech Republic
Z. Peng - Sweden
A. Petrenko - Ukraine
J. Raik - Estonia
A. Romankevich - Ukraine
A. Ryjov - Russia
R. Seinauskas - Lithuania
S. Sharshunov - Russia
A. Singh - USA
J. Skobtsov - Ukraine
V. Tverdokhlebov - Russia
V. Vardanian - Armenia
V. Yarmolik - Byelorussia

Steering Committee

M. Bondarenko - Ukraine
V. Hahanov - Ukraine
R. Ubar - Estonia
Y. Zorian - USA

Organizing Committee

S. Chumachenko - Ukraine
E. Litvinova – Ukraine
V. Kharchenko – Ukraine

EWDTS 2012 CONTACT INFORMATION

Prof. Vladimir Hahanov
Design Automation Department
Kharkov National University of Radio Electronics,
14 Lenin ave,
Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26
E-mail: hahanov@kture.kharkov.ua
Web: www.ewdtest.com/conf/

10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium (EWDTS)** is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics <http://anpre.org.ua/> in cooperation with Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Trades Committee of Kharkov National University of Radioelectronics and Trades Committee of Students, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University.



CONTENTS

An Efficient Fault Diagnosis and Localization Algorithm for Successive-Approximation Analog to Digital Converters Melkumyan T., Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.	15
Application of Defect Injection Flow for Fault Validation in Memories Amirkhanyan K., Davtyan A., Harutyunyan G., Melkumyan T., Shoukourian S., Vardanian V., Zorian Y.	19
SSBDDs and Double Topology for Multiple Fault Reasoning Raimund Ubar, Sergei Kostin, Jaan Raik	23
Self Compensating Low Noise Low Power PLL design Vazgen Melikyan, Armen Durgaryan, Ararat Khachatryan, Manukyan Hayk, Eduard Musaelyan	29
Optimization Considerations in QCA Designs Zahra NajafiHaghi, Marzieh Mohammadi, Behjat Forouzandeh, Zainalabedin Navabi	33
Implementation of Address-Based Data Sorting on Different FPGA Platforms Dmitri Mihhailov, Alexander Sudnitson, Valery Sklyarov, Ioulia Skliarova	38
Comparison of Model-Based Error Localization Algorithms for C Designs Urmaz Repinski, Jaan Raik	42
Synthesis of Clock Trees for Sampled-Data Analog IC Blocks Bilgiday Yuce, Seyrani Korkmaz, Vahap Baris Esen, Fatih Temizkan, Cihan Tunc, Gokhan Guner, I. Faik Baskaya, Iskender Agi, Gunhan Dundar, H. Fatih Ugurdag	46
Experiences on the road from EDA Developer to Designer to Educator H. Fatih Ugurdag	50
Multi-Beam Constant Modulus Adaptive Arrays in Real-Valued Arithmetic Victor I. Djigan	54
Simulation of Total Dose Influence on Analog-Digital SOI/SOS CMOS Circuits with EKV-RAD macromodel Petrosyants K. O., Kharitonov I. A., Sambursky L. M., Bogatyrev V. N., Povarnitcyna Z. M., Drozdenko E. S.	60
Models for Embedded Repairing Logic Blocks Hahanov V.I., Litvinova E.I., Frolov A., Tiecoura Yves	66
Real-time Interconnection Network for Single-Chip Many-Core Computers Harald Richter	72
Invariant-Oriented Verification of HDL-Based Safety Critical Systems Kharchenko V., Konorev B., Sklyar V., Reva L.	76
An Improved Scheme for Pre-computed Patterns in Core-based SoC Architecture Elahe Sadredini, Qolamreza Rahimi, Paniz Foroutan, Mahmood Fathy, Zainalabedin Navabi	80

Synthesis of Moore FSM with transformation of system in CPLD Aleksander Barkalov, Larysa Titarenko, and Sławomir Chmielewski	85
A WSN Approach to Unmanned Aerial Surveillance of Traffic Anomalies: Some Challenges and Potential Solutions David Afolabi, Ka Lok Man, Hai-Ning Liang, Eng Gee Lim, Zhun Shen, Chi-Un Lei, Tomas Krilavičius, Yue Yang, Lixin Cheng, Vladimir Hahanov, and Igor Yemelyanov	91
Synthesis of Qubit Models for Logic Circuits Wajeb Gharibi, Zaychenko S.A., Dahiri Farid, Hahanova Yu.V., Guz O.A., Ngene Christopher Umerah, Adiele Stanley	95
Theory of Optimal Nonlinear Filtering in Infocommunication's Problems Victor V. Panteleev	102
Verification of Specifications in the Language L with respect to Temporal Properties Expressible by GR(1) Formulas Anatoly Chebotarev	110
Properties of code with summation for logical circuit test organization Anton Blyudov, Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov	114
Loop Nests Parallelization for Digital System Synthesis Alexander Chemeris, Julia Gorunova, Dmiry Lazorenko	118
Decreasing the Power Consumption of Content-Addressable Memory in the Dataflow Parallel Computing System Levchenko N.N., Okunev A.S., Yakhontov D.E., Zmejev D.N.	122
WebALLTED: Interdisciplinary Simulator Based on Grid Services Zgurovsky M., Petrenko A., Ladogubets V., Finogenov O., Bulakh B.	126
Malfunctions Modeling of Converters and Homogeneous-chain Distributed Structure Devices Artur Gulin, Zhanna Sukhinets	130
On structure of quasi optimal algorithm of analogue circuit designing Zemliak A., Michua A., Markina T.	134
A Neuro-Fuzzy Edge Based Spectrum Sensing Processor for Cognitive Radios Mohammadreza Baharani, Mohammad Aliasgari, Mohammadreza {Najafi, Jamali}, Hamid Noori	138
Qubit Model for Solving the Coverage Problem Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas, Eshetie Abebech Mandefro	142
PDF testability of the circuits derived by special covering ROBDDs with gates Matrosova A., Nikolaeva E., Kudin D., Singh V.	146
Compositional Microprogram Control Unit with Operational Automaton of Transitions Alexander Barkalov, Roman Babakov, Larisa Titarenko	151
Observability Calculation of State Variable Oriented to Robust PDFs and LOC or LOS Techniques Matrosova A., Ostanin S., Melnikov A., Singh V.	155

Low-Voltage Low-Power 2.5 GHz Linear Voltage Controlled Ring Oscillator Hayk H Dingchyan	161
High Speed IC Output Buffer with Reduced Power Consumption Karine Movsisyan	165
Engineering-Maintenance Methods of the Calculation Service Area Fixed BWA-paths Sergey I. Myshlyakov, Victor V. Panteleev	170
Analyses of two run march tests with address decimation for BIST procedure Ireneusz Mrozek, Svetlana V. Yarmolik	176
Design of Area Efficient Second Order Low Pass Analog Filter Andranik Hovhannisyan	180
Power Consumption Analysis of Content-Addressable Memories Levchenko N.N., Okunev A.S., Yakhontov D.E.	183
IC Physical Design Optimization Due to Effects of Device Physical Geometries Avag Sargsyan	187
System-on-Chip FPGA-Based GNSS Receiver Alexander Fridman, Serguey Semenov	190
Testware and Automatic Test Pattern Generation for Logic Circuits Victor Zviagin	196
Artificial Neural Network for Software Quality Evaluation Based on the Metric Analysis Oksana Pomorova, Tetyana Hovorushchenko	200
Self-Compensation of Influence of Parasitic Gate-Drain Capacitances of CMOS Transistors in Analog Microcircuitry Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov	204
Hash-based Detection of OFDM Watermarking Symbol for Radiotelephone Identification Aleksandr V. Shishkin, Aleksandr A. Lyashko	208
A Novel Wideband Circular Ring DGS Antenna Design for Wireless Communications Rakesh Sharma, Abhishek Kandwal, Sunil Kumar Khah	211
Universal technique of the analysis of round-off noise in digital filters with arbitrary structure described by topological matrixes Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev	215
Hardware Reduction for Compositional Microprogram Control Unit Dedicated for CPLD Systems Barkalov A., Titarenko L., Smolinski L.	219
Conservative Finite-difference Scheme for the Problem of Laser Pulse Propagation in a Medium with Third-order Dispersion Vyacheslav A. Trofimov, Anton D. Denisov	225
A Four Bit Low Power 165MSPS Flash-SAR ADC for Sigma-Delta ADC Applications Hasan Molaei, Khosrow Hajsadeghi	229
Matrix Implementation of Moore FSM with Nonstandard Presentation of State Codes Titarenko L., Hebda O.	233

Alowpower1.2GS/s4-bitflashADCin0.18mCMOS Mohammad Chahardori, Mohammad Sharifkhani, Sirous Sadughi	237
Symmetrical Differential Stages on CMOS Transistors with Circuits of Self-Compensation and Cancellation Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov	241
Lower Bound of Error in AOA Based Passive Source Localization Using Single Moving Platform Hejazi F., Norouzi Y., Nayebi M.M.	245
A Design for Testability Technique for Quantum Reversible Circuits Joyati Mondal, Debesh K. Das, Dipak K. Kole, Hafizur Rahaman	249
A Flexible Design for Optimization of Hardware Architecture in Distributed Arithmetic based FIR Filters Fazel Sharifi, Saba Amanollahi, Mohammad Amin Taherkhani, Omid Hashemipour	253
Models for Quality Analysis of Computer Structures Murad Ali Abbas, Chumachenko S.V., Hahanova A.V., Gorobets A.A., Priymak A.	258
Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology Daniel Foty, Bruce Smith, Saurabh Sinha, Michael Schröter	264
Sampling Theorem for Finite Duration Signal in Limited Frequency Band Gamlet S. Khanyan	270
SiGe HBT Performance Modeling after Proton Radiation Exposure Konstantin Petrosyants, Maxim Kozhukhov	274
Classical Models of Test used in Advanced Electronics Quality Assurance Surendra Batukdeo	278
The Use of Natural Resources for Increasing a Checkability of the Digital Components in Safety-Critical Systems Drozd A., Kharchenko V., Antoshchuk S., Drozd J., Lobachev M., Sulima J.	283
New version of Automated Electro-Thermal Analysis in Mentor Graphics PCB Design System Petrosyants K.O., Kozynko P.A., Kharitonov I.A., Sidorov A.V., Chichkanov Y. N.	289
An Approach to Testing of Planar Integrated Antennas in Frequency Range of 5–7 GHz Aleksandr Timoshenko, Ksenia Lomovskaya, Victor Barinov, Andrey Tikhomirov	293
Optimal project solution decision making in telecommunication systems using multicriteria optimization methods Valery Bezruk, Alexander Bukhanko	298
Software implementation and debugging of forward error correction codes Alexey Smirnov, Danila Migalin, Ilya Muravyev, Leonid Pertsev	303
Architecture of Built-In Self-Test and Recovery Memory Chips Andrienko V.A., Moamar Daa, Ryabtsev V.G., Utkina T.Yu.	307
The methods of exclusion of variables in symbolic time models of linear periodically time-variable circuit Yuriy Shapovalov, Dariya Smal	311

Two-Component Encoding of Approximating Picture Pixels in Telecommunication Facilities Barannik V., Dodukh A., Safronov R.	315
Development of parameterized cell using Cadence Virtuoso Vadim Borisov	319
Simulation Methods of Diffusion Alloying Process by Means of Taurus TSUPREM-4 Programme Lagunovich N.L., Borzdov V.M.	321
Control and Diagnosis by Complexity Indicators of System Functioning Process Tverdokhlebov V.A.	323
Features of the Transfer of Information with Different Reliability in a Single Channel Alexander Bakhtin, Leonid Pertsev, Olga Timofeeva	327
Construction of Signals with Controlled Peak-Factor Koshevyy V. M., Dolzhenko D.O.	330
The Effective Method of Space Filtering of Noise in Rayleigh Communication Channel with the Adaptive Antenna Maistrenko G. V., Rybalko A. M., Shokalo V. M., Strelnitskiy A. A.	333
A New Structure for Interconnect Offline Testing Somayeh Sadeghi-Kohan, Shahrzad Keshavarz, Farzaneh Zokaee, Farimah Farahmandi, Zainalabedin Navabi	336
Researching of Mathematical Models Based on Optimal Control Approaches for Congestion Control in Telecommunication Network Lemeshko A.V., Semenyaka M.V.	341
Higher Order Propagation Modes Error and Its Compensation Zaichenko O. B., Klyuchnyk I. I., Martynenko L. G.	345
Strategy of analyzing most common algorithms for path finding in discrete labyrinth using software statistic data collector Krasnov Evgeniy, Dmitry Bagaev	349
Method of Implementation of Technology of Orders Based Transparent Parallelizing for Solving Computationally Complex Problems on Cluster Vitaliy D. Pavlenko, Viktor V. Burdejnyj, Sergey V. Pavlenko	353
Scheduling Tests for 3D SoCs with Temperature Constraints Indira Rawat, Gupta M.K., Virendra Singh	356
Automated application mapping into Network-on-Chip topologies Bykov S. O.	360
MIMO Radar with Phase-coded waveforms Amirsadegh Roshanzamir, Bastani M. H.	363
BBN-based Approach For Assessment of Smart Grid And Nuclear Power Plant Interaction Eugene Brezhnev, Vyacheslav Kharchenko	367
Design, Test and Fault Detection in QCA 4-to-1 Multiplexer Zahra NajafiHaghi, Behjat Forouzandeh	374

The Evaluation of Statistical Characteristics of the Retransmission Meter Signal Frequency and Initial Phase on the Basis of VHDL-model Dmitry A. Velychko, Iegor I. Vdovychenko	378
A Research of Heuristic Optimization Approaches to the Test Set Compaction Procedure Based On a Decomposition Tree for Combinational Circuits Valentina Andreeva, Kirill A. Sorudeykin	382
Power Reduction of 7T Dual-Vt SRAM Cell Using Forward Body Biasing Sahba Sabetghadam Jahromi, Raziye Bounik	388
VLSI: An Investigation into Electromagnetic Signatures (EMS) for Non-Invasive Testing and Signal-integrity Verification Kadim HJ, Coulibaly L. M.	392
Secure Data over GSM based on Algebraic Codebooks Kazemi R., Nashtaali D., Boloursaz M., Behnia F.	397
Simulation of Telecommunication Channel Using Volterra Model Vitaliy D. Pavlenko, Viktor O. Speransky	401
Extracting Complete Set of Equations to Analyze VHDL-AMS Descriptions Arezoo Kamran, Vahid Janfaza, and Zainalabedin Navabi	405
A Data Modem for GSM Adaptive Multi Rate Voice Channel Boloursaz M., Hadavi A. H., Kazemi R., Behnia F.	409
Trends and prospects of development of techniques for extracting acoustic sounding information of the atmospheric boundary layer Klyuchnik I., Panchenko A., Umyarov R.	413
Decision-Making in Robotics and Adaptive Tasks Tsybmal A.M., Bronnikov A.I.	417
Design of Nonvolatile Memory Based on Magnetic Tunnel Junction for Special Electronic Systems Aleksandr Kostrov, Vladislav Nelayev, Viktor Stempitsky, Anatoly Belous, Arkady Turtsevich	421
Improving the Dependability of a Water Supply System via a Multi-Agent based CPS Teodora Sanislav, Liviu Miclea, Paolo Prinetto	425
Cyber Security Lifecycle and Assessment Technique for FPGA-based I&C Systems Illiashenko Oleg, Kharchenko Vyacheslav, Kovalenko Andriy	432
FPGA Technologies in Medical Equipment: Electrical Impedance Tomography Perepelitsyn Artem, Shulga Dmitry	437
A Trend-based Design Space Exploration of Multi-core Systems Using Regression Modeling Fazeleh Hajari Taheri, Omid Fatemi	441
Synchronous Rectifiers Enable High Efficiency for Buck-Boost Converter Yurii Shynkarenko and Igor Klyuchnyk	445

Test Data Compression Strategy While Using Hybrid-BIST methodology Elmira Karimi, Mohammad Hashem Haghbayan and Mahmood Tabandeh	449
Self-Adaptive Mobile Wireless Hotspot Zones Yanovsky M., Kharchenko V., Gorbenko A.	454
The Systolic Compositions of Two-dimensional and Multidimensional Lattice Filters for Space-Time Signal Processing David I. Lekhovyt'skiy, Andrii V. Semeniaka, and Dmytro S. Rachkov	458
Power Efficient Implementation of Homogenous Multi-Core Processors Aram Poghosyan	462
Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices Vladimir Hahanov, Karyna Mostova, Oleksandr Paschenko	465
Improved Scaling-Free CORDIC algorithm Leonid Moroz, Taras Mykytiv, Martyn Herasym	470
Coding Tangible Component of Transforms to Provide Accessibility and Integrity of Video Data Barannik V.V., Hahanova A.V., Krivonos V.N.	475
Review of the botnet detection techniques Oleg Savenko, Sergiy Lysenko, Kryshchuk Andrii	479
MEMS Intellect Multiprobes Contacting Devices for Electrical Checking-up of Multilayers Commutative Boards and BGA/CSP Electronic Components Nevliudov I.Sh., Palagin V.A., Razumov-Frizjuk E.A., Zharikova I.V.	483
Internet of Things: A Practical Implementation based on a Wireless Sensor Network Approach Michele Mercaldi, Andrea D'Oria, Davide Murru, Hai-Ning Liang, Ka Lok Man, Eng Gee Lim, Vladimir Hahanov, Mischenko Alexander	486
Investigation of EM Wave Propagation of the Wireless Capsule in Human Body Eng Gee Lim, Zhao Wang, Jin Hui Chen, Tammam Tillo, Ka Lok Man	490
Using pyroelectric detectors in the design of temperature measuring devices Bondarenko A.Yu., Klyuchnik I.I.	494
Transaction Level Model of Embedded Processor for Vector-Logical Analysis Irina V. Hahanova, Volodymyr Obrizan, Alexander Adamov, Dmitry Shcherbin	497
Embedded Intelligent Control Systems on the Basis of Elementary Fuzzy-Logic Cells Dontsova A., Vassiliev A.E.	502
Interconnection Analysis of the Integral Reliability Characteristics of the Monoergative Computer System and User's Competency Krivoulya G., Shkil A., Kucherenko D.	505
System approach to determination of ADC parameters Knyshev Ivan	511
Methodological Aspects of Complex Ecological Estimation of Man-Caused Territory State and Mathematical Modelling of Processes in a Environment System Kozulia T. V., Sharonova N. V. , Emelianova D. I., Kozulia M.M.	514

Method for “Failure on Demand” Latent Faults Diagnosis of NPP Safety Control Systems Gerasymenko K.E.	519
Informational Saturation of Noise Signals Kolodiy Z. A., Kolodiy A.Z.	523
The Positional Structural-Weight Coding of the Binary View of Transformants Barannik V., Krasnoruckiy A., Hahanova A.	525
Synchronization of a Fuzzy Automata Speranskiy Dmitriy	529
Models for SoC Infrastructure of Radio Frequency Identification with Code-Division Multiple Filippenko I.V., Hahanova I.V., Filippenko I.O, Maksimov M., Chugurov I.	535
Factorization of Rhythmograms Parametric Spectra on the Base of Multiplicative Linear Prediction Models Nataliia V. Kudriavtseva, Iryna O. Fil	538
Logi-Thermal Analysis of Digital Circuits Using Mixed-Signal Simulator Questa ADMS Petrosyants K.O., Rjabov N.I.	541
Method of Hybrid Regression Analysis in the Calibration Experiments Ordinartseva N. P.	545
Keynotes speeches and Invited Reports	548
AUTHORS INDEX	554

Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices

Vladimir Hahanov
KNURE, 61166, Ukraine,
Kharkiv, Lenin Ave. 14
+380 (57) 702-13-26
hahanov@knure.kharkov.ua

Karyna Mostova
KNURE, 61166, Ukraine,
Kharkiv, Lenin Ave. 14
+380 (57) 702-13-26
mostova@knure.kharkov.ua

Oleksandr Paschenko
KNURE, 61166, Ukraine,
Kharkiv, Lenin Ave. 14
+380 (57) 702-13-26
paschenko@knure.kharkov.ua

Abstract

In this paper HW/SW systems testing and faults diagnosing approach is described, also method for effective faults detection and defects localization within the system-under-test is proposed. Extended tree-view faults localization model; developed code-flow transaction graph.

1. Introduction

Essential increase of consumer requirements for complex electronic devices leads to substantial growth of complexity for HW and SW components, services, and system interfaces. Such tendency increases the importance to provide high quality for HW, SW, and networking components and services. Well known rule of ten for hardware components stating that fault detection cost increases in ten times on the next following design or manufacturing stages. The same rule is effectively applicable for Software design stages.

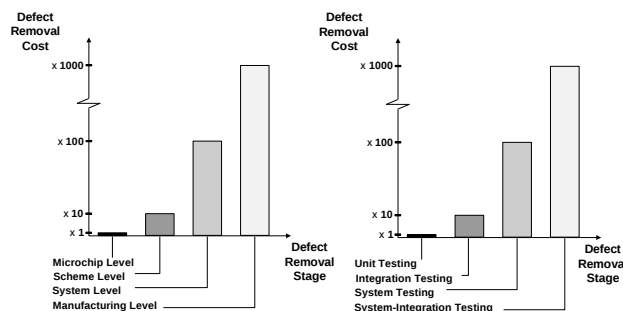


Figure 1. Defect removal cost vs. stage dependency for HW/SW development process

One of the main goals which comes to the foreground of industry is to decrease the cost of exploitation by creating the standardized infrastructures for maintenance which providing service exploitation, testing, disposal and, elimination of functional defects.

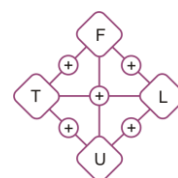
Nowadays fast growing complexities of hardware is transforming this rule into rule of twenty which makes even more important to detect the fault on early design stages, rather than on chip/PCB manufacturing, or system assembling stages [1].

Goal of this work is to develop method which increases product quality by means of developing sufficient HW/SW test and diagnosis approach, also decreasing faults detection and defects localization time in order to improve system performance on example of multimedia devices.

2. Components interconnection test model

In this thesis proposed model of tests generating, faults emulating, and defects localization based on xor-dependencies of four main components or characteristics of the system: $G=(F, U, T, L)$, where: F – functionality under test, U – unit under test, T – functional test, L – faults and defects coverage.

Such components of technical diagnosis are interconnected in the way, represented on the figure 2. Equations below represent complete set of interconnections which are forming the goal of technical diagnosis [2].



- 1) $T \oplus F \oplus L = 0$
- 2) $T \oplus L \oplus U = 0$
- 3) $T \oplus F \oplus U = 0$
- 4) $F \oplus L \oplus U = 0$

Figure 2. Technical diagnosis components interconnection schema

From equation $T \oplus F \oplus L = 0$ the next identities are following:

- 1) $T = F \oplus L$ - Tests generation, using the functionality model for the specified faults list.
- 2) $F = T \oplus L$ - Functionality model based on the specified test and the faults list.
- 3) $L = T \oplus F$ - Synthesis of the faults list of the specified functionality based on the specific test.

HW design effectiveness E can be defined by average and restricted integral criteria in the interval $[0,1]$. The result of test experiment – comparing outputs states of golden sample $f(A, B)$ and actual $f^*(A, B, L)$ – UUT with defects L of test combination A .

$$E = F(L, T, H) = \min\left[\frac{1}{3}(L + T + H)\right],$$

$$Y = (1 - P)^n; L = 1 - Y^{(1-k)} = 1 - (1 - P)^{n(1-k)};$$

$$T = [(1 - k) \times H^S] / (H^S + H^A); H = H^A / (H^S + H^A).$$

Above is described the level of product errors L , verification time T , SW/HW redundancy, defined by assertion mechanism and maintenance instruments H .

Level of production errors is characterized by Y – yield and depends on k – product testability, P – existing probability of the defect, and the number of not detected errors – n . Verification time is defined by product testability k multiplied by the structural HW/SW complexity and divided by general complexity of the product measured in SW code strings. HW/SW redundancy is dependant on assertions code complexity and other redundancies related to general code complexity. At the same time HW/SW redundancy should provide required level of functional defects diagnosis during yield's time to market defined by customer.

3. Multi-matrix processor of binary operations

Multi-matrix processor (MMP) is the minimal architecture of instructions targeted for parallel execution of single (and, or, xor, slc) operations with dedicated 2D array. Quantity of operation-related single arrays defines heterogeneous MMP of binary operations with buffer M [2]

Basing on MMP approach there was created infrastructure for UUT verification which is modification of I-IP standard 1500 [3, 4, 5]. On the figure 3 three process models for testing, faults

detection and diagnosis, performance recovering are presented.

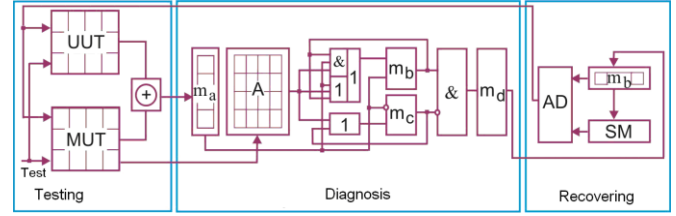


Figure 3. Testing, diagnosis, recovering process models

4. Method of Functional Defects

The analytic model verification based on temporal assertions is targeted for reaching required depth of diagnosis. The search of functional violation (FV) is based on xor-operation definition between the state of assertion (vector m) and the columns of FV table:

$$m \oplus (B_1 \vee B_2 \vee \dots \vee B_j \vee \dots \vee B_n)$$

$$B = \min_{j=1,n} [B_j = \sum_{i=1}^p (B_{ij} \oplus m_i)],$$

where

$$m = f(A, B) \oplus f^*(A, B, L).$$

5. Functional blocks tree view

For investigations it was chosen multimedia device-digital satellite receiver. During SW development and testing process all detected faults were classified in four main groups: 1) Issues detected during regression tests in core functionality; 2) Issues detected in additional features; 3) Issues detected during architectural verifications; 4) Issues detected while developing functionality on external interfaces. Results are presented in table 1.

Figure 4 represents functional blocks tree view hierarchy for digital satellite receiver. Schema represents the top list of the most occurring SW/HW faults and potential root-causes for specified faults. Chart represents 3-level hierarchy; however levels can be extended and decreased for better defect localization.

Majortiy of defects are related to architectural issues which should be planned to be tested in the first turn. At the same time majority of architectural issues are related to user interface.

Table 1. Number of detected issues per functionality

Functionality	Nº issues	% of issues
Core functionality		26.2
Signal modulation	56	3.400121433
Audio	4	0.242865817
Video	68	4.128718883
Frame	16	0.971463267
MPEG4	45	2.732240437
Memory	51	3.096539162
SW protection	57	3.460837887
Content CP	9	0.546448087
DISEQC	19	1.153612629
Dolby Digital	9	0.546448087
OTA SW download	27	1.639344262
Boot	39	2.367941712
Signal Loss / scan issues	32	1.942926533
Additional features		9.5
Timers	57	3.460837887
Reset	8	0.485731633
Subtitles	30	1.821493625
Locks	17	1.032179721
EPG	44	2.671523983
Architecture		45.4
User Interface	478	29.02246509
Application	145	8.803885853
Kernel	17	1.032179721
Boundary Issues	107	6.496660595
External Interfaces		18.9
USB	15	0.910746812
Sat Tuner	82	4.978749241
EHD	29	1.760777171
Ethernet	4	0.242865817
GPIO	3	0.182149362
HDMI/HDCEP	105	6.375227687
Homeplug	26	1.578627808
RCU	22	1.335761991
Modem	26	1.578627808
TOTAL	1647	100

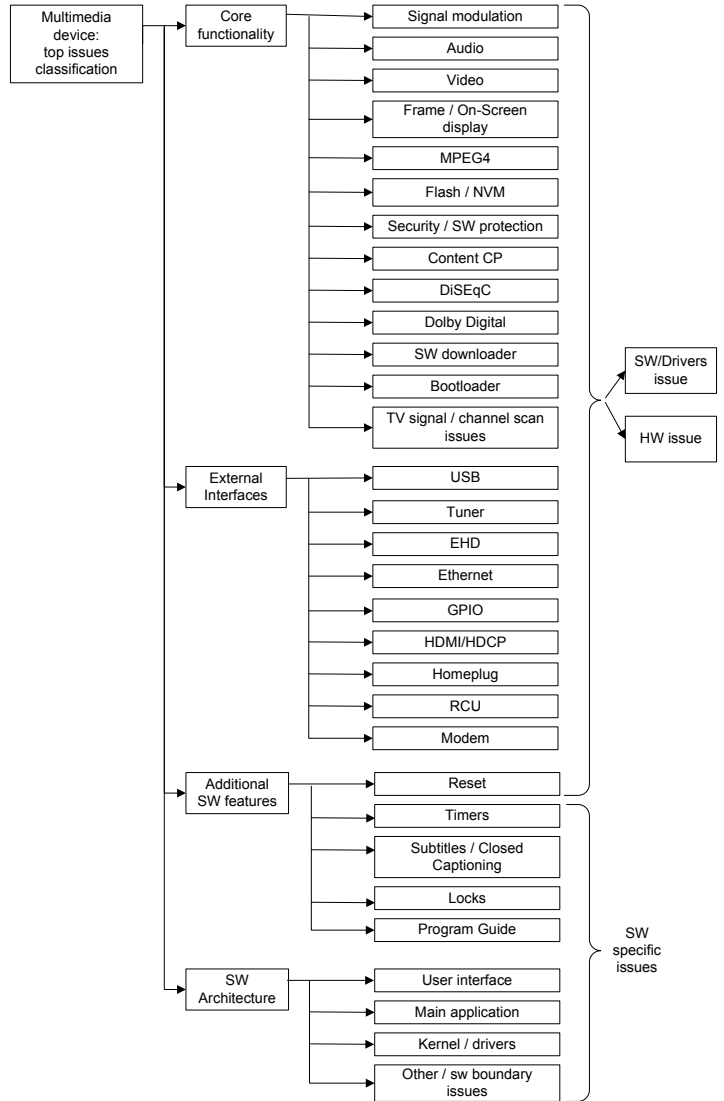


Figure 4. Digital satellite receiver tree-view hierarchy

6. Hierarchical testing process

Generic 3-level representation of tree view hierarchy is shown on the figure 5. Specific test sequence T_{ij} is applied to certain level of functional hierarchy. After testing is complete the result is being analyzed. If fault is detected, system returns block identifier B_{ij} with error description. Also there is considered false block automated reparation possibility R_{ij} . After fault detection and reparation the system should be retested from the very beginning [2, 6].

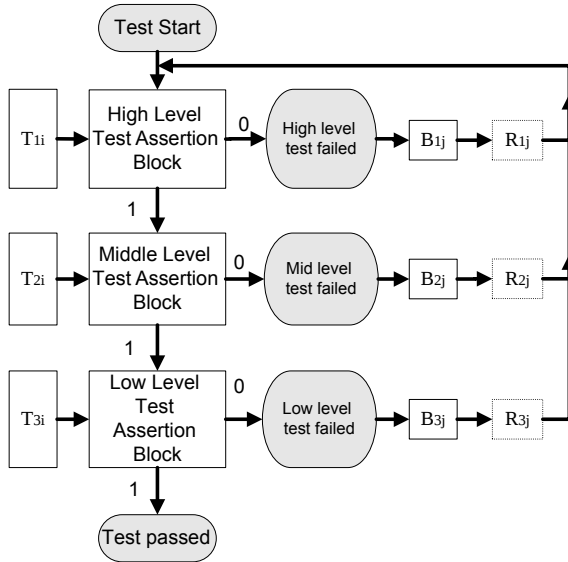


Figure 5. 3-level hierarchical testing process

7. Assertion based coverage graph

The analytic model verification, based on temporal assertions is targeted for reaching required depth of diagnosis and can be represented in the next way:

$$\begin{aligned}
 M &= f(F, A, B, S, T, L), & F &= (A * B) \times S; \quad S = f(T, B); \\
 A &= \{A_1, A_2, \dots, A_i, \dots, A_n\}; & B &= \{B_1, B_2, \dots, B_i, \dots, B_n\}; \\
 S &= \{S_1, S_2, \dots, S_i, \dots, S_m\}; & S_i &= \{S_{i1}, S_{i2}, \dots, S_{ij}, \dots, S_{ip}\}; \\
 T &= \{T_1, T_2, \dots, T_i, \dots, T_k\}; & L &= \{L_1, L_2, \dots, L_i, \dots, L_n\}.
 \end{aligned}$$

$F = (A * B) \times S$ is represented by code-flow transaction graph - CFTG, or Assertion-Based Coverage Graph – ABC graph.

$S = \{S_1, S_2, \dots, S_i, \dots, S_m\}$ - States of the HW/SW product while modeling test-segments.

Chart chords are represented by functional blocks B ,

where $B = (B_1, B_2, \dots, B_i, \dots, B_n)$, $\bigcup_{i=1}^n B_i = B$; $\bigcap_{i=1}^n B_i = \emptyset$;

A - assertion to verify block B .

State $S_i = f(T, B_i)$ influences test sequence T .

Assertions Monitor $A(S_i) = A_{i1} \vee A_{i2} \vee \dots \vee A_{in}$

Defect blocks multitude list: $L = \{L_1, L_2, \dots, L_n\}$.

For the functional block diagram (figure 4), the functional defects matrix is presented in Table 2 which covers all hierarchical (or activation) levels.

Below there are presented the requirements for functional defects table definition:

1. The number of tests $|T| \rightarrow \min$,
2. $|T_{\text{new}}| = |T| + t$, defects vector is unique
3. Diagnosability function should always tend to 1 [2, 3].

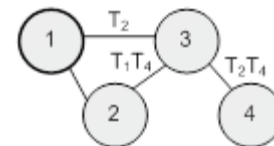
$$D = 1 \rightarrow \frac{|T| \times |A|}{|\log_2 N|} = 1 \rightarrow |\log_2 N| = |T| \times |A|$$

Basing on diagnosing procedure and the matrix of functional defects faulty components can be defined by analyzing functional defects table rows. For the functional defects matrix the next transaction graphs can be created, represented on the figure 6.

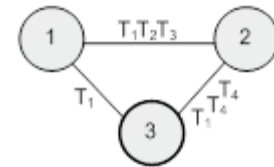
Table 2. Matrix of functional defects

Activation Levels														
1 st						2 nd					3 rd			
1 st level tests	Core Functionality	Extended interfaces	Additional features	SW Architecture	V	2nd level tests	USB	Tuner	Ethernet	V	3rd level tests	Hardware	Software	V
T ₁	.	1	1	.	0	T ₁	1	1	1	1	T ₁	1	.	0
T ₂	1	.	1	1	1	T ₂	1	1	.	0	T ₂	1	1	1
T ₃	1	1	.	.	1	T ₃	1	1	.	0	T ₃	.	1	1
T ₄	.	1	1	1	0	T ₄	.	1	1	1				
						T ₅	.	1	1	1				

1st activation level graph:



2nd activation level graph:



3rd activation level graph:

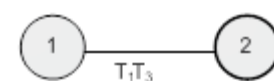


Figure 6. Code-flow transaction graph

8. Multi-level model for diagnosing digital systems

Multi-level model can be presented in a tree-like view B , where every vertex can be represented as a 3-dimensional functional modules activation table and arcs are representing navigation to lower diagnosis levels for the cases when functional block's defect was detected:

$$B = [B_{ij}^{rs}], \text{card} B = \sum_{r=1}^n \sum_{s=1}^{m_r} \sum_{j=1}^{k_{rs}} B_{ij}^{rs},$$

where n – number of multi-tree levels; m_r – number of the functional blocks and components on r level; k_{rs} – number of components in the B^{rs} table; $B_{ij}^{rs} = \{0,1\}$ – activation table component which is defined by the test vector T_{i-A_i} applicable to the monitor A_i .

Multi tree-like model is described on the figure 7.

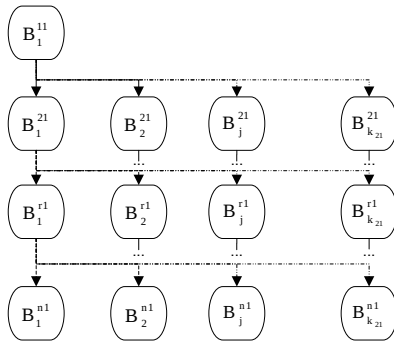


Figure 7. Multi tree-like model

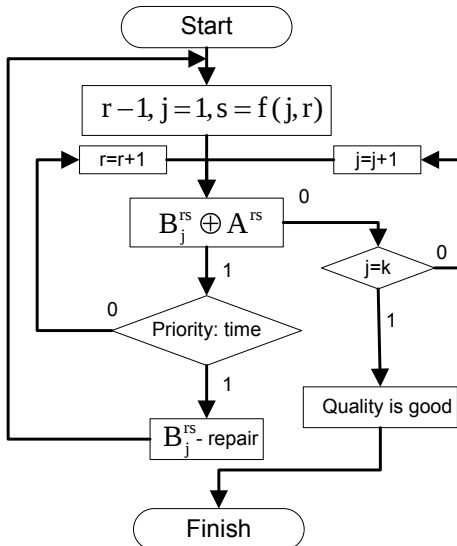


Figure 8. Multi-tree navigation algorithm

Defects detection model is based on top-to-bottom navigation to the required detailing level:

$$B_j^{rs} \oplus A^{rs} = \begin{cases} 1 \rightarrow \{B_j^{r+1,s}, R\}; \\ 0 \rightarrow \{B_j^{r+1,s}, G\}. \end{cases}$$

Detailed diagnosis algorithm for multi-tree navigation is presented on the figure 8.

9. Conclusions

This paper represents faults detection and localization technique. Described models and algorithms providing possibility to perform effective service for complex digital SW/HW systems.

Benefit for such approach is in simplicity of technical information representation and diagnosing preparation, based on minimized activation table applied to HW/SW system-under-test and in particular to functional blocks segments testing which are invariant to hierarchy levels.

10. References

- [1] Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital Memory and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers, NY, 2002, 713p.
- [2] V.I.Hahanov, I.V.Hahanova, Ye.I.Litvinova, O.A.Guz. *Digital SoCs design and verification.*– Kharkov: Novoye Slovo.– 2010.– 528p.
- [3] M.F.Bondarenko, O.A.Guz, V.I.Hahanov, Yu.P.Shabanov-Kushnarenko, *Brain-like computing processes*, Kharkov: Novoye Slovo, 2010, 160p.
- [4] V.Hahanov, S.Chumachenko, C.U.Ngene, Y.Ticoura, "Brain-like Computer Structures", *Radio Electronics and Informatics*, Kharkov, 2009, №4, pp. 30-40.
- [5] Marinissen E.J., Yervant Zorian, Guest Editors' Introduction: The Status of IEEE Std 1500, *IEEE Design & Test of Computers*, 2009, No26(1). pp.6-7.
- [6] V.Hahanov, *Technical diagnosis of digital and microprocessor structures*, Kharkov, 1995, 242p.

Camera-ready was prepared in Kharkov National University of Radio Electronics
Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 27.08.2012. Format 60×84¹/₈.

Relative printer's sheets: 49. Circulation: 200 copies.

Published by SPD FL Stepanov V.V.

Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозіуму «Схід-Захід Проектування та Діагностування – 2012»
Макет підготовлено у Харківському національному університеті радіоелектроніки

Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова

Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 27.08.2012. Формат 60×84¹/₈.

Умов. друк. Арк. 49. Тираж: 200 прим.

Видано: СПД ФЛ Степанов В.В.

Вул. Ак. Павлова, 311, Харків, 61168, Україна