KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012)

Technically Co-Sponsored by

Kharkov, Ukraine, September 14 – 17, 2012

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10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Trades Committee of Kharkov National University of Radioelectronics and Trades Committee of Students, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University.

CONTENTS

Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices

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Abstract

In this paper HW/SW systems testing and faults diagnosing approach is described, also method for effective faults detection and defects localization within the system-under-test is proposed. Extended tree-view faults localization model; developed code-flow transaction graph.

1. Introduction

Essential increase of consumer requirements for complex electronic devices leads to substantial growth of complexity for HW and SW components, services, and system interfaces. Such tendency increases the importance to provide high quality for HW, SW, and networking components and services. Well known rule of ten for hardware components stating that fault detection cost increases in ten times on the next following design or manufacturing stages. The same rule is effectively applicable for Software design stages.

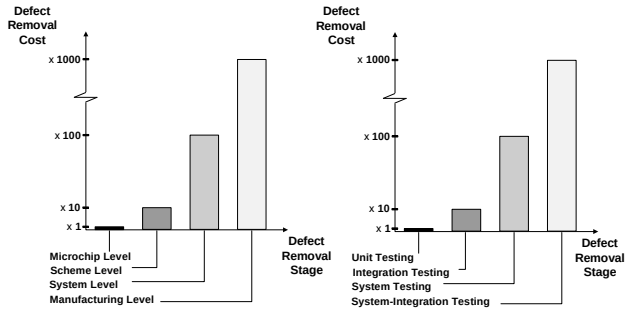


Figure 1. Defect removal cost vs. stage dependency for HW/SW development process

One of the main goals which comes to the foreground of industry is to decrease the cost of exploitation by creating the standardized infrastructures for maintenance which providing service exploitation, testing, disposal and, elimination of functional defects.

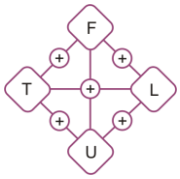
Nowadays fast growing complexities of hardware is transforming this rule into rule of twenty which makes even more important to detect the fault on early design stages, rather then on chip/PCB manufacturing, or system assembling stages [1].

Goal of this work is to develop method which increases product quality by means of developing sufficient HW/SW test and diagnosis approach, also decreasing faults detection and defects localization time in order to improve system performance on example of multimedia devices.

2. Components interconnection test model

In this thesis proposed model of tests generating, faults emulating, and defects localization based on xor-dependencies of four main components or characteristics of the system: G=(F, U, T, L), where: F – functionality under test, U – unit under test, T – functional test, L – faults and defects coverage.

Such components of technical diagnosis are interconnected in the way, represented on the figure 2. Equations below represent complete set of interconnections which are forming the goal of technical diagnosis [2].



1) $T \oplus F \oplus L = 0$
2) $T \oplus L \oplus U = 0$
3) $T \oplus F \oplus U = 0$
4) $F \oplus L \oplus U = 0$

Figure 2. Technical diagnosis components interconnection schema

From equation $T \oplus F \oplus L = 0$ the next identities are following:

1) $T = F \oplus L$ - Tests generation, using the functionality model for the specified faults list.

2) $F = T \oplus L$ - Functionality model based on the specified test and the faults list.

3) $L = T \oplus F$ - Synthesis of the faults list of the specified functionality based on the specific test.

HW design effectiveness E can be defined by average and restricted integral criteria in the interval [0,1]. The result of test experiment – comparing outputs states of golden sample $f(A, B)$ and actual $f^*(A, B, L)$ – UUT with defects L of test combination A.

$$E = F(L, T, H) = \min[\frac{1}{3}(L + T + H)],$$

$$Y = (1 - P)^n; \; L = 1 - Y^{(1-k)} = 1 - (1 - P)^{n(1-k)};$$

$$T = [(1 - k) \times H^s] / (H^s + H^a); \; H = H^a / (H^s + H^a).$$

Above is described the level of product errors L, verification time T, SW/HW redundancy, defined by assertion mechanism and maintenance instruments H.

Level of production errors is characterized by Y – yield and depends on k – product testability, P – existing probability of the defect, and the number of not detected errors – n. Verification time is defined by product testability k multiplied by the structural HW/SW complexity and divided by general complexity of the product measured in SW code strings. HW/SW redundancy is dependant on assertions code complexity and other redundancies related to general code complexity. At the same time HW/SW redundancy should provide required level of functional defects diagnosis during yield's time to market defined by customer.

3. Multi-matrix processor of binary operations

Multi-matrix processor (MMP) is the minimal architecture of instructions targeted for parallel execution of single (and, or, xor, slc) operations with dedicated 2D array. Quantity of operation-related single arrays defines heterogeneous MMP of binary operations with buffer M [2]

Basing on MMP approach there was created infrastructure for UUT verification which is modification of I-IP standard 1500 [3, 4, 5]. On the figure 3 three process models for testing, faults detection and diagnosis, performance recovering are presented.

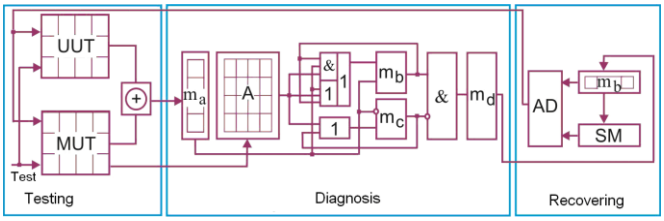


Figure 3. Testing, diagnosis, recovering process models

4. Method of Functional Defects

The analytic model verification based on temporal assertions is targeted for reaching required depth of diagnosis. The search of functional violation (FV) is based on xor-operation definition between the state of assertion (vector m) and the columns of FV table:

$$m \oplus (B_1 \vee B_2 \vee ... \vee B_j \vee ... \vee B_n).$$

$$B = \min_{j=1,n} [B_j = \sum_{i=1}^{p} (B_{ij} \oplus_{i=1}^{p} m_i)],$$

where

$$m = f(A, B) \oplus f^*(A, B, L).$$

5. Functional blocks tree view

For investigations it was chosen multimedia device-digital satellite receiver. During SW development and testing process all detected faults were classified in four main groups: 1) Issues detected during regression tests in core functionality; 2) Issues detected in additional features; 3) Issues detected during architectural verifications; 4) Issues detected while developing functionality on external interfaces. Results are presented in table 1.

Figure 4 represents functional blocks tree view hierarchy for digital satellite receiver. Schema represents the top list of the most occurring SW/HW faults and potential root-causes for specified faults. Chart represents 3-level hierarchy; however levels can be extended and decreased for better defect localization.

Majortiy of defects are related to architectural issues which should be planned to be tested in the first turn. At the same time majority of architectural issues are related to user interface.

Table 1. Number of detected issues per functionality

Functionality	№ issues	% of issues
Core functionality		**26.2**
Signal modulation	56	3.400121433
Audio	4	0.242865817
Video	68	4.128718883
Frame	16	0.971463267
MPEG4	45	2.732240437
Memory	51	3.096539162
SW protection	57	3.460837887
Content CP	9	0.546448087
DISEQC	19	1.153612629
Dolby Digital	9	0.546448087
OTA SW download	27	1.639344262
Boot	39	2.367941712
Signal Loss / scan issues	32	1.942926533
Additional features		**9.5**
Timers	57	3.460837887
Reset	8	0.485731633
Subtitles	30	1.821493625
Locks	17	1.032179721
EPG	44	2.671523983
Architecture		**45.4**
User Interface	478	29.02246509
Application	145	8.803885853
Kernel	17	1.032179721
Boundary Issues	107	6.496660595
External Interfaces		**18.9**
USB	15	0.910746812
Sat Tuner	82	4.978749241
EHD	29	1.760777171
Ethernet	4	0.242865817
GPIO	3	0.182149362
HDMI/HDCP	105	6.375227687
Homeplug	26	1.578627808
RCU	22	1.335761991
Modem	26	1.578627808
TOTAL	**1647**	**100**

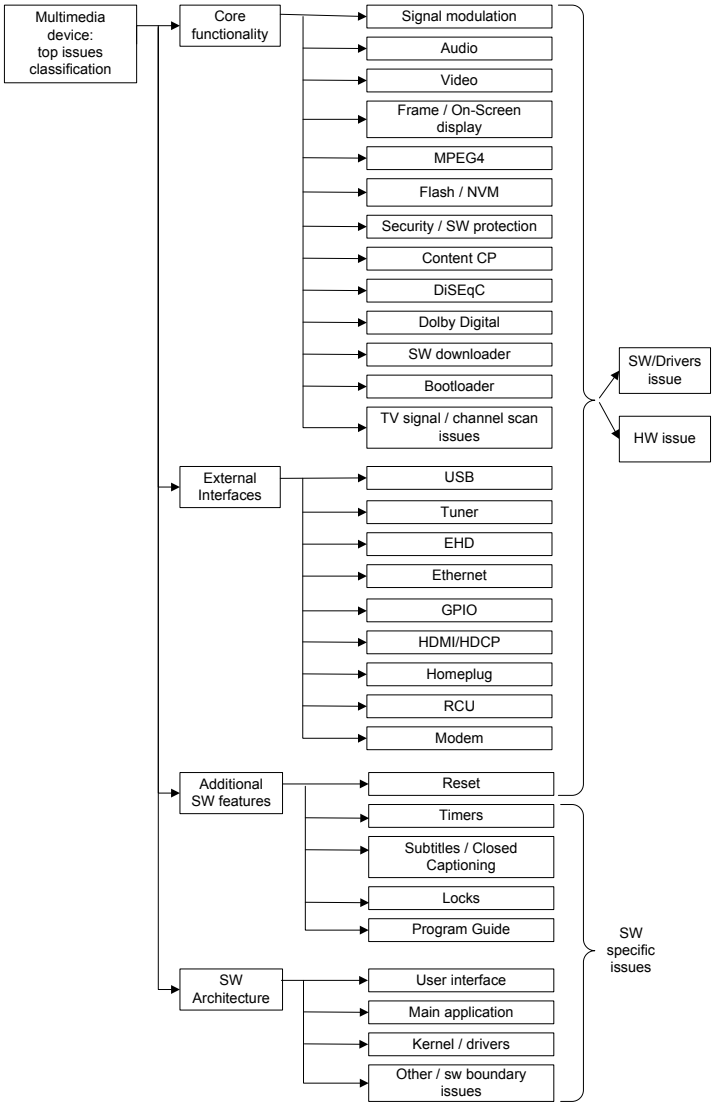


Figure 4. Digital satellite receiver tree-view hierarchy

6. Hierarchical testing process

Generic 3-level representation of tree view hierarchy is shown on the figure 5. Specific test sequence T_{ij} is applied to certain level of functional hierarchy. After testing is complete the result is being analyzed. If fault is detected, system returns block identifier B_{ij} with error description. Also there is considered false block automated reparation possibility R_{ij}. After fault detection and reparation the system should be retested from the very beginning [2, 6].

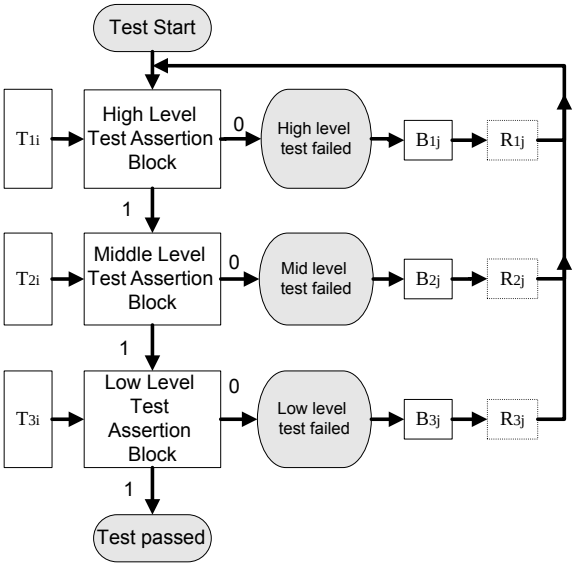


Figure 5. 3-level hierarchical testing process

7. Assertion based coverage graph

The analytic model verification, based on temporal assertions is targeted for reaching required depth of diagnosis and can be represented in the next way:

$M = f(F, A, B, S, T, L)$, $F=(A*B)\times S$; $S=f(T,B)$;

$A=\{A_1, A_2, ..., A_i, ..., A_n\}$; $B=\{B_1, B_2, ..., B_i, ..., B_n\}$;

$S=\{S_1, S_2, ..., S_i, ..., S_m\}$; $S_i=\{S_{i1}, S_{i2}, ..., S_{ij}, ..., S_{ip}\}$;

$T=\{T_1, T_2, ..., T_i, ..., T_k\}$; $L=\{L_1, L_2, ..., L_i, ..., L_n\}$.

$F = (A*B)\times S$ is represented by code-flow transaction graph - CFTG, or Assertion-Based Coverage Graph – ABC graph.

$S = \{S_1, S_2, ..., S_i, ..., S_m\}$ - States of the HW/SW product while modeling test-segments.

Chart chords are represented by functional blocks B, where $B = (B_1, B_2, ..., B_i, ..., B_n)$, $\bigcup_{i=1}^{n} B_i = B$; $\bigcap_{i=1}^{n} B_i = \varnothing$;

A - assertion to verify block B.

State $S_i = f(T, B_i)$ influences test sequence T.

Assertions Monitor $A(S_i) = A_{i1} \vee A_{i2} \vee ... \vee A_{in}$

Defect blocks multitude list: $L = \{L_1, L_2, ..., L_n\}$.

For the functional block diagram (figure 4), the functional defects matrix is presented in Table 2 which covers all hierarchical (or activation) levels.

Below there are presented the requirements for functional defects table definition:

1. The number of tests |T| -> min,
2. $|T_{new}|=|T|+t$, defects vector is unique
3. Diagnosability function should always tend to 1 [2, 3].

$$D = 1 \rightarrow \frac{|T|\times|A|}{]\log_2 N[} = 1 \rightarrow]\log_2 N[= |T|\times|A|$$

Basing on diagnosing procedure and the matrix of functional defects faulty components can be defined by analyzing functional defects table rows. For the functional defects matrix the next transaction graphs can be created, represented on the figure 6.

Table 2. Matrix of functional defects

Activation Levels														
1st						2nd					3rd			
1st level tests	Core Functionality	Extended interfaces	Additional features	SW Architecture	V	2nd level tests	USB	Tuner	Ethernet	V	3rd level tests	Hardware	Software	V
T_1	.	1	1	.	0	T_1	1	1	1	1	T_1	1	.	0
T_2	1	.	1	1	1	T_2	1	1	.	0	T_2	1	1	1
T_3	1	1	.	.	1	T_3	1	1	.	0	T_3	.	1	1
T_4	.	1	1	1	0	T_4	.	1	1	1				
						T_5	.	1	1	1				

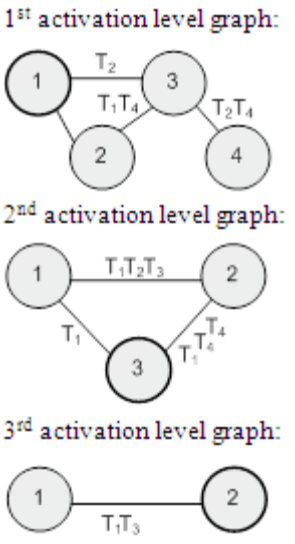


Figure 6. **Code-flow transaction graph**

8. Multi-level model for diagnosing digital systems

Multi-level model can be presented in a tree-like view B, where every vertex can be represented as a 3-dimentional functional modules activation table and arcs are representing navigation to lower diagnosis levels for the cases when functional block's defect was detected:

$$B = [B_{ij}^{rs}], cardB = \sum_{r=1}^{n} \sum_{s=1}^{m_r} \sum_{j=1}^{k_{rs}} B_{ij}^{rs},$$

where n – number of multi-tree levels; m_r - number of the functional blocks and components on r level; krs - number of components in the B^{rs} table; B_{ij}^{rs} = {0,1} - activation table component which is defined by the test vector T_{i-A_i} applicable to the monitor A_i.

Multi tree-like model is described on the figure 7.

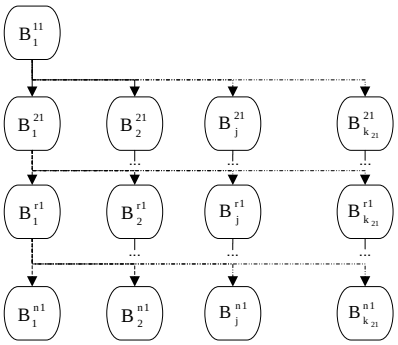


Figure 7. Multi tree-like model

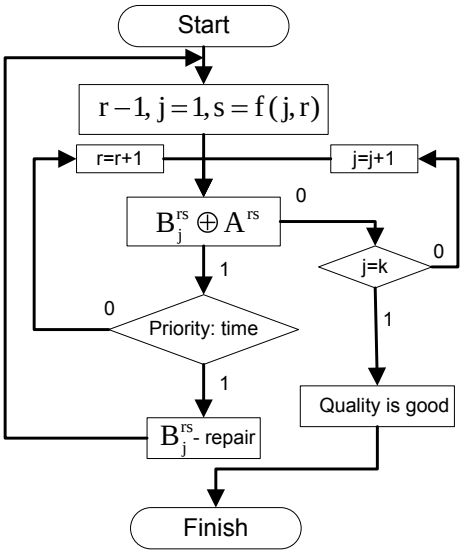


Figure 8. Multi-tree navigation algorithm

Defects detection model is based on top-to-bottom navigation to the required detailing level:

$$B_j^{rs} \oplus A^{rs} = \begin{cases} 1 \rightarrow \{B_j^{r+1,s}, R\}; \\ 0 \rightarrow \{B_j^{r+1,s}, G\}. \end{cases}$$

Detailed diagnosis algorithm for multi-tree navigation is presented on the figure 8.

9. Conclusions

This paper represents faults detection and localization technique. Described models and algorithms providing possibility to perform effective service for complex digital SW/HW systems.

Benefit for such approach is in simplicity of technical information representation and diagnosing preparation, based on minimized activation table applied to HW/SW system-under-test and in particular to functional blocks segments testing which are invariant to hierarchy levels.

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Camera-ready was prepared in Kharkov National University of Radio Electronics
Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 27.08.2012. Format 60×841/8.
Relative printer's sheets: 49. Circulation: 200 copies.
Published by SPD FL Stepanov V.V.
Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозіуму «Схід-Захід Проектування та Діагностування – 2012»
Макет підготовлено у Харківському національному університеті радіоелектроніки
Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова
Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 27.08.2012. Формат 60×84$^{1}/_{8}$.
Умов. друк. Арк. 49. Тираж: 200 прим.
Видано: СПД ФЛ Степанов В.В.
Вул. Ак. Павлова, 311, Харків, 61168, Україна