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HARDWARE ASIST VERIFICATION

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Abstract. The rapid development of semiconductor technology is driven by four complex elements: software, hardware, interface, and architecture. As modern chips integrate billions of transistors, support heterogeneous computing, and perform increasingly software-defined workloads, ensuring their functionality has never been more challenging. Modern systems use complex software stacks, requiring early software validation along with hardware verification. HAV platforms allow for pre-silicon software creation through FPGA-based emulation and prototyping.

Keywords: AI, high-performance computing, SoC, RTL, FPGA.

Introduction. The semiconductor industry is experiencing an unprecedented shift toward artificial intelligence, driven by the ever-increasing demand for computing power, autonomous systems, and next-generation architectures. As a result, the complexity of silicon components and the software content in systems and products continue to grow exponentially.

Manufacturers and their suppliers are redesigning system-level components using new electrical/electronic (EE) architectures that help create new quality. This trend is spreading to other markets such as industrial automation, high-performance computing (HPC) data centres, and aerospace, where software-defined systems are delivering massive computing power both at the edge (smartphones, cars, and cameras) and in the core data centre.

Compounding complexities – spanning software, hardware, interfaces, and workload-optimized architectures – are creating tremendous challenges for those developing today’s most advanced chip, system on chip (SoC), and multi-die designs. Verification and software development processes, in particular, can require quadrillions of test and validation cycles across simulation, emulation, and prototyping stages. As a result, there has been a distinct need for faster HAV solutions that accelerate the development and validation of advanced chip designs and help ensure optimized functionality of the software-defined systems they enable.

As artificial intelligence now impacts nearly every aspect of modern technology, chip designers face new challenges to ensure their products meet performance expectations and operate reliably and efficiently under increasing computational demands. These changes are pushing the boundaries of traditional design and verification methodologies, creating a need for innovative solutions for today's integrated circuit architectures and industrial systems.

To understand the complexity of modern integrated circuit design, it is important to consider each step of the process, starting with the fundamental

using a hybrid approach using both on-premises and cloud resources. The key to effective verification is to seamlessly transition between different use cases, from rapid early-stage RTL debugging to high-throughput validation of software workloads. HAV platforms that are configurable and can effectively handle this spectrum are essential for validating the real-world complexities of chip and system design that require real-world workloads.

HAV Hardware Justification

Designing AI accelerator chips is incredibly complex. Modern chips contain billions of transistors and multiple processors (CPUs, NPUs, GPUs, etc.) that work in parallel. Verifying this complexity with traditional simulation is challenging, not only for functional correctness, but also to ensure power efficiency and performance targets under real-world workloads.

New AI accelerators typically use workload-specific optimizations (e.g., high-precision arithmetic, new data streams), which require extensive architectural validation. The sheer scale of the operations (often quadrillions of cycles for a full validation) makes software simulation alone impractical.

Software stacks (drivers, AI frameworks) are complex, so hardware validation must now include early software preparation and collaborative validation. Finally, high-speed memory and I/O interfaces (HBM, PCIe, etc.) add another layer of complexity and must be tested at real-world speeds to avoid bottlenecks. In short, AI accelerators go beyond traditional methods in terms of scale, speed, and scalability.

Implementing HAV systems provides several tangible benefits for advanced chips in general and AI accelerator projects in particular:

- **Faster verification cycles:** Hardware emulation and prototyping can speed up verification throughput by orders of magnitude. Tests that take days or weeks in traditional software simulation can be completed on an FPGA-based emulator in a matter of hours.

- **Early software preparation and validation:** Software teams need to develop and test firmware, drivers, and AI models long before silicon becomes available. With HAV, developers can boot an operating system on an emulated accelerator or use an FPGA prototype to run real-world AI workloads against the design. This early, joint verification of software and hardware means that by the time the silicon arrives, the hardware and software are verified together, reducing integration issues. Parallel development of software and silicon can significantly accelerate time to market and build design confidence.

- **Higher level of verification and accuracy:** HAV allows for a much higher number of cycles and more complex scenarios to be run than traditional simulation. Engineers can test more corner cases, longer sequences, and full application workloads to uncover bugs that short simulations might miss. The result is a more thoroughly verified design with fewer hidden bugs, which directly reduces the risk of catastrophic silicon failures. In addition, emulators

have RTL-level cycle accuracy, so the behavior closely matches the actual silicon, increasing the accuracy of verification results.

- Performance bottleneck detection: The actual throughput of an AI accelerator can only be estimated by running near-real-time workloads on prototypes. This feedback can lead to design adjustments (such as adjusting buffer sizes or scheduling algorithms) before going to film. Power consumption can also be monitored so the team can ensure that the chip meets energy efficiency goals.

- Reduced risk of silicon reflow: Risk reduction is perhaps the most important benefit of HAV. Hardware-based solutions significantly reduce the likelihood of a critical silicon defect by identifying functional errors, integration issues, or performance issues during pre-silicon validation.

- Reduced time to market: These factors—faster validation, concurrent software development, and avoidance of rework—combine to shorten the overall development cycle. A well-validated chip can confidently go into production, and the software can be ready to deploy on real hardware when the chip returns from the factory, giving companies a competitive advantage in the rapidly evolving AI market.

The HAPS series of test systems developed by Synopsys are primarily used for FPGA-based prototyping.

Summary

HAV has become indispensable for AI accelerator development teams. It solves the critical challenges of validating incredibly complex, high-performance chips in realistic environments. By using solutions like the Synopsys HAV portfolio, teams can achieve greater confidence in their designs, meet high performance/power targets, and avoid costly errors—all while accelerating the overall development cycle.

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