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Design of real-time system logic control on FPGA

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Abstract— Problems of real-time hardware logic control systems design on the FPGA are considered. The control algorithm is implemented based on a timed FSM model, represented by a temporal state diagram. The design of the control device model using hardware description language VHDL in the form of the three-process pattern is made. The functional verification of the model was carried out using Active-HDL tools, the synthesis of the circuit was carried out on the Spartan 3E FPGA technology platform using Xilinx ISE CAD tools. The hardware costs for the circuit implementation of the control device were analyzed.

Keywords— timed FSM, temporal state diagram, VHDL, functional verification, pattern, FPGA.

I. INTRODUCTION

Among the entire set of control systems, the significant part are logical control systems, in which control signals take values of the logical zero or one, depending on boundary values of physical quantities that define these parameters. For the technical implementation of these systems, the Finite State Machine (FSM) is the most suitable, and the visual representation of functioning algorithm is a state diagram. The distinctive feature of the FSM for logic control is that among input values there are not only announcing signals of the operational state machine, but also external, towards to the controlled system, events of external world, which are playing role of interrupts for the control algorithm.

A control FSM functions in machine time, is determined by the operation time of machine. But the most of real logical control systems cooperate with external world in the metric time, i.e. they are real-time systems.

The real-time control system is a system in which the resultant action (activity) depends not only on logical values of simple control actions, but also on time during which these actions are performed. The main difference between tasks in real time and tasks that are not dependent on time is that tasks in real-time systems must be completed within a specified

period of time, that allow to complete processing of data correctly. For their implementation, it is customary to use a timed FSM model, which allows taking into account the effect of metric time on transitions between technical states of control system.

Any local digital device that implements an information processing or control algorithm can be implemented in two ways: hardware or software-hardware. With hardware implementation method, a given algorithm is described in hardware description language (HDL) and is synthesized by instrumental tools of computer-aided design (CAD) in FPGA (Field-Programmable Gate Array circuit). The advantage of this approach is hardware flexibility (ability to implement any algorithm) and a sufficiently large speed.

During describing the functioning algorithm for digital logical control devices in CAD systems, one of code styles is the style of automata-based programming. In automata-based programming, a concept of "state" is used as the base one [1]. A state is a mathematical abstraction that is uniquely associated to each of physical states of a control object, since usually an operation of technical systems is shown through a change of their states. At the same time, each state in a control algorithm maintains a control object in a proper state, and the transition to a new state in an algorithm leads to the transition of an object to a new corresponding state, which ensures the process of object' logical control. A state is a set of parameters of a technical system at a given moment of time. A current state carries all information about the history of a system, which is necessary to determine its response to any input action that is formed at a given time.

Thus, the task of developing an unified pattern in the hardware description language for the design of real-time logic control devices, which based on FSM in the style of automata-based programming, becomes urgent. The goal of this work is to develop a pattern for describing finite state

machine in the hardware description language VHDL, and automated synthesis of the received model with.

II. THE MODEL OF STRUCTURAL FSM IN REAL-TIME SYSTEMS

When describing a behavior of real-time control systems, it is necessary to take into account timing aspects of their behavior. For this, a state machine model is expanded by introducing a timed variable, and the concept of a timed FSM [2, 3] is introduced. A timed variable constantly increases its value and "resets" to 0 upon the arrival of an input signal and a FSM transitions to a new state. Time variables are measured in automata cycles.

As a rule, three parameters are used to describe timing aspects in the automata-based model: timing constraints t_c , (input) timeouts t_{io} and output delays t_d , which sometimes are called as output timeouts. An input timeout determines the maximum waiting time for input effects (events) for each state of a FSM. If an input symbol was not filed before the end of a timeout, a state machine starts polling input variables and can switch to another state. Time constraints are intervals on transitions that limit the time during which the transition can be performed. Output delays (output timeouts) shows the time that a state machine spends on executing of a transition, i.e. an output signal will appear at an output after a time interval, which is determined by the output delay.

In logical control systems, a concept of "input values" is divided into input actions and events. Input actions are implemented automatically by polling in accordance with an algorithm of its operation in a control loop, and events are implemented instantaneously and lead to a change in a state of the state machine.

Event processing in real-time systems, as a rule, are determined on a basis of dynamic characteristics of control processes and related events. An event is an abstract concept, implying such a change in environmental conditions, which generates a certain reaction of a system [4]. Events can be generated both by an external environment and within a control system by its components.

There are three main options for an interaction of a control FSM with an external environment.

1. Events are used for an interaction of a control and operating FSM within an automatic control system. In this case, if events are exceptional (two events cannot occur simultaneously), events' processing doesn't differ from processing of input variables values of a FSM.

2. Events along with input variables provide an interaction of a FSM with an external environment. This design solution should reflect the difference between events and input variables: a FSM processes events at the moment of its occurrence, while values of input variables are polled by a FSM on its own initiative.

3. An each event is associated with a separate state (transition) of a FSM. This solution is only suitable for implementing of an exceptional event model. In addition, it reflects an active role of events, and the fact that the occurrence of events, by itself, initiates an operation of a FSM. This solution is the best coordinated with traditional event systems, where any output function is related to the content of events.

Depending on a purpose and features of using models of a timed FSM, there are many modifications of such models, which differently take into account both, the method of events' processing and the way of delays' accounting in states of a FSM [5, 6].

Based on functioning features of logic control systems, a full model of a structural timed FSM can be represented by a nine $W = (X, Y, Z, f, g, z_0, T_c, T_{io}, T_d)$, where: $X = \{X_C, X_E\}$ – a set of input variables, X_C – a set of announcing signals from a control object, X_E – a set of external events; $Y = \{Y_C, Y_F\}$ – a set of output variables, Y_C – a set of reactions (control signals), Y_F – a set of activities (output functions); Z – a set of internal variables that determine coding states of a FSM; f – a transition function, g – an output function; z_0 – a code of the initial state of a FSM; $T_c = \{t_{c1}, t_{c2} \dots t_{cp}\}$ – a set of timed variables for timing restrictions on each arc of a state diagram, where p – is a number of arcs in a state diagram, $t_{ci} = \{1, k\}$, k – a maximum number of clocks' restrictions on transitions to the i -th node of a state diagram in polling mode, $k = \{1, \infty\}$, ∞ – responds exclusively by an effective transition function, $T_{io} = \{t_{io1}, t_{io2} \dots t_{ion}\}$ – a set of timed variables for timeouts (expected) of each state of a FSM, $t_{ioi} = \{1, n\}$ – timeout for each state, n – a number of states of a FSM; $T_d = \{t_{d1}, t_{d2} \dots t_{dm}\}$ – is a set of delays for the realization of the corresponding output signal, where m – is a number of output variables, $t_{dm} = \{1, l\}$, where l – is a maximum number of clock cycles for the realization of output functions in the specified state of a FSM.

In general, a timed FSM can contain all three time parameters, but for a specific task timed FSM with one or two of specified parameters can be used.

A classical model of timed FSM, which consist of three timing parameters $\langle t_c, t_{io}, t_d \rangle$ can't be directly attributed to the traditional Moore model. The output function is similar to Moore FSM, but the output signal is formed after delay, and not when the FSM transits to a new state. A time of appearance (change) of output signals is connected to a working edge of the synchronization signal. In the proposed model of the timed FSM, the logic of its operation is as follows.

During FSM transitions to the current state a_i , the main time parameter $t_{io}(a_i)$ (timeout) is determined for it, that is, a time during which a FSM should be in the current state if an external event will not transfer the FSM into another state ahead of time. Value of t_{io} is defined in FSM cycles. After the time t_{io} is expired, a FSM responds to input signals (polls them) and transfers to a next state. Output signals of a FSM in the current state a_i appear at outputs of the FSM at the time determined by $t_{dj}(a_i)$ (output delays), that is, output delays for signals y_j in the state a_i . For each of output signals y_j , the initial delay is determined in FSM cycles and can be different. When $y_j = 0$, timed FSM approaches the classical Moore model.

A processing of external events is as follows. For each state a_i , the time constraints $t_c(a_i)$ (input constraints) are set,


```

-- clk synchronization
process (Clk, Reset)
begin
if Reset = '1' then count <= (others => '0');
elsif rising_edge(Clk) then
if State /= next_state then count <= (others => '0');
else count <= count + 1;
end if;
end if;
end process;
-- transition function
process (state, x, Btn, count)
begin
case State is
...
when a2 =>
if Btn = '1' and count >= constraint_a2_L - 1 and
count < constraint_a2_H then next_state <= a4;
elsif count < T2 - 1 then next_state <= state;
elsif x(1) = '1' then next_state <= a4;
elsif x(2) = '1' then next_state <= a1;
else next_state <= a3;
end if;
-- output function
y(1) <= '1' when ((state = a1) or (state = a2) or (state =
a4)) and count >= output_delay_Y1 else '0';

```

Fig. 4. Fragment of the VHDL model of timed Moore FSM

Figure 5 shows the timing diagram (waveform) of the simulation results of the considered control device of the ALDEC Active-HDL system.

The processing of the *Btn* event at time 2550 ns is of particular interest. This event falls into the interval *Input Constraint* for *Btn* [4; 5] for the state *a₂* and realizes the transition to the state *a₄* (highlighted arc *Btn* in fig. 3).

The synthesis report in figure 6 shows the results of the synthesis of the control device in the XILINX ISE system for FPGA: Spartan 3E, XC3S500E chip, Package FG 320 (xc3s500e-4fg320).

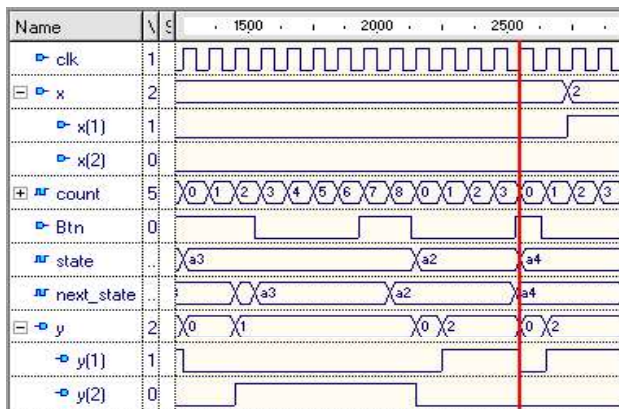


Fig. 5. Control device simulation results

```

Analyzing FSM <MFsm> for best encoding.
Optimizing FSM <FSM_0> on signal <state[1:2]> with user
encoding.
State | Encoding a1|00 a2|01 a3|10 a4|11
Final Register Report : Macro Statistics
# Registers : 6 Flip-Flops : 6

```

Fig. 6. The synthesis report of control device

The structure, consisting of two blocks, is synthesized: control FSM (2 D flip-flops for states coding, combinational

circuits implementing transition and output functions) and counter based on 4 D flip-flops for counting 9 cycles of the maximum timeout. To confirm the complete correctness of timing parameters of the proposed model, it was necessary to perform timing simulation, but this is the subject of further research.

CONCLUSION

As a result of the conducted research, it was shown that during automated design of real-time logic control systems it is advisable to use models of the timed control FSM. Problems of constructing timed FSM that take into account timing constraints, input timeouts and output delays were considered. To describe these models in hardware description language VHDL during automated design, a three-process pattern in the style of automata-based programming for Moore FSM was developed, which contains the combinational process for describing transition functions, the synchronous process for new state assigning, and the synchronous process for accounting of FSM cycles. The simulation of developed VHDL model in the Active-HDL system and the circuit synthesis using the XILINX ISE CAD tools in the FPGA on the Spartan 3E board showed the efficiency of the proposed model. At the same time, hardware costs don't go beyond the standard rate for FSM states' encoding and formation discharges of FSM cycles' counter.

A practical value of obtained results is that authors proposed the pattern, describing algorithms for the functioning of the timed FSM in real-time logic control systems in the VHDL language, which can be used by beginner designers of digital logic control systems, as well as students of the specialty "Computer Engineering".

A direction of further research may be the use of the Mealy model for the implementation of timed control FSM

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