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The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

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CONTENTS

The Method of Fault Backtracing for HDL - Model Errors Searching

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Abstract

In this paper the method of design error searching in non-structured HDL-code was considered. The method of backtracing was developed. An experiment on HDL-model of digital device using this method was carried out.

1. Problem statement

In modern CAD tools the basic way of device description is usage of hardware description languages, i.e. VHDL or Verilog, which allow making SOC design process faster. World companies – vendors of digital circuits, are forced to decrease their time-to-market. Verification of digital projects, that is hardware or built-in hardware-software systems described in a Hardware Description Language - HDL, is the important task during designing digital devices. Often more than 70% of development time is spent on search and correction of mistakes in the project. Process of diagnosing is based on: DD model, allowing carrying out tests generation; designing errors, characteristic for HDL-models; algorithm of tests generation; methods of design errors search. Within the framework of technical diagnostics methods, there are several algorithms of defects search: based on available tests and known function of the device (functional algorithms on the base of errors tables or functions of errors tables), and based on the structure of the device (structural algorithms on the base of a reachability matrix). *The purpose* of the given work is to develop methods of defects/errors search in a non-structured HDL-code, allowing to reduce time of carrying out of diagnostic experiment and to reduce length of the diagnosis. Proceeding from the aforesaid, it is necessary to solve *a task* of adaptation of the method of backtracing at verification of HDL-models and to carry out diagnostic experiments on defect/design error search within the framework of verification.

2. The method of defect search

In this paper, similar to the definition of defect the concept of design errors is used. Diagnostic Experiment (DE) on HDL-code is implemented in two phases. At the first stage an unconditional experiment is held. If at least one external output does not match the benchmark, the second phase of DE is carried out. The problem of diagnosing the technical condition of the digital model is to minimize the area of error existence domain considering the predefined class, which is called the set of equivalent defects, at the allowable length of the test parameters and the number of observed outputs. The greater the length of the test and the number of observed outputs, the higher the resolution of the diagnosis algorithm, which should provide the component defect search only for the actual reactions without accessing control points (CP). At fixing the length of the test parameters and the number of observed outputs in defect search algorithms, based on the analysis of malfunctions tables, the depth of diagnosis can be increased through the use of input-output relationship of elements (operands and operators) in a digital model of the device. The maximum adequate reaction of the model with a defect on a test-vector is a row-vector with values on observable elements of the model. As an example, the method of testing diagnosing errors in a digital device model based on multi-value fault table (MVT) and the analysis of the structure of the object can be considered. All functional elements (FE) or operand vertexes enter into the initial area of suspected design errors. Diagnostic experiment is carried out

with the assumption, that there is the single mistake in a code resulting in a faulty value on some operand vertex which is either a control point, or an external output. The main principle underlying structural methods of design error search is the following. If in the next control point the result of the elementary check is negative, the FE itself and all its predecessors enter into the area of suspected mistakes on the next step of the algorithm. If the result of the check is positive, all predecessors are assumed fault-free, and the suspected mistake has taken place among the other FE from the area of suspected mistakes on the previous step of the algorithm. If transportation of a design error on an external output is impossible, it is necessary to break the graph into subgraphs by a principle of sensitization existence. The reason of sensitization impossibility can be either in a code which was constructed in such a way, or there is a mistake in a code (a prospective place of a mistake - a subgraph of its predecessors). Etalon checking tests are inadequate for the several reasons. The basic of them is that the construction of checking tests is based on the concepts of transportation and sensitization of a path along which the error is transported to an external output of the circuit. And it not always obviously possible for fulfilling, as in a HDL-code functional malfunctions can be disguised by further calculations in such a manner that the mistake will not be observed on an external output. For example, a mistake on an output of any functional element is not transported on an external output if among its successors there is a logic OR operator with constant 1 on one of the inputs. For decomposition of the initial graph control points (similarly to control points at generation of tests which allow "to break" a path of sensitization and to define borders of subgraphs) are used. The given control points will be the outputs of each of subgraphs. Thus, a design error is transported on an external output of each subgraph. There are two types of the control points used by search of a place of a mistake. Control points of the first sort - the model signal (variable), etalon values of which are known from the specification. Control points of the second sort - the model signal (variable), values of which are observable, but prior to the experiment start are unknown. Structuring of the initial model on HDL is carried out by allocation multi-output subgraph which is generated (activated) as a result of driving specialized test onto inputs. Inputs of a subgraph are external inputs (operand vertexes, not only physical), and outputs are CP of the first sort. By results of carrying out the first stage of diagnostic experiment (driving tests for definition of presence of a design error in the description) the vector of experimental check results is formed, it fixes equality of etalon and experimental reactions. In other words, it is defined what outputs a design error influences on.

3. The method of backtracing

In specifications of HDL-models of real digital devices, as a rule, there is very few CPs of the first sort, etalon values of which are known prior to the experiment start. Therefore localization up to a subgraph with the CP of the first sort is insufficient. It is desirable to carry out localization of erroneous operators up to a CP of the second sort, but etalon are nowhere to be taken from. The decision for this contradiction is to apply the method of backtracing, which has originally been focused on constant faults search in digital circuits in conditions of etalon absence in internal points, in a subgraph where CP the first sort is an output. The classical method of backtracing which sometimes was named a method of "seeking", was based on the following positions: there is a device with accessible internal lines and its structural-functional model; there is a condition of essentiality for each element; there is a test which activate paths in the model, there are etalon reactions on the external output of the model. To use this method at "seeking" in a class of equivalent mistakes at diagnostics of a HDL-code, updating of the method is necessary. The following positions are accepted:

1. A class of design errors - replacement of a functional element.
2. Distinguishing sequence (DS) are used as tests for every FE.
3. Faulty (erroneous) FE is the one on which inputs the discrepancy with etalons was last observed.

The algorithm of "seeking":

1. Tests simulation on real model up to an external output (CP) is carried out.
2. If discrepancy with the etalon on the output is revealed, backtracing is carried out.
3. Backtracing goes until the result is equal to ∅; it is performed by intersection of the current vector with conditions of essentiality of a functional element.
4. The subset of suspected elements is formed on a base of nonempty intersections.

Let there be some erroneous HDL-code (fig.1), for the circuit in fig.2. There is an error in the code: in operator S12 the OR is replaced with the AND.

Entity SCH **is Port** (X1,X2,X3,X4,X5,X6,X7, X8: **in bit**; O15: **out bit**); **End**; **Architecture** BEH **of** SCH **is signal** S9, S10, S11, s12, s13, S14: **bit**; **begin**
S9<=X1 **and** x2; S10<=X3 **and** x4; S11<=X5 **and** x6; S12<=X7 **and** X8; S13<=S9 **and** S10; S14<= S11 **and** S12; O15<=S13 **nand** S14; **End**;

Figure 1. The example of HDL-model

For this fragment a test is built: 11011100 – and there is the etalon value 0 on the external output (O15). As a result of driving the test on the HDL-model '1' is received on its output that does not coincide with the etalon. Let's execute backtracing, marking its results for presentation on the fragment of the digital circuit (fig.2), equivalent to the resulted code.

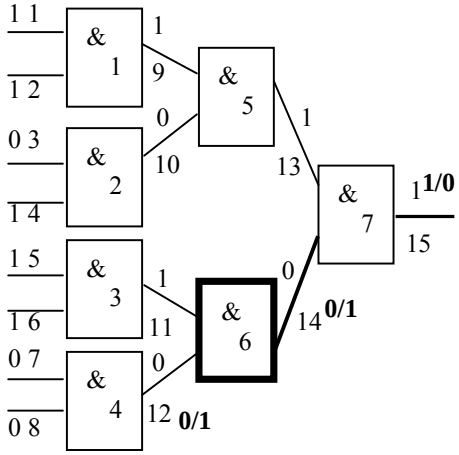


Figure 2. The example of «seeking» for the structurally functional circuit

The most effective form for realization of return implication is the cubic form of model primitive elements; therefore for better understanding we shall consider "seeking" method application in the cubic form. If to consider a condition of essentiality in the cubic form, they are similar to D-coverings, but don't take into account the direction of transition (inversion). Coverings of essentiality for AND and OR are in fig.3.

X1	X2	X3	Y
Z	1	1	Z
1	Z	1	Z
1	1	Z	Z

X1	X2	X3	Y
Z	0	0	Z
0	Z	0	Z
0	0	Z	Z

Figure 3. Coverings of essentiality for AND / OR

The procedure of the backtracing for a fragment of the HDL-code with predetermined concurrent signals assignments (CSA) is similar to the procedure of return implication for a combinational circuit, on condition that coverings of essentiality of corresponding CSA are used as primitive elements. Simulation of the test on a real (faulty) code is originally carried out and the result of simulation is written to the first row. The result does not coincide with the etalon from the specification; backtracing therefore is carried out by intersecting the received vector with coverings of essentiality of the model elements. Intersections are carried out until the result is not equal ∅. The procedure of backtracing is resulted in table 1.

Table 1. Backtracing procedure

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	1	0	1	1	1	0	0	1	0	1	0	1	0	1	etalonis 0
														z	Line 15 is essencial
												1	z	z	∩≠∅
												z	1	z	→∅
1	1	0	1	1	1	0	0	1	0	1	0	1	z	z	Line 14 is essencial
										z	1		z		→∅
										1	z		z		∩≠∅
1	1	0	1	1	1	0	0	1	0	1	z	1	z	z	Line 12 is essencial
						z	1				z				→∅
						1	z				z				→∅

Thus, the element at which line 12 is an input, i.e. element 6, is faulty: it was OR, and became AND, as it was shown. Each specialized test generates a multi–output subgraph which inputs are external inputs (or CP of the first sort), and outputs are external outputs (or CP of the first sort). Except CSA there are sequential operators in a HDL-code. Special interest at backtracing is represented by conditional operators (*IF, CASE*) since they are on a joint of data and control. Let's consider *IF*: *IF ((x1 and x2) or (x3 and x4)) THEN y<=d1 ELSE y<=d2*. *IF*, realizing two-output conditional vertex, consists of a logic condition *C* and two executing CSAs. Logic condition *C* in *IF* (C) is the equation, the decision in the cubic form is in fig. 4:

$$C = X1 \cdot X2 \vee X3 \cdot X4$$

X1	X2	X3	X4	C
0	X	0	X	0
0	X	X	0	0
X	0	0	X	0
X	0	X	0	0
1	1	X	X	1
X	X	1	1	1

Figure 4. The solution of the equation

Thus, *IF* can be submitted by the multiplexer model with two information inputs, a group of control inputs, and 1 (2) output (2 output in case of different signals). The covering of essentiality of *IF* is in fig.5.

X1	X2	X3	X4	D1	D2	Y
0	X	0	X	X	Z	Z
0	X	X	0	X	Z	Z
X	0	0	X	X	Z	Z
X	0	X	0	X	Z	Z
1	1	X	X	Z	X	Z
X	X	1	1	Z	X	Z

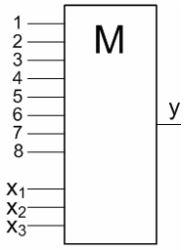
Figure 5. Coverings of essentiality of *IF*

Except the *IF*, the *CASE* can be treated as a conditional operator which realizes multi-output conditional vertex. The fragment of the HDL-code with *CASE* is submitted in figure 6.

```
variable xxx : in std_logic_vector(2 downto 0);
case xxx is when "000"=> Y<=D1; when "001"=> Y<=D2; when "010"=> Y<=D3; when "011"=> Y<=D4; when "100"=> Y<=D5; when "101"=> Y<=D6; when "110"=> Y<=D7; when "111"=> Y<=D8; end case;
```

Figure 6. The fragment of the HDL-code with *CASE*

The model of *CASE* in the form of the multiplexer and its covering of essentiality is submitted in fig.6.



1	2	3	4	5	6	7	8	X1	X2	X3	Y
Z	X	X	X	X	X	X	X	0	0	0	Z
X	Z	X	X	X	X	X	X	0	0	1	Z
X	X	Z	X	X	X	X	X	0	1	0	Z
X	X	X	Z	X	X	X	X	0	1	1	Z
X	X	X	X	Z	X	X	X	1	0	0	Z
X	X	X	X	X	Z	X	X	1	0	1	Z
X	X	X	X	X	X	Z	X	1	1	0	Z
X	X	X	X	X	X	X	Z	1	1	1	Z

Figure 7. The model of *CASE* as multiplexer and its covering of essentiality

The arithmetic operators executed, as a rule, with multidigit operators can be considered to be CSA too. If to consider addition of one-digit operands S=A+B the circuit realization of it is the one-digit two-input adder. Its law of its functioning and a fragment of the essentiality covering are resulted in fig.7. It is necessary to note, that the covering of essentiality is constructed dynamically on the basis of the functioning law of the adder. Having coverings of essentiality for the one-digit adder and taking into account procedures of return implication through arithmetic operands, procedures of backtracing of essentiality through multidigit arithmetic operations can be easily built. We shall note that only coverings of essentiality, which are one-dimensional on inputs, can be correct for arithmetic operations.

A_i	B_i	C_{i-1}	S	C_i
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

A_i	B_i	C_{i-1}	S	C_i
Z	0	0	Z	0
0	Z	0	Z	0
0	0	Z	Z	0
Z	1	1	Z	1
1	Z	1	Z	1
1	1	Z	Z	1
Z	0	1	Z	Z
0	Z	1	Z	Z

Figure 8. The function law and a fragment of the essentiality covering of the one-digit adder

As an example let's consider addition of two four-digit operands S(4)=A(4)+B(4) where A=5, B=6, S=5+6=11. In the binary code S=A+B is 0101+0110=1011. If S=10Z1 (the symbol of essentiality is in the third output digit category), there is only one correct decision: A=0101 and B=01Z0. As a check let's consider S=A+B=0101+01Z0=10Z1, on condition that Z={0,1}. The given example confirms an opportunity of carrying out return implication of symbol Z through multidigit arithmetic operators. Thus, having coverings of essentiality for CSAs and conditional operators it is possible to carry out backtracing for any fragments of a HDL-code.

4. Conclusion

Methods of search of defects (design errors) for verification of HDL-models allow not only to speak about presence of an error in the design, but also to define precisely a place of its occurrence (to locate defect). In this work we offer the method of backtracing which is applicable for "seeking" in the subgraphs which do not have control points of the first sort inside. This classical method of "seeking" was improved and it can be applied to HDL-code of different complexity.

5. References

[1].Yev. Yef. Syrevitch Verification of HDL-based models // PhD Thesis. Kharkov. 2007.

[2].Syrevitch Yev., Kucherenko D., Karasev A. Structural defect search method in HDL-models of radio electronic devices // 3rd International Radio and electronic Forum Kharkov, Ukraine, 22-24 October 2008, p. 48-51.

[3]. Abramovici M., Breuer M., Friedman A. Digital System Testing and Testable Design // IEEE Press. New York, 1998. 652 p.

[4]. G. Kryvulya, Yev. Syrevitch, A. Karasyov, D. Chegikov. Test Generation for VHDL Descriptions Verification // Proc. of IEEE EWDT. Odessa, Ukraine, September 15 – 19, 2005, 191 195.

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