THREE APPROACHES FOR ORGAIZATION OF CONTROL UNITS FOR EMC

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Abstract

Three new approaches are analysed targeting at implementing FPGA-based circuits of control units. Each of them leads to a unique architecture of a control unit. Depending on characteristics of a control unit, one of these approaches provides minimum hardware consumption. The methods target control blocks for electromagnetic compatibility of radiotechnical devices.

1. Introduction

Providing the electromagnetic compatibility for different radiotechnical devices is one of very important problems connected with FPGA-based design. This problem arises, for example, during the design of sophisticated embedded systems [1]. To solve this problem, various sequential blocks should be used. These blocks can be represented using the model of Mealy finite state machine (FSM) [2]. If circuits of these blocks are implemented using look-up table (LUT) elements, then a problem of hardware reduction arises [3, 4]. To optimize the FSM characteristics, various methods of state assignment can be used. Three new methods are analysed in this paper.

2. The essence of a problem

To implement an FSM circuit, it is necessary to construct two systems of Boolean functions (SBFs) [5]. Functions of both SBFs depend on FSM inputs $\boldsymbol{x_l} \in \boldsymbol{X}$ and state variables $\boldsymbol{T_r} \in \boldsymbol{T}$. These SBFs represent input memory functions (IMFs) $\boldsymbol{D_r} \in \boldsymbol{D}$ and FSM outputs $\boldsymbol{y_n} \in \boldsymbol{Y}$ [5]. As a rule, an FSM has $\boldsymbol{L}$ inputs, $\boldsymbol{N}$ outputs, $\boldsymbol{R}$ state variables and IMFs. These SBFs are represented by sum-of-products having product terms with up to $\boldsymbol{L + R}$ literals.

The peculiarity of LUT is a very small number of inputs, $\boldsymbol{S_L}$ [5]. For a majority of practical FSMs, the following relation holds:

$$\boldsymbol{L + R \gg S_L}. \quad (1)$$

If (1) takes place, then various methods of functional decomposition [2] should be used. They lead to multi-level LUT-based FSM circuits having complicated systems of spaghetti-type interconnections [1].

As a rule, three main characteristics are used to estimate the quality of an FSM circuit. They are [6]: the LUT count, the maximum operating frequency, and the power consumption. To improve these characteristics, it is necessary to diminish the numbers of LUTs and their levels of FSM circuits.

3. Main idea of proposed state assignment methods

In this article, we propose to solve this problem using methods of state assignment based on finding some partition $\boldsymbol{\Pi_A} = \{\boldsymbol{A^1}, \dots, \boldsymbol{A^K}\}$ of the set of states $\boldsymbol{A} = \{\boldsymbol{a_1}, \dots, \boldsymbol{a_M}\}$. This partition should include a minimum possible number of classes. The following condition should be satisfied for each class of $\boldsymbol{\Pi_A}$:

$$\boldsymbol{R_k + L_k \le S_L}. \quad (2)$$

In (2), the symbol $\boldsymbol{R_k}$ stands for the number of state variables encoding the states $\boldsymbol{a_m} \in \boldsymbol{A^k}$, the symbol $\boldsymbol{L_k}$ stands for the number of FSM inputs determining transitions from the states $\boldsymbol{a_m} \in \boldsymbol{A^k}$.

In this case, an FSM circuit includes special blocks implementing the systems of partial functions

$$\boldsymbol{D^k = D^k(T^k, X^k)}; \quad (3)$$

$$\boldsymbol{Y^k = Y^k(T^k, X^k)}. \quad (4)$$

To implement systems (3)-(4), special blocks $\boldsymbol{LUTerk}$ ($\boldsymbol{k \in \{1, \dots, K\}}$) are introduced into an FSM circuit. Next, some block $\boldsymbol{LUTerF}$ implements the sum-of-products of functions $\boldsymbol{D_r \in D}$ and $\boldsymbol{y_n \in Y}$.

In this case, FSM states are represented by extended state codes (ESCs). Each ESC $\boldsymbol{K(a_m)}$ is a concatenation of partial codes $\boldsymbol{C^1(a_m)}$,..., $\boldsymbol{C^K(a_m)}$. As a result, there are $\boldsymbol{R_1 + R_2 + \dots + R_K = R_C}$ bits in the ESC.

Three different approaches can be used for generating ESCs. Each of them results in the different architecture of an FSM structural diagram. Also, each approach produces FSM circuits with different values of LUT counts and operating frequencies.

In the first case, they are generated by a special block $\boldsymbol{LUTerT}$. To implement this block, it is necessary to use additional LUTs and programmable interconnections. The block adds some delay in the resulting FSM performance (it reduces the value of the maximum operating frequency).

In the second case, the ESCs are generated by the LUTs from the second logic level. Due to it, there is no an additional block $\boldsymbol{LUTerT}$. But in this case, it is necessary $\boldsymbol{R_C}$ flip-flops to keep the state variables. This increases the requirements for the synchronization tree. In turn, this increases the power consumption.

In the third case, the same state variables are used for encoding states insides each class $\boldsymbol{A^k \in \Pi_A}$. To distinguish the classes $\boldsymbol{A^k \in \Pi_A}$, they should be encoded by special class codes. Now, a state code is a concatenation of two codes. This approach provides the minimum total number of state variables. But it leads to increasing electrical requirements for sources of state variables.

4.Conclusion

Three different methods of FSM logic circuit organization are discussed in this paper. All of them are based on using extended state codes for state assignment in LUT-based Mealy FSMs. In the first case (case 1), a special logic block transforms traditional state codes [5, 6] into ESCs. This block consumes some resources of an FPGA chip. Also, it increases the FSM operation cycle. In the second case (case 2), there is no additional block; the extended state codes are produced in parallel with output functions. This accelerates the FSM operation, but requires a lot of flip-flops. In turn, it leads to increasing the power consumption. In the third case (case 3), all classes use the same state variables for encoding the states for all classes. It is possible, if the classes have their own codes.

Our research [2] shows that the final FSM circuit characteristics depend on the relation between some characteristics of FSM ($\boldsymbol{L + R = S_F}$) and the number of LUT inputs, $\boldsymbol{S_L}$. If $\boldsymbol{S_F \le 2S_L}$, then using the case 1 leads to the best FSM circuit characteristics. If $\boldsymbol{S_F \le 4S_L}$, then using the case 2 leads to FSM circuits with the best characteristics. If $\boldsymbol{S_F > 4S_L}$, then it makes sense to use the case 3.

Our analysis helps to choose the best approach for the state assignment. This approach can be used in the LUT-based optimization of various sequential devices providing electromagnetic compatibility in telecommunications.

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