KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2013)

Copyright © 2013 by the Institute of Electrical and Electronics Engineers, Inc.



Technically Co-Sponsored by



tttc



Rostov-on-Don, Russia, September 27 – 30, 2013

IEEE EAST-WEST DESIGN AND TEST SYMPOSIUM 2013 COMMITTEE

General Chairs

Program Committee

Steering Committee

V. Hahanov – Ukraine Y. Zorian – USA

General Vice-Chairs

- R. Ubar Estonia
- P. Prinetto Italy

Program Chairs

- S. Shoukourian Armenia
- D. Speranskiy Russia

Program Vice-Chairs

- Z. Navabi Iran
- M. Renovell France

Publicity Chair's

- G. Markosyan Armenia
- S. Mosin Russia

Public Relation Chair

V. Djigan – Russia

J. Abraham – USA M. Adamski – Poland A.E.Mohamed Mohamed – Egypt A . Barkalov – Poland R. Bazylevych – Ukraine A. Chaterjee – USA V. Djigan – Russia A. Drozd – Ukraine E. Evdokimov – Ukraine E. Gramatova – Slovakia A. Ivanov – Canada M. Karavay – Russia V. Kharchenko – Ukraine K. Kuchukjan – Armenia W. Kuzmicz – Poland A. Matrosova – Russia V. Melikyan – Armenia L. Miklea – Romania O. Novak - Czech Republic Z. Peng – Sweden A. Petrenko – Ukraine J. Raik – Estonia A. Romankevich – Ukraine A. Ryjov – Russia R. Seinauskas – Lithuania S. Sharshunov – Russia A. Singh – USA J. Skobtsov – Ukraine V. Tverdokhlebov – Russia V. Vardanian – Armenia

V. Yarmolik – Byelorussia

EWDTS 2013 CONTACT INFORMATION

Prof. Vladimir Hahanov Design Automation Department Kharkov National University of Radio Electronics, 14 Lenin ave, Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26 E-mail: hahanov@kture.kharkov.ua Web: www.ewdtest.com/conf/

- V. Hahanov Ukraine
- R. Ubar Estonia
- Y. Zorian USA

Organizing Committee

- S. Chumachenko Ukraine
- M. Karyakin Russia
- S. Krutchinskiy Russia
- E. Litvinova Ukraine
- N. Prokopenko Russia
- B. Steinberg Russia

11th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2013) Rostov-on-Don, Russia, September 27-30, 2013

The main target of the **East-West Design & Test Symposium** (EWDTS) is to exchange experiences between the scientists and technologies of the Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic systems. The symposium aims at attracting scientists especially from countries around the Black Sea, the Baltic states and Central Asia. We cordially invite you to participate and submit your contribution(s) to EWDTS'13 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level TPG
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Test
- Power Issues in Testing
- Real Time Embedded Systems

- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- Using UML for Embedded System Specification

CAD Session:

- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Rostov-on-Don, Russia, one of the biggest scientific and industrial center. Venue of EWDTS 2013 is Don State Technical University – the biggest dynamically developing centre of science, education and culture.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Don State Technical University and Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Aldec, Synopsys, DataArt Lab, Tallinn Technical University, Aldec Inc.



CONTENTS

Impact of Process Variations on Read Failures in SRAMs Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.	15
Noise Effect Estimation and Reduction in High-Speed Voltage Controlled Oscillators Vazgen Melikyan, Abraham Balabanyan, Armen Durgaryan	19
A Probabilistic Approach for Counterexample Generation to Aid Design Debugging Payman Behnam, Hossein Sabaghian-Bidgoli, Bijan Alizadeh, Kamyar Mohajerani, Zainalabedin Navabi	23
Hybrid History-Based Test Overlapping to Reduce Test Application Time Vahid Janfaza, Payman Behnam, Mohammadreza Najafi, Bahjat Forouzandeh	28
A Mathematical Model for Estimating Acceptable Ratio of Test Patterns Vahid Janfaza, Paniz Foroutan, M. H. Haghbayan, Zain Navabi	32
Session based Core Test Scheduling for Minimizing the Testing Time of 3D SOC Surajit Roy, Payel Ghosh, Hafizur Rahaman, Chandan Giri	36
Functional Fault Model Definition for Bus Testing Elmira Karimi, Mohamad Hashem Haghbayan, Adele Maleki, Mahmoud Tabandeh	40
Evolution of von Neumann's Paradigm: Dependable and Green Computing Kharchenko V., Gorbenko A.	46
Quantum Technology for Analysis and Testing Computing Systems Wajeb Gharibi, Hahanov V.I., Anders Carlsson, Hahanova I.V., Filippenko I.V.	52
Diversity Assessment of Multi-Version NPP I&C Systems: NUREG7007 and CLB-BASED Techniques Kharchenko V Duzhvi V Sklvar V Volkoviv A) 57
Features of Design, Implementation, and Characterization of On-Chip Antennas for Microwave Frequencies Aleksandr Timoshenko, Ksenia Lomovskaya, Mikhail Suslov	62
Design and Optimization of a Planar UWB Antenna Eng Gee Lim, Zhao Wang, Gerry Juans, Ka Lok Man, Nan Zhang, Vladimir Hahanov, Eugenia Litvinova, Svetlana Chumachenko, Mishchenko Alexander, Dementiev Sergey	67
Cloud Traffic Control System Hahanov V.I., Guz O.A., Ziarmand A.N., Ngene Christopher Umerah, Arefjev A.	72
Cloud Infrastructure for Car Service Litvinova E.I., Englesy I.P., Miz V.A., Shcherbin D.	77

Quantum Computing Approach for Shortest Route Finding Volodymyr Hahanov, Volodymyr Miz	85
Quantum Modeling and Repairing Digital Systems Baghdadi Ammar Awni Abbas, Hahanov V.I., Palanichamy Manikandan, Litvinova E.I., Dementiev S.	88
Quantum Models for Description of Digital Systems Hahanov V.I., Hahanova I.V., Litvinova E.I., Priymak A., Elena Fomina, Maksimov M., Tiecoura Yves, Malek Jehad Mohammad Jararweh	94
A Concept of Computing Based on Resources Development Analysis Drozd J., Drozd A., Zashcholkin K., Antonyuk V., Kuznetsov N., Kalinichenko V.	102
Blind Least Mean Square Criterion Algorithms for Communication Adaptive Arrays Victor I. Djigan	108
Estimation of structural complexity of IIR digital filters Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich	113
ASICPlacementAnalyzer: Software Tool for Data Analysis and Visualization of ASIC Placement Victor M. Kureichik, Maria V. Lisyak	118
Robust Watermarking System for Audio Identification Aleksandr V. Shishkin	122
Adaptive Artificial Boundary Conditions for Schrödinger Equation Taking into Account the First Order Dispersion of Laser Pulse and Diffraction of Laser Beam Vyacheslav A. Trofimov, Anton D. Denisov	125
Research of Methods to Create Informational Composition With the View of CAD of Intellectual Training Devices Knowledge-Based Signals of Cerebral Cortex Lavlinskiy V.V., Bibikov D.V., Burov R.B., Tabakov Y.G., Zolnikov K.V., Achkasov V.N.	129
Development of Upgraded Version of Finite Element Package ACELAN Arcady Soloviev, Pavel Oganesyan, Darya Krivorotova	123
Statistical Characteristics of Envelope Outliers Duration of non-Gaussian Information Processes Artyushenko V. M., Volovach V. I.	137
Optimizing Test Time for Core-Based 3-D Integrated Circuits by a Technique of Bi-partitioning Manjari Pradhan, Chandan Giriy, Hafizur Rahamany, Debesh K. Das	141
Basic Concept of Linear Synthesis of Multi-Valued Digital Structures in Linear Spaces Chernov N.I., Yugai V.Ya., Prokopenko N.N., Butyrlagin N.V.	146

Boundary Problem for Nonlinear Elliptic Equations on Video Card Hasmik A. Osipyan	150
The High-Frequency Correction Circuit for Resistive Voltage Dividers with Capacitive Loa Prokopenko N.N., Budyakov P.S., Butyrlagin N.V.	id 154
Simulation Features of Diffusion Doping Process by Means of Software Package of Synopsys Company Lagunovich N.L., Borzdov V.M., Turtsevich A.S.	158
Synthesis Circuit Correction for Speed Sensors of Physical Quantities and Current-Voltage Converters with Parasitic Capacitance Prokopenko N.N., Gaiduk A.R., Budyakov P.S., Butyrlagin N.V.	161
Microwave Selective RC Amplifiers with Control Parameters Prokopenko N.N., Krutchinsky S.G., Budyakov P.S.	165
Using Java Optimized Processor as an Intellectual Property core beside a RISC Processor in FPGA Mohammad Erfan Khazaee, Shima Hoseinzadeh	169
The automated testing system for optimizing and parallelizing program transformations Alymova E., Golozubov A., Morylev R., Pitinov A., Steinberg R.	175
Methodology to Design-For-Testability Automation for Mixed-Signal Integrated Circuits Sergey Mosin	178
Static Analysis of HDL Descriptions: Extracting Models for Verification Alexander Kamkin, Sergey Smolov, Igor Melnichenko	184
Fault-Injection Testing: FIT-Ability, Optimal Procedure and Tool for FPGA-Based Systems SIL Certification Kharchenko V., Sklyar V., Odarushchenko O., Ivasuyk A.	188
Query Optimization Based on Time Scheduling Approach Wajeb Gharibi, Ayman Mousa	193
Analysis of Error-Detection Possibilities of CED Circuits Based on Hamming and Berger Codes Valery Sapozhnikov, Vladimir Sapozhnikov, Dmitry Efanov, Anton Blyudov	200
Low-Power Design of Combinational CMOS Networks Dmitry Cheremisinov, Liudmila Cheremisinova	208
IGBT on SOI. Technology and Construction Investigation Ivan Lovshenko, Vladislav Nelayev, Sergey Shvedov, Vitaly Solodukha, Arkady Turtsevich	212
Generating Pipeline Integrated Circuits Using C2HDL Converter Denis Dubrov, Alexander Roshal	216

Data-Flow Multiprocessor with Deterministic Architecture Novatsky A. A., Glushko Je. V., Chemeris A.A., Pugachov O.S.	220
An Approach to Estimate the Error of Oscillator Time-Domain Analysis Vadim N. Biryukov, Alexandr M. Pilipenko	223
Sampling Theorem Applied to Data Interpolation Problem Gamlet S. Khanyan	227
A Few Test Generation Algorithms for web Applications from Imitational Model Anahit Asatryan	231
Design Automation Tool to Generate EDIF and VHDL Descriptions of Circuit by Extraction of FPGA Configuration Cheremisinov D.I.	235
Object-Oriented Approach to Software Implementation of Virtual Laboratory Workshop Gubsky D.S., Zemlyakov V.V., Mamay I.V., Sinyavsky G.P.	239
Schematic Design of HF and UHF Op-Amp for SiGe Technology Sergei G. Krutchinsky, Evgeniy A. Zhebrun, Victor A. Svizev	243
Improvement of Common-Mode Rejection Ratio in Symmetrical Differential Stages with Dynamic Load Sergei G. Krutchinsky, G.A. Svizev, Alexey E. Titov	247
Adaptation of the FPGA to Logic Failures Tyurin S.F., Grekov A.V., Gromov O.A.	251
Testable Combinational Circuit Design Based on Free ZDD-implementation of Irredundant SOP of Boolean Function Ostanin S.	257
On the Problem of Selection of Code with Summation for Combinational Circuit Test Organization	
Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov, Anton Blyudov	261
A 6-bit CMOS Inverter Based Pseudo-Flash ADC with Low Power Consumption Morozov D.V., Pilipko M.M., Piatak I.M.	267
Method of free C++ code migration between SoC level tests and stand-alone IP-Core UVM environments Fedor Putrya	271
A List Decoding Algorithm for Practical Reed-Solomon codes Sergey Egorov	275
On Stability of Optimization Process for Analog Circuits Markina T., Zemliak A.	279

Analysis of Converters with Heterogeneous Three-Pole Chain Structure Zhanna Sukhinets, Artur Gulin	283
The Modeling of Electromagnetic Fields Intensity in Urban Development Condition Anishin M.M., Zargano G. F., Zemlyakov V.V., Hondu A.A.	287
Estimation of Radio Wave Frequency Shift and Phase Incursion on the Basis of FPGA in the Retransmission Meter Vdovychenko I.I., Velychko D.A.	291
Delay Testable Sequential Circuit Designs Matrosova A., Mitrofanov E., Singh V.	293
Supervision in Airborne Systems with Antenna Array Klochko V.K., Nguyen Tr.T.	297
Self-timed Functionally Complete Tolerant Element with Different Supply Voltage Kamenskih A.N., Tyurin S.F.	300
SPICE Model Parameters Extraction Taking into Account the Lonizing Radiation Effects Konstantin Petrosyants, Maxim Kozhukhov	304
Analysis and Simulation of Temperature-Current Rise in Modern PCB Traces Petrosyants K.O., Kortunov A.V., Kharitonov I. A., Popov A.A., Gomanilova N.B., Rjabov N.N.	308
Coupled TCAD-SPICE Simulation of Parasitic BJT Effect on SOI CMOS SRAM SEU Petrosyants K.O., Kharitonov I.A., Popov D.A.	312
Digital Converter of Frequency Deviation Based on Three Frequency Generator Shakurskiy M.V., Shakurskiy V.K., Ivanov V.V.	316
Comparative Analysis of Coding Effectiveness in Telecommunication Systems with ARQ Anfalov K. V., Volovach V. I.	320
Multiagent Bionic Algorithm for Optimization of Circuitry Solutions Andrey Bereza, Andrey Storogenko, Luis Blanco	324
Nonlinear Filtering of Pseudonoise Signals Using High-Order Markov Chain Model Dmitriy Prozorov, Anton Chistyakov	328
Representation of Solutions in Genetic Placement Algorithms Zaporozhets D.U., Zaruba D.V., Kureichik V.V.	332
Digital Adaptive System of Linearization Power Amplifier Natalya V. Gudkova, Vladimir M. Chuykov, Ksenya V. Besklubova	336
A Parallel Shrinking Algorithm for Connected Component Labeling of Text Image Sergey S. Zavalishin, Yury S. Bekhtin	340

Automated Measurement of Digital Video Cameras Exposure Time Budilov V.N., Volovach V.I., Shakurskiy M.V., Eliseeva S.V.	344
Hybrid Pareto-Evolutionary Algorithm for Solving Mathematical Models of High Dimensional Electronic Circuits (HPEA) Vadim Beglyarov, Andrey Bereza, Luis Blanco	348
Finite State Machine Synthesis for Evolutionary Hardware Andrey Bereza, Maksim Lyashov, Luis Blanco	352
Increasing Efficiency of Information Transmission with Interference Influence by the Use of Multi-parameter Adaptation Nechaev Y.B., Kashenko G.A., Plaksenko O.A.	356
Analysis of Ferromagnetic Structures Fast-Acting Under the Influence of External Magnetic Fields of Various Intensity Alexander Shein, Gennady Sinyavsky, Larissa Cherkesova, George Shalamov	360
Modeling Using Multivariate Hybrid Regression Analysis Method Danilov A. A., Ordinartseva N. P.	365
Analog Input Section of the Ultrafast ADCs Prokopenko N.N., Serebryakov A.I., Butyrlagin N.V., Pakhomov I.V.	368
A Recursive Least Squares Solution to AOA Based Passive Source Localization Hejazi F., Azimi K., Nayebi M.M.	371
Identification Discrete Fractional Order Linear Dynamic Systems with Errors-in-Variables Ivanov D.V.	374
Self-Calibration Method for Capacitor Mismatch Elimination Vazgen Melikyan, Harutyun Stepanyan, Ani Aleksanyan, Ani Harutyunyan, Armen Durgaryan	378
Whitespace Calculation in 3D IC Ara Gevorgyan	382
Low-Voltage Compatible Linear Voltage Ramp Generator for Zero-Crossing-Based Integrators Melikyan Vazgen Sh., Dingchyan Hayk H., Sahakyan Arthur S., Vardan Grigoryants P., Safaryan Karo H.	386
High Accuracy Equalization Method for Receiver Active Equalizer Melikyan Vazgen Sh., Sahakyan Arthur S., Safaryan Karo H., Dingchyan Hayk H.	390
Implementation of Parallel Dataflow Computational Model on Cluster Supercomputers Levchenko N.N., Okunev A.S., Klimov Ark.V., Zmejev D.N.	394

Semiconductor Electronic Parts Testing Efficiency Martynov Oleg, Ogurtsov Alexander, Sashov Alexander	397
An Approach to Accelerated Life Tests of Electronic Components Koulibaba Andrey, Krasnov Mikhail, Prischepova Svetlana	401
Next Generation Visual Programming Technology Velbitskiy I.V.	404
Efficient Calculation of Cyclic Convolution by Means of Fast Fourier Transform in a Finite Field Amerbaev V.M., Solovyev R. A., Stempkovskiy A.L., Telpukhov D.V.	411
High-level Test Program Generation Strategies for Processors Shima Hoseinzadeh, Mohammad Hashem Haghbayan	415
Fault Tolerance of the Distributed Structure of Object Controllers for Automation of Transport Sergey Rodzin, Lada Rodzina	419
Effective planning of calculations on the PDCS "Buran" Architecture Levchenko N.N., Okunev A.S., Zmejev D.N., Klimov A.V.	423
Ways to Ensure the Stability of Circuits to Single Events in the Design of Radiation-Resistant Circuits Smerek V.A., Utkin D.M., ZoInikov V.K.	426
Smart Road Infrastructure Artur Ziarmand	430
Testing of Transport System Management Strategy Sergey Lupin, Than Shein, Kyaw Kyaw Lin, Anastasia Davydova	435
The Bioinspired Algorithm of Electronic Computing Equipment (ECE) Schemes Elements Placement Kureichik V.V., Kureichik VI.VI.	439
The Hardware Architecture and Device for Accurate Time Signal Processing Jiřr´ı Dost´al, Vladim´ır Smotlacha	443
Management Methods of Computational Processes in the PDCS "Buran" Levchenko N.N., Okunev A.S., Zmejev D.N., Klimov A.V.	446
Service-Oriented Computing (SOC) in a Cloud Computing Environment Petrenko A.I.	449
The Methodology of Two-Stage Masking Images in Information and Telecommunications Systems Barannik V. V., Vlasov A. V., Shiryaev A. V.	453

Perforated with Technology of Description Massives Differential Representation in the Delivery Compressed Images Systems Kulitsa O.S., Lekakh A.A., Akimov R.I.	457
Method of Coding Bitmap Transformant to Improve Image Compression while Maintaining a Predetermined Quality Image to be Transmitted in Infocommunication Real Time Systems Krasnorutskyi A.A., Hahanova A.V., Demedetskiy A.O.	461
Method Structure Coding of Aperture Elements for Image in Infocommunication Systems Barannik V.V., Dodukh A.N., Krivonos V.N.	465
Domain-Driven Design the Database Structure in Terms of Metamodel of Object System Pavel P. Oleynik	469
An Approach to the Fuzzy Logic Modeling of Digital Devices Dmitriy Speranskiy	473
Reconfiguration of FPGAs Using Genetic Algorithms Gorodilov A. Yu., Tyurin S. F.	477
Algorithm for Automated Custom Network-on-Chip Topologies Design Bykov S. O.	481
Choice of Variants of Radio-Frequency Identification Systems on Set of Quality Parameters Bagdasaryan A.S., Kashenko A.G., Kashenko G.A., Semenov R.V.	484
Green logic FPGA Tyurin Sergey, Kharchenko Vyacheslav, Prokhorov Andrey	489
Restoration missing values of discrete signal during the calibration ADC with build-in interpolation Koroleva Ksenia, Gritsutenko Stanislav	492
Keynotes Speeches and Invited Reports	496
AUTHORS INDEX	501

Quantum Computing Approach for Shortest Route Finding

Volodymyr Hahanov, Volodymyr Miz

DSc, Computer aided design department of Kharkiv National university of Radioelectronics PhD student, Computer aided design department of Kharkiv National university of Radioelectronics hahanov@kture.kharkov.ua, mizvladimir@gmail.com

Abstract

In this paper shortest path finding approach is proposed. This approach is based on graph theory and uses main idea of the quantum computing. Quantum computing approach allows making parallel computations faster. Using this approach in shortest route fining problem helps to find several ways simultaneously and give several alternative solutions which can be chosen according to special metrics and parameters.

1. Introduction

According to Cisco's forecasts, the global Internet traffic will reach 1.3 zettabyte in 2016. It is more than the total traffic over a period from 1984 to 2012. In 2011, 369 exabytes were transferred over IP-based networks around the world. The number of Internet-connected devices will rise to 18.9 billion in 2016, or two-and-a-half for each person on the Earth. In 2011 this figure was equal to 10.3 billion. Today's personal desktop computers consume 95% of overall traffic. In 2016 this value will decrease to 81% due to growth number of mobile devices. The total Internet audience reaches 3.4 billion people, and the average fixed connection speed will increase from 9 to 34 megabits per second. Each user will load through a network about 32.3 gigabytes per month.

Nowadays every modern car is equipped with an onboard embedded computer, which also has access to the World Wide Web. Total number of cars in the world is continuously growing with an incredible pace. Thus in 2009, the center of the global auto industry, WardsAuto, has registered approximately 980 million vehicles. In 2010 this number has exceeded 1 billion. The most automobile countries (car:number of citizens) are the USA (1:1.3), Italy (1:1.45), the United Kingdom, France and Japan (1:1.7) [4]. Thus,

analyzing and comparing world's data traffic consumption and the rapid growth of the number of vehicles with on-board computers, it can be concluded that it is addressing the creation of global services for cars will be one of the major challenges in the field of information technology in the near future, namely information analysis and microelectronic systems design.

One of the most difficult driver's tasks is to build the best route on the road map. To date, this problem is not completely solved by existing devices, as they do not take into account the different metrics that affect the time and comfort of the route.

At this moment, quantum calculation approach allows to find several possible results simultaneously. This can greatly increase efficiency of the shortest route finding.

2. Metrics

Component, object, process and phenomenon identification in cyberspace provided by creation an effective metric measuring distances in discrete boolean (logical-vector) space, which is used for highspeed robots-engines development, which determine the derivative and the similarity or difference level between two components or objects.

Discrete vector-logical space (cyberspace) is a set of information processes and phenomena interacting according to specific metrics and described by vectors (matrices) and logical variables. They use computer systems and networks as a carrier.

Metric is a way of the distance measuring between the components in the space of processes or phenomena described by vectors of logical variables. Distance in cyberspace is xor-relation between the pair of vectors signifying the components of a process or phenomenon. This distinguishes it from the Hamming code distance. Distance, derivative (Boolean), change level, difference, similarity are isomorphic. They are connected with two components or phenomena definition. The components proximity (distance) notion in cyberspace is a measure of their differences. Comparison, measurement, evaluation, recognition, testing, diagnosis, identification procedures are a relationships determining method in that case if at least one object exists.

Cyberspace metrics can be defined by equation:

$$b = \bigoplus_{i=1}^{n} d_i = 0$$

which creates 0-vector, for XOR of each d_i – distance between non-zero and finite number of points (objects) in loop. Here n is number of the distances between components (vectors) in cyberspace, which creates the loop $D = (d_1,...,d_n)$, d_i is distance vector corresponding to edge of the loop which connects two components (vectors) of the a, b space.

3. Road graph

In order to create a route, we need to represent entire map as a directed graph of roads. Road graph is a set of metrically and topologically related vertexes and edges which represent traffic direction with high accuracy, distance and communication between crossroads. The direction of the edges shows the traffic direction, vertexes or nodes – crossroads. Each edge has a metric-based weight. The metrics are selected on the graph creation step, for example minimum number of left turns, better quality roads, the highest possible speed, the minimum number of traffic lights, etc.

Road graph must be updated each time when optimal route is requested to improve a relevance of the information about the routes. You cannot use the road graph laid during design phase, since the traffic situation is constantly changing and the route that was considered as optimal for one traffic situation may lose relevance to current traffic situation. For example, road can be repaired, car crash may occur, traffic can be blocked during public events, etc. Constantly updated road graph gives possibility to generate the best route at given time, and this route does not lose relevance until next road graph update.

The Road graph update means edges weight update. Complete rebuild the road graph for each request does not make a sense, since the roads position on the map, traffic direction and crossroads remain unchanged for a long enough period of time. Weights update allows you to track every detail of the road network changes and allows using a constant road graph.

4. Quantum approach for shortest path

The problem of finding the shortest path between two points in a weighted graph is an old one. The question of which classical algorithms can be sped up by quantum computing is of course a very interesting one. At present there are only a few general techniques known in the field of quantum computing and finding new problems that are amenable to quantum speedups is a high priority. Quantum approach for finding the lowest weight path has been considered in M. Heiligman's work [1].

In the classical case, the total work for the algorithm is max $(O(kn^2), O(n^2))=O(n^2)$ which is minimized by taking k=1, therefore

$$W_{classical} = O(n^2)$$

In the quantum case, the situation is a bit different. The total work on the first step is just the maximum of the work on next two steps, since the work on the first step is always dominated by these other work factors. The total work is therefore

$$\max (O(k^{\frac{1}{2}}n^{\frac{3}{2}}), O(k^{-\frac{1}{2}}n^{2}))$$

and to minimize this, the parameter k should be chosen to make these two work factors the same. Setting $k^{1/2} n^{3/2} = k^{-1/2} n^2$ gives $k = n^{1/2}$ and therefore

$$W_{quantum} = O(^{n7/4})$$

This indeed is an improvement over the classical work factor of n^2 .

5. Choosing the best path

Quantum approach allows finding several alternative solutions of shortest path problem. Then we need to choose one of the found path using metrics and parameters. Every metric and parameter of the optimal path should be presented as a vector. The aim of the vector-logical quality criteria is to significantly improve calculating performance of the interaction between components (vectors) by using only vector operations performed simultaneously of all discharges. We can make it with help of logical merging [2]: $\begin{array}{l} Q=d(m,A)\vee \mathbb{M}(m\in A)\vee \mathbb{M}(A\in m)=\\ =(m\oplus A)\vee (A\wedge\overline{m}\wedge A)\vee (m\wedge\overline{m}\wedge A)=\\ =(m\oplus A)\vee [A\wedge (\overline{m}\vee \overline{A})]\vee [m\wedge (\overline{m}\vee \overline{A})]=\\ =(m\oplus A)\vee [(A\wedge\overline{m})\vee (A\wedge\overline{A})\vee (m\wedge\overline{m})\vee (m\wedge\overline{A})]=\\ =[(A\wedge\overline{m})\vee (m\wedge\overline{A})]\vee [(A\wedge\overline{m})\vee (A\wedge\overline{A})\vee (m\wedge\overline{m})\vee (m\wedge\overline{A})]=\\ =(A\wedge\overline{m})\vee (m\wedge\overline{A})\vee (A\wedge\overline{m})\vee (A\wedge\overline{A})\vee (m\wedge\overline{m})\vee (m\wedge\overline{A})=\\ =m\oplus A. \end{array}$

Better solution searching model with a minimal number of '1' is shown on the figure. It includes following operations:

1) Initially, every coordinate of the result vector Q is filled by '1' value (the worst solution). Operation SLC (left shift) is performed simultaneously to compress '1' in the current vector Q_i .

2) Compare two vectors: \boldsymbol{Q} and $\boldsymbol{Q}_i,$ from decision list.

3) Vector operation AND is implemented Q^AQ_i and the result is compared with vector Q. This makes possible to modify it if the vector Q_i has a minimal number of '1' values.

4) The best solution finding procedure is repeated n times.



$$Q = Q(\overline{(\vee((Q \land Q_i) \oplus Q))}) \lor Q_i(\vee((Q \land Q_i) \oplus Q));$$

$$Y = \lor((Q \land Q_i) \oplus Q);$$

$$Q = Q\overline{Y} \lor Q_i Y.$$

In this case OR-reduction operator (after XOR element) generates a one-bit binary decision based on OR logic operation on the n bits of the quality criterion. For two binary vectors (quality criteria) selection the best one procedure is presented below:

$Q_1(m, A) = (6, 12)$	1	1	1	1	1	1					•	•
$Q_2(m, A) = (8, 12)$	1	1	1	1	1	1	1	1			•	•
$Q_1(m,A) \land Q_2(m,A)$	1	1	1	1	1	1	•	•	•	•	•	•
$Q_1(m, A) \oplus Q_1(m, A) \land Q_2(m, A)$		•						•		•	•	•
$Q(m, A) = Q_1(m, A)$	1	1	1	1	1	1						•

Numerical estimates are presented as explanatory information for a user Thus, quality vector logical criterion of objects interaction in cyberspace allows obtaining with a high speed parallel logic an estimate of search, pattern recognition and decision-making operations [3], which are particularly important for fast finding shortest path and selection the best one from several proposed solutions.

6. Conclusions

In this paper has been proposed new approach for shortest path search. It means using quantum algorithms and calculation approaches for getting several paths simultaneously using quantum algorithm. Vector logical operations are used for choosing one path from several solutions due to high performance of hardware in case of vector logical operations. Combination of these approaches gives the opportunity to find shortest path with high performance in short time.

7. References

[1] M. Heiligman. "Quantum algorithms for lowest weight paths and spanning trees in complete graphs", *Quantum Physics*, Cornell University, Cornell, 2003, pp. 10-19.

[2] M. Bondarenko, V. Hahanov, Y. Litvinova. "Logic associative processor structure", *Automatics and tele-mechanics*, Kharkiv, 2012, pp. 71-92

[3] V. Hahanov, W. Gharibi, Y. Litvinova, S. Chumachenko. "Information analysis infrastructure for diagnosis", *Information an int. interdisciplinary journal*, Tokyo. 2011, pp. 2419-2433. Camera-ready was prepared in Kharkov National University of Radio Electronics Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

> Approved for publication: 11.09.2013. Format 60×841/8. Relative printer's sheets: 52. Circulation: 200 copies. Published by SPD FL Stepanov V.V. Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозіуму «Схід-Захід Проектування та Діагностування – 2013» Макет підготовлено у Харківському національному університеті радіоелектроніки Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

> Підписано до публікації: 11.09.2013. Формат 60×84¹/₈. Умов. друк. Арк. 52. Тираж: 200 прим. Видано: СПД ФЛ Степанов В.В. Вул. Ак. Павлова, 311, Харків, 61168, Україна