

KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

# **Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012)**

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## EWDTS 2012 CONTACT INFORMATION

Prof. Vladimir Hahanov  
Design Automation Department  
Kharkov National University of Radio Electronics,  
14 Lenin ave,  
Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26  
E-mail: hahanov@kture.kharkov.ua  
Web: www.ewdtest.com/conf/

# 10<sup>th</sup> IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium (EWDTS)** is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
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- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
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- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

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## CONTENTS

An Efficient Fault Diagnosis and Localization Algorithm for Successive-Approximation Analog to Digital Converters <b>Melkumyan T., Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.</b>	15
Application of Defect Injection Flow for Fault Validation in Memories <b>Amirkhanyan K., Davtyan A., Harutyunyan G., Melkumyan T., Shoukourian S., Vardanian V., Zorian Y.</b>	19
SSBDDs and Double Topology for Multiple Fault Reasoning <b>Raimund Ubar, Sergei Kostin, Jaan Raik</b>	23
Self Compensating Low Noise Low Power PLL design <b>Vazgen Melikyan, Armen Durgaryan, Ararat Khachatryan, Manukyan Hayk, Eduard Musaelyan</b>	29
Optimization Considerations in QCA Designs <b>Zahra NajafiHaghi, Marzieh Mohammadi, Behjat Forouzandeh, Zainalabedin Navabi</b>	33
Implementation of Address-Based Data Sorting on Different FPGA Platforms <b>Dmitri Mihhailov, Alexander Sudnitson, Valery Sklyarov, Ioulia Skliarova</b>	38
Comparison of Model-Based Error Localization Algorithms for C Designs <b>Urmaz Repinski, Jaan Raik</b>	42
Synthesis of Clock Trees for Sampled-Data Analog IC Blocks <b>Bilgiday Yuce, Seyrani Korkmaz, Vahap Baris Esen, Fatih Temizkan, Cihan Tunc, Gokhan Guner, I. Faik Baskaya, Iskender Agi, Gunhan Dundar, H. Fatih Ugurdag</b>	46
Experiences on the road from EDA Developer to Designer to Educator <b>H. Fatih Ugurdag</b>	50
Multi-Beam Constant Modulus Adaptive Arrays in Real-Valued Arithmetic <b>Victor I. Djigan</b>	54
Simulation of Total Dose Influence on Analog-Digital SOI/SOS CMOS Circuits with EKV-RAD macromodel <b>Petrosyants K. O., Kharitonov I. A., Sambursky L. M., Bogatyrev V. N., Povarnitcyna Z. M., Drozdenko E. S.</b>	60
Models for Embedded Repairing Logic Blocks <b>Hahanov V.I., Litvinova E.I., Frolov A., Tiecoura Yves</b>	66
Real-time Interconnection Network for Single-Chip Many-Core Computers <b>Harald Richter</b>	72
Invariant-Oriented Verification of HDL-Based Safety Critical Systems <b>Kharchenko V., Konorev B., Sklyar V., Reva L.</b>	76
An Improved Scheme for Pre-computed Patterns in Core-based SoC Architecture <b>Elahe Sadredini, Qolamreza Rahimi, Paniz Foroutan, Mahmood Fathy, Zainalabedin Navabi</b>	80

Synthesis of Moore FSM with transformation of system in CPLD <b>Aleksander Barkalov, Larysa Titarenko, and Sławomir Chmielewski</b>	<b>85</b>
A WSN Approach to Unmanned Aerial Surveillance of Traffic Anomalies: Some Challenges and Potential Solutions <b>David Afolabi, Ka Lok Man, Hai-Ning Liang, Eng Gee Lim, Zhun Shen, Chi-Un Lei, Tomas Krilavičius, Yue Yang, Lixin Cheng, Vladimir Hahanov, and Igor Yemelyanov</b>	<b>91</b>
Synthesis of Qubit Models for Logic Circuits <b>Wajeb Gharibi, Zaychenko S.A., Dahiri Farid, Hahanova Yu.V., Guz O.A., Ngene Christopher Umerah, Adiele Stanley</b>	<b>95</b>
Theory of Optimal Nonlinear Filtering in Infocommunication's Problems <b>Victor V. Panteleev</b>	<b>102</b>
Verification of Specifications in the Language L with respect to Temporal Properties Expressible by GR(1) Formulas <b>Anatoly Chebotarev</b>	<b>110</b>
Properties of code with summation for logical circuit test organization <b>Anton Blyudov, Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov</b>	<b>114</b>
Loop Nests Parallelization for Digital System Synthesis <b>Alexander Chemeris, Julia Gorunova, Dmiry Lazorenko</b>	<b>118</b>
Decreasing the Power Consumption of Content-Addressable Memory in the Dataflow Parallel Computing System <b>Levchenko N.N., Okunev A.S., Yakhontov D.E., Zmejev D.N.</b>	<b>122</b>
WebALLTED: Interdisciplinary Simulator Based on Grid Services <b>Zgurovsky M., Petrenko A., Ladogubets V., Finogenov O., Bulakh B.</b>	<b>126</b>
Malfunctions Modeling of Converters and Homogeneous-chain Distributed Structure Devices <b>Artur Gulin, Zhanna Sukhinets</b>	<b>130</b>
On structure of quasi optimal algorithm of analogue circuit designing <b>Zemliak A., Michua A., Markina T.</b>	<b>134</b>
A Neuro-Fuzzy Edge Based Spectrum Sensing Processor for Cognitive Radios <b>Mohammadreza Baharani, Mohammad Aliasgari, Mohammadreza {Najafi, Jamali}, Hamid Noori</b>	<b>138</b>
Qubit Model for Solving the Coverage Problem <b>Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas, Eshetie Abebech Mandefro</b>	<b>142</b>
PDF testability of the circuits derived by special covering ROBDDs with gates <b>Matrosova A., Nikolaeva E., Kudin D., Singh V.</b>	<b>146</b>
Compositional Microprogram Control Unit with Operational Automaton of Transitions <b>Alexander Barkalov, Roman Babakov, Larisa Titarenko</b>	<b>151</b>
Observability Calculation of State Variable Oriented to Robust PDFs and LOC or LOS Techniques <b>Matrosova A., Ostanin S., Melnikov A., Singh V.</b>	<b>155</b>

Low-Voltage Low-Power 2.5 GHz Linear Voltage Controlled Ring Oscillator <b>Hayk H Dingchyan</b>	<b>161</b>
High Speed IC Output Buffer with Reduced Power Consumption <b>Karine Movsisyan</b>	<b>165</b>
Engineering-Maintenance Methods of the Calculation Service Area Fixed BWA-paths <b>Sergey I. Myshlyakov, Victor V. Panteleev</b>	<b>170</b>
Analyses of two run march tests with address decimation for BIST procedure <b>Ireneusz Mrozek, Svetlana V. Yarmolik</b>	<b>176</b>
Design of Area Efficient Second Order Low Pass Analog Filter <b>Andranik Hovhannisyan</b>	<b>180</b>
Power Consumption Analysis of Content-Addressable Memories <b>Levchenko N.N., Okunev A.S., Yakhontov D.E.</b>	<b>183</b>
IC Physical Design Optimization Due to Effects of Device Physical Geometries <b>Avag Sargsyan</b>	<b>187</b>
System-on-Chip FPGA-Based GNSS Receiver <b>Alexander Fridman, Serguey Semenov</b>	<b>190</b>
Testware and Automatic Test Pattern Generation for Logic Circuits <b>Victor Zviagin</b>	<b>196</b>
Artificial Neural Network for Software Quality Evaluation Based on the Metric Analysis <b>Oksana Pomorova, Tetyana Hovorushchenko</b>	<b>200</b>
Self-Compensation of Influence of Parasitic Gate-Drain Capacitances of CMOS Transistors in Analog Microcircuitry <b>Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov</b>	<b>204</b>
Hash-based Detection of OFDM Watermarking Symbol for Radiotelephone Identification <b>Aleksandr V. Shishkin, Aleksandr A. Lyashko</b>	<b>208</b>
A Novel Wideband Circular Ring DGS Antenna Design for Wireless Communications <b>Rakesh Sharma, Abhishek Kandwal, Sunil Kumar Khah</b>	<b>211</b>
Universal technique of the analysis of round-off noise in digital filters with arbitrary structure described by topological matrixes <b>Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev</b>	<b>215</b>
Hardware Reduction for Compositional Microprogram Control Unit Dedicated for CPLD Systems <b>Barkalov A., Titarenko L., Smolinski L.</b>	<b>219</b>
Conservative Finite-difference Scheme for the Problem of Laser Pulse Propagation in a Medium with Third-order Dispersion <b>Vyacheslav A. Trofimov, Anton D. Denisov</b>	<b>225</b>
A Four Bit Low Power 165MSPS Flash-SAR ADC for Sigma-Delta ADC Applications <b>Hasan Molaei, Khosrow Hajsadeghi</b>	<b>229</b>
Matrix Implementation of Moore FSM with Nonstandard Presentation of State Codes <b>Titarenko L., Hebda O.</b>	<b>233</b>

Alowpower1.2GS/s4-bitflashADCin0.18mCMOS <b>Mohammad Chahardori, Mohammad Sharifkhani, Sirous Sadughi</b>	<b>237</b>
Symmetrical Differential Stages on CMOS Transistors with Circuits of Self-Compensation and Cancellation <b>Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov</b>	<b>241</b>
Lower Bound of Error in AOA Based Passive Source Localization Using Single Moving Platform <b>Hejazi F., Norouzi Y., Nayebi M.M.</b>	<b>245</b>
A Design for Testability Technique for Quantum Reversible Circuits <b>Joyati Mondal, Debesh K. Das, Dipak K. Kole, Hafizur Rahaman</b>	<b>249</b>
A Flexible Design for Optimization of Hardware Architecture in Distributed Arithmetic based FIR Filters <b>Fazel Sharifi, Saba Amanollahi, Mohammad Amin Taherkhani, Omid Hashemipour</b>	<b>253</b>
Models for Quality Analysis of Computer Structures <b>Murad Ali Abbas, Chumachenko S.V., Hahanova A.V., Gorobets A.A., Priymak A.</b>	<b>258</b>
Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology <b>Daniel Foty, Bruce Smith, Saurabh Sinha, Michael Schröter</b>	<b>264</b>
Sampling Theorem for Finite Duration Signal in Limited Frequency Band <b>Gamlet S. Khanyan</b>	<b>270</b>
SiGe HBT Performance Modeling after Proton Radiation Exposure <b>Konstantin Petrosyants, Maxim Kozhukhov</b>	<b>274</b>
Classical Models of Test used in Advanced Electronics Quality Assurance <b>Surendra Batukdeo</b>	<b>278</b>
The Use of Natural Resources for Increasing a Checkability of the Digital Components in Safety-Critical Systems <b>Drozd A., Kharchenko V., Antoshchuk S., Drozd J., Lobachev M., Sulima J.</b>	<b>283</b>
New version of Automated Electro-Thermal Analysis in Mentor Graphics PCB Design System <b>Petrosyants K.O., Kozyenko P.A., Kharitonov I.A., Sidorov A.V., Chichkanov Y. N.</b>	<b>289</b>
An Approach to Testing of Planar Integrated Antennas in Frequency Range of 5–7 GHz <b>Aleksandr Timoshenko, Ksenia Lomovskaya, Victor Barinov, Andrey Tikhomirov</b>	<b>293</b>
Optimal project solution decision making in telecommunication systems using multicriteria optimization methods <b>Valery Bezruk, Alexander Bukhanko</b>	<b>298</b>
Software implementation and debugging of forward error correction codes <b>Alexey Smirnov, Danila Migalin, Ilya Muravyev, Leonid Pertsev</b>	<b>303</b>
Architecture of Built-In Self-Test and Recovery Memory Chips <b>Andrienko V.A., Moamar Daa, Ryabtsev V.G., Utkina T.Yu.</b>	<b>307</b>
The methods of exclusion of variables in symbolic time models of linear periodically time-variable circuit <b>Yuriy Shapovalov, Dariya Smal</b>	<b>311</b>

Two-Component Encoding of Approximating Picture Pixels in Telecommunication Facilities <b>Barannik V., Dodukh A., Safronov R.</b>	<b>315</b>
Development of parameterized cell using Cadence Virtuoso <b>Vadim Borisov</b>	<b>319</b>
Simulation Methods of Diffusion Alloying Process by Means of Taurus TSUPREM-4 Programme <b>Lagunovich N.L., Borzdov V.M.</b>	<b>321</b>
Control and Diagnosis by Complexity Indicators of System Functioning Process <b>Tverdokhlebov V.A.</b>	<b>323</b>
Features of the Transfer of Information with Different Reliability in a Single Channel <b>Alexander Bakhtin, Leonid Pertsev, Olga Timofeeva</b>	<b>327</b>
Construction of Signals with Controlled Peak-Factor <b>Koshevyy V. M., Dolzhenko D.O.</b>	<b>330</b>
The Effective Method of Space Filtering of Noise in Rayleigh Communication Channel with the Adaptive Antenna <b>Maistrenko G. V., Rybalko A. M., Shokalo V. M., Strelnitskiy A. A.</b>	<b>333</b>
A New Structure for Interconnect Offline Testing <b>Somayeh Sadeghi-Kohan, Shahrzad Keshavarz, Farzaneh Zokaee, Farimah Farahmandi, Zainalabedin Navabi</b>	<b>336</b>
Researching of Mathematical Models Based on Optimal Control Approaches for Congestion Control in Telecommunication Network <b>Lemeshko A.V., Semenyaka M.V.</b>	<b>341</b>
Higher Order Propagation Modes Error and Its Compensation <b>Zaichenko O. B., Klyuchnyk I. I., Martynenko L. G.</b>	<b>345</b>
Strategy of analyzing most common algorithms for path finding in discrete labyrinth using software statistic data collector <b>Krasnov Evgeniy, Dmitry Bagaev</b>	<b>349</b>
Method of Implementation of Technology of Orders Based Transparent Parallelizing for Solving Computationally Complex Problems on Cluster <b>Vitaliy D. Pavlenko, Viktor V. Burdejnyj, Sergey V. Pavlenko</b>	<b>353</b>
Scheduling Tests for 3D SoCs with Temperature Constraints <b>Indira Rawat, Gupta M.K., Virendra Singh</b>	<b>356</b>
Automated application mapping into Network-on-Chip topologies <b>Bykov S. O.</b>	<b>360</b>
MIMO Radar with Phase-coded waveforms <b>Amirsadegh Roshanzamir, Bastani M. H.</b>	<b>363</b>
BBN-based Approach For Assessment of Smart Grid And Nuclear Power Plant Interaction <b>Eugene Brezhnev, Vyacheslav Kharchenko</b>	<b>367</b>
Design, Test and Fault Detection in QCA 4-to-1 Multiplexer <b>Zahra NajafiHaghi, Behjat Forouzandeh</b>	<b>374</b>

The Evaluation of Statistical Characteristics of the Retransmission Meter Signal Frequency and Initial Phase on the Basis of VHDL-model <b>Dmitry A. Velychko, Iegor I. Vdovychenko</b>	<b>378</b>
A Research of Heuristic Optimization Approaches to the Test Set Compaction Procedure Based On a Decomposition Tree for Combinational Circuits <b>Valentina Andreeva, Kirill A. Sorudeykin</b>	<b>382</b>
Power Reduction of 7T Dual-Vt SRAM Cell Using Forward Body Biasing <b>Sahba Sabetghadam Jahromi, Raziye Bounik</b>	<b>388</b>
VLSI: An Investigation into Electromagnetic Signatures (EMS) for Non-Invasive Testing and Signal-integrity Verification <b>Kadim HJ, Coulibaly L. M.</b>	<b>392</b>
Secure Data over GSM based on Algebraic Codebooks <b>Kazemi R., Nashtaali D., Boloursaz M., Behnia F.</b>	<b>397</b>
Simulation of Telecommunication Channel Using Volterra Model <b>Vitaliy D. Pavlenko, Viktor O. Speransky</b>	<b>401</b>
Extracting Complete Set of Equations to Analyze VHDL-AMS Descriptions <b>Arezoo Kamran, Vahid Janfaza, and Zainalabedin Navabi</b>	<b>405</b>
A Data Modem for GSM Adaptive Multi Rate Voice Channel <b>Boloursaz M., Hadavi A. H., Kazemi R., Behnia F.</b>	<b>409</b>
Trends and prospects of development of techniques for extracting acoustic sounding information of the atmospheric boundary layer <b>Klyuchnik I., Panchenko A., Umyarov R.</b>	<b>413</b>
Decision-Making in Robotics and Adaptive Tasks <b>Tsybmal A.M., Bronnikov A.I.</b>	<b>417</b>
Design of Nonvolatile Memory Based on Magnetic Tunnel Junction for Special Electronic Systems <b>Aleksandr Kostrov, Vladislav Nelayev, Viktor Stempitsky, Anatoly Belous, Arkady Turtsevich</b>	<b>421</b>
Improving the Dependability of a Water Supply System via a Multi-Agent based CPS <b>Teodora Sanislav, Liviu Miclea, Paolo Prinetto</b>	<b>425</b>
Cyber Security Lifecycle and Assessment Technique for FPGA-based I&C Systems <b>Illiashenko Oleg, Kharchenko Vyacheslav, Kovalenko Andriy</b>	<b>432</b>
FPGA Technologies in Medical Equipment: Electrical Impedance Tomography <b>Perepelitsyn Artem, Shulga Dmitry</b>	<b>437</b>
A Trend-based Design Space Exploration of Multi-core Systems Using Regression Modeling <b>Fazeleh Hajari Taheri, Omid Fatemi</b>	<b>441</b>
Synchronous Rectifiers Enable High Efficiency for Buck-Boost Converter <b>Yurii Shynkarenko and Igor Klyuchnyk</b>	<b>445</b>

Test Data Compression Strategy While Using Hybrid-BIST methodology <b>Elmira Karimi, Mohammad Hashem Haghbayan and Mahmood Tabandeh</b>	<b>449</b>
Self-Adaptive Mobile Wireless Hotspot Zones <b>Yanovsky M., Kharchenko V., Gorbenko A.</b>	<b>454</b>
The Systolic Compositions of Two-dimensional and Multidimensional Lattice Filters for Space-Time Signal Processing <b>David I. Lekhovyt'skiy, Andrii V. Semeniaka, and Dmytro S. Rachkov</b>	<b>458</b>
Power Efficient Implementation of Homogenous Multi-Core Processors <b>Aram Poghosyan</b>	<b>462</b>
Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices <b>Vladimir Hahanov, Karyna Mostova, Oleksandr Paschenko</b>	<b>465</b>
Improved Scaling-Free CORDIC algorithm <b>Leonid Moroz, Taras Mykytiv, Martyn Herasym</b>	<b>470</b>
Coding Tangible Component of Transforms to Provide Accessibility and Integrity of Video Data <b>Barannik V.V., Hahanova A.V., Krivonos V.N.</b>	<b>475</b>
Review of the botnet detection techniques <b>Oleg Savenko, Sergiy Lysenko, Kryshchuk Andrii</b>	<b>479</b>
MEMS Intellect Multiprobes Contacting Devices for Electrical Checking-up of Multilayers Commutative Boards and BGA/CSP Electronic Components <b>Nevliudov I.Sh., Palagin V.A., Razumov-Frizjuk E.A., Zharikova I.V.</b>	<b>483</b>
Internet of Things: A Practical Implementation based on a Wireless Sensor Network Approach <b>Michele Mercaldi, Andrea D'Oria, Davide Murru, Hai-Ning Liang, Ka Lok Man, Eng Gee Lim, Vladimir Hahanov, Mischenko Alexander</b>	<b>486</b>
Investigation of EM Wave Propagation of the Wireless Capsule in Human Body <b>Eng Gee Lim, Zhao Wang, Jin Hui Chen, Tammam Tillo, Ka Lok Man</b>	<b>490</b>
Using pyroelectric detectors in the design of temperature measuring devices <b>Bondarenko A.Yu., Klyuchnik I.I.</b>	<b>494</b>
Transaction Level Model of Embedded Processor for Vector-Logical Analysis <b>Irina V. Hahanova, Volodymyr Obrizan, Alexander Adamov, Dmitry Shcherbin</b>	<b>497</b>
Embedded Intelligent Control Systems on the Basis of Elementary Fuzzy-Logic Cells <b>Dontsova A., Vassiliev A.E.</b>	<b>502</b>
Interconnection Analysis of the Integral Reliability Characteristics of the Monoergative Computer System and User's Competency <b>Krivoulya G., Shkil A., Kucherenko D.</b>	<b>505</b>
System approach to determination of ADC parameters <b>Knyshev Ivan</b>	<b>511</b>
Methodological Aspects of Complex Ecological Estimation of Man-Caused Territory State and Mathematical Modelling of Processes in a Environment System <b>Kozulia T. V., Sharonova N. V. , Emelianova D. I., Kozulia M.M.</b>	<b>514</b>

Method for “Failure on Demand” Latent Faults Diagnosis of NPP Safety Control Systems <b>Gerasymenko K.E.</b>	<b>519</b>
Informational Saturation of Noise Signals <b>Kolodiy Z. A., Kolodiy A.Z.</b>	<b>523</b>
The Positional Structural-Weight Coding of the Binary View of Transformants <b>Barannik V., Krasnoruckiy A., Hahanova A.</b>	<b>525</b>
Synchronization of a Fuzzy Automata <b>Speranskiy Dmitriy</b>	<b>529</b>
Models for SoC Infrastructure of Radio Frequency Identification with Code-Division Multiple <b>Filippenko I.V., Hahanova I.V., Filippenko I.O, Maksimov M., Chugurov I.</b>	<b>535</b>
Factorization of Rhythmograms Parametric Spectra on the Base of Multiplicative Linear Prediction Models <b>Nataliia V. Kudriavtseva, Iryna O. Fil</b>	<b>538</b>
Logi-Thermal Analysis of Digital Circuits Using Mixed-Signal Simulator Questa ADMS <b>Petrosyants K.O., Rjabov N.I.</b>	<b>541</b>
Method of Hybrid Regression Analysis in the Calibration Experiments <b>Ordinartseva N. P.</b>	<b>545</b>
<b>Keynotes speeches and Invited Reports</b>	<b>548</b>
<b>AUTHORS INDEX</b>	<b>554</b>

# Models for SoC Infrastructure of Radio Frequency Identification with Code-Division Multiple

Filippenko I.V., Hahanova I.V., Filippenko I.O, Maksimov M., Chugurov I.

Computer Engineering Faculty, Kharkov National University of Radioelectronics,  
Kharkov, Ukraine, hahanov@kture.kharkov.ua

## Abstract

*Application of the direct spread spectrum technology to radio frequency identification system for solving problems of speed, reliability and electromagnetic compatibility is considered. The models of systems-on-chips for tag and reader of RFID systems with code-division multiple, based on technology of direct spread spectrum, are proposed.*

## 1. Introduction

Nowadays, the most promising technology for automatic identification is radio frequency identification (RFID), when data is transferred without any mechanical contact between the devices. Contactless identification technologies correspond to all the requirements of computer control systems, where recognition and registration of objects are realized in real time.

Modern infrastructure of RFID systems (Fig. 1) involves readers, tags and various protocols, which allow integrating the system in global information networks and variety of applications of enterprise levels. In addition, the infrastructure can also include other devices, such as bar code readers, input/output devices, for instance label printers, motion detectors, photo sensors.

Transponder and reader communicate with each other by using radio frequency channel. Wireless data channel is the most vulnerable link in the system, because the data transmitted by radio channel, may be intercepted. Also the problem of electromagnetic compatibility of various wireless devices is important. This paper is devoted to solving this problem through the creation of models of systems-on-chips for tag and reader by using the direct spread spectrum technology (CDMA).

## 2. SoC models for tag and reader

To implement this system the communication protocol for reader and tag, structural SoC models of tag and reader are developed.

Functional circuit of the tag model involves the following blocks (Fig. 2):

- RF module for transmitting and receiving information from the reader;
- memory ROM (storage of control software and volatile data, such as serial number);
- memory block EEPROM or FRAM (application data);
- control unit, implemented on a microcontroller;
- block for generating pseudorandom sequence (PRS), encoding and decoding useful information, and generator of response time delay;
- sensors (for instance, temperature, humidity);
- I-IP module, focused to solving the design quality problem and increasing yield.

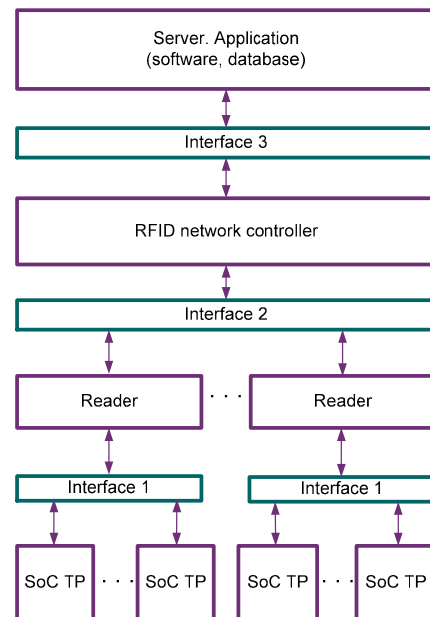


Fig.1. Infrastructure of RFID system

Functional circuit of the reader involves the following blocks (Fig. 3):

- RF module for transmitting and receiving information from the tag;
- memory ROM for storing control software;

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- The block diagram illustrates the internal components and connections of the MC control unit. On the left, a vertical stack of four blocks represents external components: ROM, EEPROM or RAM, Sensors, and a pair of Vcc and I-P blocks. Each of these is connected to a central vertical block labeled 'MC control unit' via a bidirectional arrow. To the right of the MC control unit is a dashed green box containing three blocks: a Decoder, a Generator of response time delay, and a Coder. The MC control unit has bidirectional connections to the Decoder and the Coder, and a unidirectional connection to the Generator of response time delay. The Generator of response time delay has a unidirectional connection to the Coder. To the right of the dashed box is a vertical block labeled 'RF path'. The MC control unit has a bidirectional connection to the RF path, and the Coder also has a bidirectional connection to it. Finally, the RF path is connected to an antenna, represented by three concentric circles.

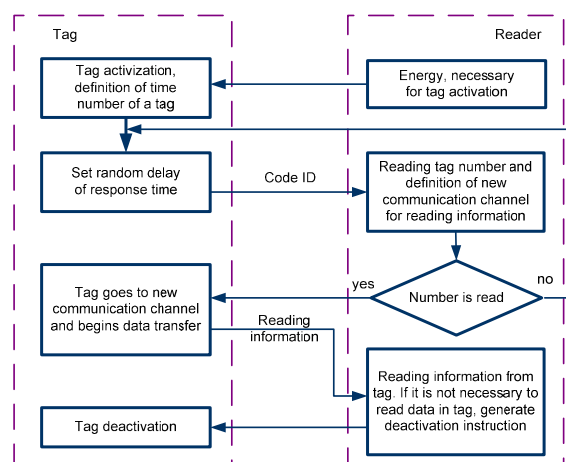
The diagram illustrates the system architecture, showing the flow of signals between various components. The components are organized into several functional blocks:

- RF path**: The input path for the system, connected to the synchronization and processing short PRS channel and the channel for generating control signals of tag.
- Synchronization and processing short PRS channel**: A channel that receives signals from the RF path and processes them for synchronization.
- Synchronization unit**: A unit that receives signals from the synchronization and processing short PRS channel and the channel for generating control signals of tag, and outputs signals to the channels for data processing of 'long' PRSs.
- Channels for data processing of 'long' PRSs**: A set of channels (labeled 'long' PRS1, ..., 'long' PRSn) that receive signals from the synchronization unit and output them to the IMC control unit.
- Channel for generating control signals of tag**: A channel that receives signals from the RF path and the IMC control unit, and outputs signals to the synchronization unit.
- IMC control unit**: A central control unit that receives signals from the channels for data processing of 'long' PRSs and the channel for generating control signals of tag, and outputs signals to the I/O interface, RAM, ROM, and I-IP.
- I/O interface**: An interface that connects the IMC control unit to the RAM, ROM, and I-IP.
- RAM**: Random Access Memory, connected to the I/O interface.
- ROM**: Read-Only Memory, connected to the I/O interface.
- I-IP**: Input-Output Processor, connected to the I/O interface.

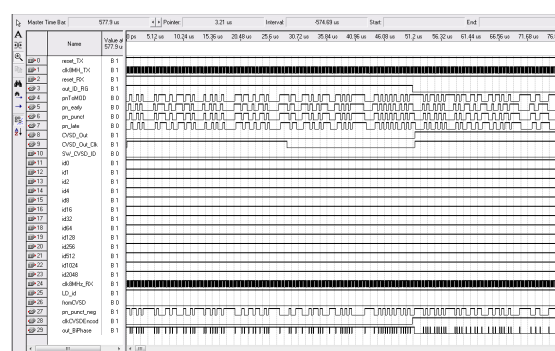
The diagram shows the flow of signals between these components, indicating the system's architecture and the flow of data and control signals.

The protocol for communicating reader and tag, which allows minimizing the time of tag identification, and provide concurrent reading information from a set of tags, is shown in Fig. 4.

functioning of blocks. The simulation results are shown in Fig. 5.



**Fig. 4. Flowchart of the protocol for data communication tag-reader**



**Fig. 5. Timing of the project**

## 4. Conclusion

A model of RFID infrastructure with code division multiple is first proposed. It is based on the technology of direct spread spectrum, which gives the ability to reuse the spectrum with high structural and informational secrecy, increased noise immunity and reliability of information transfer. An infrastructure model allows solving the problem of electromagnetic compatibility of the system with radio devices for different purposes.

SoC models of tag and reader, as well as the protocol of their interaction in RFID infrastructure with code division multiple through direct extension of the spectrum are developed.

Functional simulation and verification of proposed models of tag and reader have confirmed the correctness of the logical operation of the developed system.

## 10. References

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Вул. Ак. Павлова, 311, Харків, 61168, Україна