

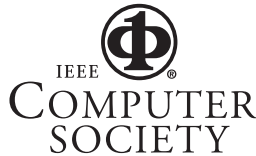
KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'09)

Copyright © 2009 by The Institute of Electrical and Electronics Engineers, Inc.

SPONSORED BY

IEEE Computer Society Test Technology Technical Council



Moscow, Russia, September 18 – 21, 2009

IEEE EAST-WEST DESIGN AND TEST SYMPOSIUM 2009 ORGANISING COMMITTEE

General Chairs

V. Hahanov – Ukraine
Y. Zorian – USA

General Vice-Chairs

D. Bikov - Russia
R. Ubar – Estonia

Program Chairs

S. Shoukourian – Armenia
D. Speranskiy – Russia

Program Vice-Chairs

M. Renovell – France
Z. Navabi – Iran

Steering Committee

M. Bondarenko – Ukraine
V. Hahanov – Ukraine
R. Ubar – Estonia
Y. Zorian – USA

Publicity Chairs

R. Ubar - Estonia
S. Mosin – Russia

Program Committee

E. Evdokimov – Ukraine
A. Chaterjee – USA
E. Gramatova – Slovakia
S. Hellebrand – Germany
A. Ivanov – Canada
M. Karavay – Russia
V. Kharchenko – Ukraine
K. Kuchukjan – Armenia
A. Matrosova – Russia
V. Melikyan - Armenia

O. Novak – Czech Republic

A. Orailoglu – USA
Z. Peng – Sweden
A. Petrenko – Ukraine
P. Prinetto – Italy
J. Raik – Estonia
A. Romankevich – Ukraine
A. Ryjov – Russia
R. Seinauskas – Lithuania
S. Sharshunov – Russia
A. Singh – USA
J. Skobtsov – Ukraine
A. Stempkovsky – Russia
V. Tverdokhlebov – Russia
V. Vardanian – Armenia
V. Yarmolik – Byelorussia
E. J. Aas – Norway
J. Abraham – USA
M. Adamski – Poland
A. Barkalov – Poland
R. Bazylevych – Ukraine
V. Djigan – Russia
A. Drozd – Ukraine
W. Kuzmicz – Poland

Organizing Committee

S. Chumachenko – Ukraine
N. Kulbakova – Ukraine
V. Obrizan – Ukraine
A. Kamkin – Russia
K. Petrosyanz – Russia
A. Sokolov – Russia
Y. Gubenko – Russia
M. Chupilko – Russia
E. Litvinova – Ukraine
O. Guz – Ukraine
G. Markosyan – Armenia

EWDTS CONTACT INFORMATION

Prof. Vladimir Hahanov
Design Automation Department
Kharkov National University of Radio Electronics,
14 Lenin ave,
Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26
E-mail: hahanov@kture.kharkov.ua
Web: www.ewdtest.com/conf/

7th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)
Moscow, Russia, September 18-21, 2009

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design

- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television
- Signal and Information Processing in RF and Communication

The symposium is organized by Kharkov National University of Radio Electronics, in cooperation with Tallinn University of Technology, Institute for System Programming of RAS, and Moscow Institute of Electronics and Mathematics. It is sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Cadence, JTAG Technologies, Kaspersky Lab, Synopsys, Mentor Graphics, Tallinn Technical University, Donetsk Institute of Road Transport, Moscow Institute of Electronics and Mathematics, Virage Logic, Echostar, Aldec, Teprocomp, DataArt Lab.



CONTENTS

Simulation-based Verification with APRICOT Framework using High-Level Decision Diagrams Maksim Jenihhin, Jaan Raik, Anton Chepurov, Raimund Ubar.....	13
Fault-Detection Capability Analysis of a Hardware-Scheduler IP-Core in Electromagnetic Interference Environment J. Tarrillo, L. Bolzani, F. Vargas, E. Gatti, F. Hernandez, L. Fraigi.....	17
Hardware Reduction in FPGA-Based Compositional Microprogram Control Units Barkalov A.A., Titarenko L.A., Miroshkin A.N.....	21
Optimization of Control Units with Code Sharing Alexander A. Barkalov, Larisa A. Titarenko, Alexander S. Lavrik.....	27
SAT-Based Group Method for Verification of Logical Descriptions with Functional Indeterminacy Liudmila Cheremisinova, Dmitry Novikov.....	31
MicroTESK: Automation of Test Program Generation for Microprocessors Alexander Kamkin.....	35
Verification Methodology Based on Algorithmic State Machines and Cycle-Accurate Contract Specifications Sergey Frenkel and Alexander Kamkin.....	39
Coverage Method for FPGA Fault Logic Blocks by Spares Vladimir Hahanov, Eugenia Litvinova, Wajeb Gharibi, Olesya Guz.....	43
Testing and Verification of HDL-models for SoC components Vladimir Hahanov, Irina Hahanova, Ngene Christopher Umerah, Tiecoura Yves.....	48
The Model of Selecting Optimal Test Strategy and Conditions of ICs Testing During Manufacturing Sergey G. Mosin.....	54
A Technique to Accelerate the Vector Fitting Algorithm for Interconnect Simulation Gourary M.M., Rusakov S.G., Ulyanov S.L., Zharov M.M.....	59
Frequency Domain Techniques for Simulation of Oscillators Gourary M.M., Rusakov S.G., Stempkovsky A.L., Ulyanov S.L., Zharov M.M.....	63
Distributed RLC Interconnect: Estimation of Cross-coupling Effects H.J. Kadim, L.M. Coulibaly.....	67
Constrained-Random Verification for Synthesis: Tools and Results D. Bodean, G. Bodean, O. Ghincul.....	71
Discussion on Supervisory Control by Solving Automata Equation Victor Bushkov, Nina Yevtushenko, Tiziano Villa.....	77
Generalized Faulty Block Model for Automatic Test Pattern Generation F. Podyablonsky, N. Kascheev.....	80
Self Calibration Technique of Capacitor's Mismatching For 1.5 Bit Stage Pipeline ADC Vazgen Melikyan, Harutyun Stepanyan.....	84
Applied Library of Adaptive Lattice Filters for Nonstationary Signal Processing Victor I. Djigan.....	87
On-chip Measurements of Standard-Cell Propagation Delay S.O. Churayev, B.T. Matkarimov, T.T. Paltashev.....	93
FPGA FFT Implementation S.O. Churayev, B.T. Matkarimov.....	96

Reconfiguration and Hardware Agents in Testing and Repair of Distributed Systems G. Mois, I.Ştefan, Sz. Enyedi, L. Miclea.....	99
Symmetrization in Digital Circuit Optimization Natalia Eliseeva, Jie-Hong R. Jiang, Natalia Kushik, Nina Yevtushenko.....	103
Embedded Processor Power Reduction via Power aware Custom Instruction Selection Hoda Ahmadinejad, Saeed Safari, and Hamid Noori.....	107
Level Quantization Effects in Digital Signal Processing by Discrete Fourier Transform Method Gamlet S. Khanyan.....	111
A New Paradigm in Design of IIR Digital Filters Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev.....	115
Evolutionary Approach to Test Generation of Sequential Digital Circuits with Multiple Observation Time Strategy Yu. A. Skobtsov, V. Yu. Skobtsov.....	119
SMT-based Test Program Generation for Cache-memory Testing Evgeni Kornikhin.....	124
Critical Path Test Generation in Asynchronous QDI Circuits Fahime Khoramnejad, Hossein Pedram.....	128
Model-driven & Component-based Development Method of Multi-core Parallel Simulation Models Nianle Su, Wenguang Yu, Hongtao Hou, Qun Li and Weiping Wang.....	135
Minimizing of Number of Discrete Device's Controllable Points Dmitriy Speranskiy, Ekaterina Ukolova.....	142
VHPI-compatible Simulation and Test Generation System Dmitriy Speranskiy, Ivan Ukolov.....	147
Fault Tolerant HASH function with Single Element Correction and Minimum Delay Overhead Costas A. Argyrides, Carlos A. Lisboa, Dhiraj K. Pradhan, Luigi Carro.....	151
Analysis of the Control Vector Optimal Structure for a Minimal-Time Circuit Optimization Process A.M. Zemliak, M.A. Torres, T.M. Markina.....	156
Parallel Simulation of Boolean Functions by Means of GPU Włodzimierz Bielecki, Alexander Chemeris, Svetlana Reznikova.....	162
Two-Criterial DSSS Synchronization Method Efficiency Research Kharchenko H.V., Tklich I.O., Vdovychenko Y.I.....	165
An Efficient March Test for Detection of All Two-Operation Dynamic Faults from Subclass S_{av} Gurgen Harutyunyan, Hamazasp Avetisyan, Valery Vardanian, Y. Zorian.....	175
Large and Very Large-scale Placement Bazylevych R.P., Bazylevych L.V., Shcherb'yuk I.F.....	179
An Educative Brain-Computer Interface Kirill Sorudeykin.....	183
Time-Hardware Resource: A Criterion of Efficiency of Digital Signal Search and Detection Devices Alexander Fridman.....	187
A New Principle of Dynamic Range Expansion by Analog-to-Digital Converting Elina A. Biberdorf, Stanislav S. Gritsutenko, Konstantin A. Firsanov.....	193
FREP: A Soft Error Resilient Pipelined RISC Architecture Viney Kumar, Rahul Raj Choudhary, Virendra Singh.....	196

System Remote Control of the Robotized Complex - Pegas Dmitry Bagayev, Evsyakov Artem	200
Use of Predicate Categories for Modelling of Operation of the Semantic Analyzer of the Linguistic Processor Nina Khairova, Natalia Sharonova	204
Methodological Aspects of Mathematical Modelling of Processes in a Corporate Ecological System Kozulia T.V., Sharonova N.V.	208
Getting Optimal Load Distribution Using Transport-Problem-Based Algorithm Yuri Ladyzhensky, Viatcheslav Kourktchi	212
Dialogue-based Optimizing Parallelizing Tool and C2HDL Converter Steinberg B., Abramov A., Alymova E., Baglij A., Guda S., Demin S., Dubrov D., Ivchenko A., Kravchenko E., Makoshenko D., Molotnikov Z., Morilev R., Nis Z., Petrenko V., Povazhniy A., Poluyan S., Skiba I., Suhoverkhov S., Shapovalov V., Steinberg O., Steinberg R.	216
The System for Automated Program Testing Steinberg B., Alimova E., Baglij A., Morilev R., Nis Z., Petrenko V., Steinberg R.	218
Development of the University Computing Network for Integrated Circuit Design Atkin E., Volkov Yu., Garmash A., Klyuev A., Semenov D., Shumikhin V.	221
Increase in Reliability of On-Line Testing Methods Using Natural Time Redundancy Drozd A., Antoshchuk S., Martinuk A., Drozd J.	223
An Algorithm of Carrier Recovery for Modem with M-ary Alphabets APK-Signals without PLL Victor V. Panteleev	230
At Most Attainable of Lengths a Symmetrical Digital Subscriber Line on xDSL-technologies: Engineering-Maintenance Methods of the Calculation Victor V. Panteleev, Nikolay I. Tarasov	234
New Approach to ADC Design Stanislav S. Gritsutenko	240
Simulation of Radiation Effects in SOI CMOS Circuits with BSIMSOI-RAD Macromodel K.O. Petrosjanc, I.A. Kharitonov, E.V. Orekhov, L.M. Sambursky, A.P. Yatmanov	243
Thermal Design System for Chip- and Board-level Electronic Components K.O. Petrosjanc, I.A. Kharitonov, N.I. Ryabov, P.A. Kozynko	247
TCAD Modeling of Total Dose and Single Event Upsets in SOI CMOS MOSFETs K.O. Petrosjanc, I.A. Kharitonov, E.V. Orekhov, A.P. Yatmanov	251
Reduction in the number of PAL Macrocells for Moore FSM implemented with CPLD A. Barkalov, L. Titarenko, S. Chmielewski	255
Schematic Protection Method from Influence of Total Ionization Dose Effects on Threshold Voltage of MOS Transistors Vazgen Melikyan, Aristakes Hovsepyan, Tigran Harutyunyan	260
5V Tolerant Power clamps for Mixed-Voltage IC's in 65nm 2.5V Salicided CMOS Technology Vazgen Melikyan, Karen Sahakyan, Armen Nazaryan	263
Analysis and Optimization of Task Scheduling Algorithms for Computational Grids Morev N. V.	267
A Low Power and Cost Oriented Synthesis of the Common Model of Finite State Machine Adam Klimowicz, Tomasz Grzes, Valeri Soloviev	270

Comparison of Survivability & Fault Tolerance of Different MIP Standards Ayesha Zaman, M.L. Palash, Tanvir Atahary, Shahida Rafique	275
Hardware Description Language Based on Message Passing and Implicit Pipelining Dmitri Boulytchev, Oleg Medvedev	279
V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non-Linear Analog Circuits Suraj Sindia, Virendra Singh, Vishwani Agrawal	283
GA-Based Test Generation for Digitally-Assisted Adaptive Equalizers in High-Speed Serial Links Mohamed Abbas, Kwang-Ting (Tim) Cheng, Yasuo Furukawa, Satoshi Komatsu, Kunihiro Asada	287
Between Standard Cells and Transistors: Layout Templates for Regular Fabrics Mikhail Talalay, Konstantin Trushin, Oleg Venger	293
On-Chip Optical Interconnect: Analytical Modelling for Testing Interconnect Performance H J Kadim	300
The Problem of Trojan Inclusions in Software and Hardware Alexander Adamov, Alexander Saprykin	304
Design methods for modulo $2n+1$ multiply-add units C. Efstathiou, I. Voyiatzis, M. Prentakis	307
Geometrical Modeling and Discretization of Complex Solids on the Basis of R-functions Gomenyuk S.I., Choporov S.V., Lisnyak A.O.	313
Selective Hardening: an Enabler for Nanoelectronics Ilia Polian and John P. Hayes	316
Parameterized IP Infrastructures for Fault-Tolerant FPGA-Based Systems: Development, Assessment, Case-Study Kulanov Vitaliy, Kharchenko Vyacheslav, Perepelitsyn Artem	322
Generating Test Patterns for Sequential Circuits Using Random Patterns by PLI Functions M. H. Haghbayan, A. Yazdanpanah, S. Karamati, R. Saeedi, Z. Navabi	326
A New Online BIST Method for NoC Interconnects Elnaz Koopahi, Zainalabedin Navabi	332
Low Cost Error Tolerant Motion Estimation for H.264/AVC Standard M. H. Sargolzaie, M. Semsarzadeh, M. R. Hashemi, Z. Navabi	335
Method of Diagnosing FPGA with Use of Geometrical Images Epifanov A.S.	340
Performance Analysis of Asynchronous MIN with Variable Packets Length and Arbitrary Number of Hot-Spots Vyacheslav Evgrafov	344
System in Package. Diagnosis and Embedded Repair Vladimir Hahanov, Aleksey Sushanov, Yulia Stepanova, Alexander Gorobets	348
Technology for Faulty Blocks Coverage by Spares Hahanov Vladimir, Chumachenko Svetlana, Litvinova Eugenia, Zakharchenko Oleg, Kulbakova Natalka	353
The Unicast Feedback Models for Real-Time Control Protocol Babich A.V., Murad Ali Abbas	360
Algebra-Logical Repair Method for FPGA Logic Blocks Vladimir Hahanov, Sergey Galagan, Vitaliy Olchovoy, Aleksey Priymak	364

The Method of Fault Backtracing for HDL - Model Errors Searching Yevgeniya Syrevitch, Andrey Karasyov, Dariya Kucherenko	369
Handling Control Signals for the Scan Technology Olga Lukashenko, Dmitry Melnik, Vladimir Obrizan	373
Robust Audio Watermarking for Identification and Monitoring of Radiotelephone Transmissions in the Maritime Communication Vitaliy M. Koshevyy, Aleksandr V. Shishkin	377
An Interconnect BIST for Crosstalk Faults based on a Ring LFSR Tomasz Garbolino, Krzysztof Gucwa, Andrzej Hlawiczka, Michał Kopeć	381
Generation of Minimal Leakage Input Vectors with Constrained NBTI Degradation Pramod Subramanyan, Ram Rakesh Jangir, Jaynarayan Tudu, Erik Larsson, Virendra Singh	385
Very Large-Scale Intractable Combinatorial Design Automation Problems – Clustering Approach for High Quality Solutions Roman Bazylevych and Lubov Bazylevych	389
Flexible and Topological Routing Roman Bazylevych and Lubov Bazylevych	390
An Algorithm for Testing Run-Length Constrained Channel Sequences Oleg Kurmaev	391
Constructing Test Sequences for Hardware Designs with Parallel Starting Operations Using Implicit FSM Models Mikhail Chupilko	393
Redundant Multi-Level One-Hot Residue Number System Based Error Correction Codes Somayyeh Jafarali Jassbi, Mehdi Hosseinzade, Keivan Navi	397
Parallel Fault Simulation Using Verilog PLI Mohammad Saeed Jahangiry, Sara Karamati, Zainalabedin Navabi	401
IEEE 1500 Compliant Test Wrapper Generation Tool for VHDL Models Sergey Mikhtonyuk, Maksim Davydov, Roman Hwang, Dmitry Shcherbin	406
Early Detection of Potentially Non-synchronized CDC Paths Using Structural Analysis Technique Dmitry Melnik, Olga Lukashenko, Sergey Zaychenko	411
An Editor for Assisted Translation of Italian Sign Language Nadereh Hatami, Paolo Prinetto, Gabriele Tiotto	415
Architecture Design and Technical Methodology for Bus Testing M.H. Haghbayan, Z. Navabi	419
Assertion Based Verification in TLM AmirAli Ghofrani, Fatemeh Javaheri, Zainalabedin Navabi	424
Flash-memories in Space Applications: Trends and Challenges Maurizio Caramia, Stefano Di Carlo, Michele Fabiano, Paolo Prinetto	429
Design Experience with TLM-2.0 Standard: A Case Study of the IP Lookup LC-trie Application of Network Processor Masoom Hashemi, Mahshid Sedghi, Morteza Analoui, Zainalabedin Navabi	433
Test Strategy in OSCI TLM-2.0 Mina Zolfy, Masoom Hashemi, Mahshid Sedghi, Zainalabedin Navabi and Ziaeddin Daeikozekanani	438
Synthesizing TLM-2.0 Communication Interfaces Nadereh Hatami, Paolo Prinetto	442

Advanced Topics of FSM Design Using FPGA Educational Boards and Web-Based Tools Alexander Sudnitson, Dmitri Mihhailov, and Margus Kruus	446
A Mixed HDL/PLI Test Package Nastaran Nemati, Majid Namaki-Shoushtari, Zainalabedin Navabi	450
Testing Methodologies on Communication Networks Nadereh Hatami, Paolo Prinetto, Gabriele Tiotto, Paola Elia	456
A Novel High Speed Residue to Binary Converter Design Based on the Three-Moduli Set $\{2n, 2n+1+1, 2n+1-1\}$ Muhammad Mehdi Lotfinejad, Mohammad Mosleh and Hamid Noori	460
Performance Evaluation of SAT-Based ATPG on Multi-Core Architectures Alejandro Czuto, Bernd Becker, Ilia Polian	463
Intelligent Testbench Automation and Requirements Tracking Ivan Selivanov, Alexey Rabovoluk	471
Iterative Sectioning of High Dimensional Banded Matrices Dmytro Fedasyuk, Pavlo Serdyuk, Yuriy Semchyshyn	476
Estimating Time Characteristics of Parallel Applications in Technology of Orders Based Transparent Parallelizing Vitalij Pavlenko, Viktor Burdeinyi	480
Phase Pictures Properties of Technical Diagnostics Complex Objects Tverdokhlebov V.A.	483
Information Technology of Images Compression in Infocommunication Systems Alexander Yudin, Natalie Gulak, Natalie Korolyova	486
Technology of Cascade Structural Decoding Leonid Soroka, Vladimir Barannik, Anna Hahanova	490
Technology of the Data Processing on the Basis of Adaptive Spectral- Frequency Transformation of Multiadical Presentation of Images Vladimir Barannik, Sergey Sidchenko, Dmitriy Vasiliev	495
Compression Apertures Method - Color Different Images Konstantin Vasyuta, Dmitry Kalashnik, Stanislav Nikitchenko	499
Isotopic Levels Architectural Presentation of Images Relief Vladimir Barannik, Alexander Slobodyanyuk	502
Method and Mean of Computer's Memory Reliable Work Monitoring Utkina T.Yu., Ryabtsev V.G.	505
Extended Complete Switch as Ideal System Network Mikhail F. Karavay and Victor S. Podlazov	513
Image Compression: Comparative Analysis of Basic Algorithms Yevgeniya Sulema, Samira Ebrahimi Kahou	517
Networked VLSI and MEMS Designer for GRID Petrenko A.I.	521
Path Delay Fault Classification Based on ENF Analysis Matrosova A., Nikolaeva E.	526
COMPAS – Advanced Test Compressor Jiří Jeníček, Ondřej Novák	532
INVITED TALKS	538
AUTHORS INDEX	545

Early Detection of Potentially Non-synchronized CDC Paths Using Structural Snalysis Technique

Dmitry Melnik, Olga Lukashenko, Sergey Zaychenko

Design Automation Department, Kharkov National University of Radio Electronics, Ukraine

E-mail: explorer@inbox.ru

Abstract

The number of independent clock domains found on the typical today's device is continuously growing. According to the latest industry research, the average number of clock domains on a single device is >15—20 and it becomes higher and higher from day to day. The CDC-related design flaws are also growing exponentially, appearing to be very dangerous as the roots of intermittent chip failures (can be found only in the silicon). Static CDC verification is considered as one of the first de-facto steps in today's SoC design methodology; only static techniques can work as soon as the RTL starts taking shape [1]. This paper discusses early detection of potentially missing synchronizers on clock domain crossing paths, using structural static analysis.

1. Introduction

The sections of logic elements that driven by clocks coming from different sources are called clock domains [2]. The signals that interface between asynchronous clock domains are called the clock domain crossing (CDC) signals (see Figure 1). The DATA_A signal is considered as an asynchronous signal into the receiving clock domain (no constant phase and time relationship exists between CLK_A and CLK_B).

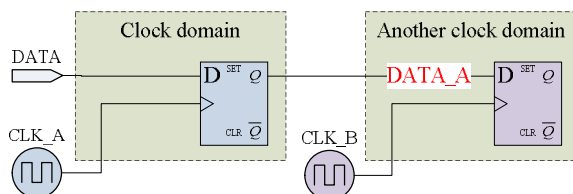


Figure 1. Clock domains and CDC signal

The nature of CDC bugs is intermittent; it simply means that a test suite can be successfully completed on a chip in the morning, but the same tests will complete with errors for the same chip in the afternoon [3]. Consider the simplest flip-flop example: such a flip-flop is located anywhere in the chip; the data signal for this flip-flop comes from the domain #A but the clock signal — from the domain #B... so whenever the setup or hold condition is violated, the flip-flop can go to one or to zero and it cannot be predicted (see Figure 2).

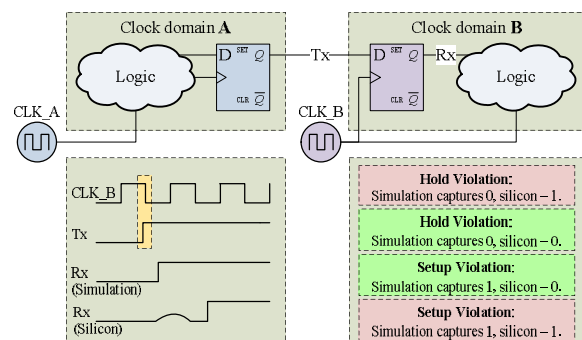


Figure 2. Possible metastability effects

The metastability term is used to describe what happens in digital circuits when the clock and data inputs of a flip-flop change values at approximately the same time. As shown in the Figure 2, it leads to the flip-flop output oscillating and not settling to a value within the appropriate delay window [4]. Such glitches happen in every design wherein two or more discrete systems communicate (the number of clock domains is greater than two).

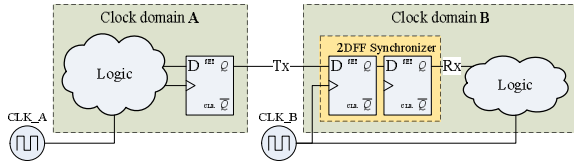


Figure 3. Simplest synchronizer (2 DFF in series)

Designers have actually found a solution to this and most of them is aware that metastability can be controlled using synchronizers on CDC signals (outputs of metastable registers are isolated so that the metastable value does not propagate to downstream logic) [5, 6]. Whenever there is a domain crossing signal, two flip-flops are placed one next to the other clocked by the same clock (see Figure 3). Such a synchronization structure decreases the MTBF (see Formula 1, where the f_{clk} – clock frequency, f_{in} – input signal frequency, t_d – duration of critical time window) from hours to thousands years [4].

$$MTBF = \frac{1}{f_{clk} \times f_{in} \times t_d}$$

Formula 1. Mean (average) time between failures.

Recent trends have been in favor of using static analysis tools [1]. But the biggest disadvantage of this approach is that it comes pretty late in the game — after the design has been synthesized, and the gate-level netlist is available (finding a CDC at this stage — which needs to be fixed — could set the design schedule totally off). So there is a need in static analysis tool that:

1. Performs lightweight synthesis (netlist synthesis emulation) directly from the RTL description — alongside with Verilog, VHDL or SystemVerilog compilation;
2. Reports domain crossing paths with potentially missing synchronizers, thus providing an obvious advantage in the form of early checking.

2. Automatic clock domains extraction

Clock domains extraction with further synchronizers detection is illustrated by the dataflow that is shown in the Figure 4. It involves several steps, starting with the compilation of the RTL description and creation of the database with netlist elements (lightweight synthesis), proceeding with special attributes assignment and their propagation through a design hierarchy (global clocks detection), and further

manipulations with global clocks (clock domains look up).

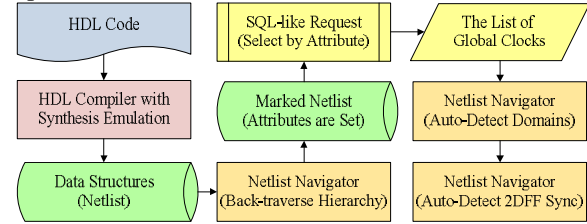


Figure 4. Clock domains and sync. detection dataflow

Detect global clocks in a design. Attributes are distributed through the design hierarchy (netlist): “DESIGN_CLOCK” attribute is back-propagated from each flip-flop clock pin. Since all the netlist elements were added to the database, it further can be used for selection by the particular attribute(s) presence (SQL-like request).

- The back-propagation of the attribute is terminated on the storage elements (flip-flops and latches) and tri-states. While back-propagation is stopped, it means that the signal which feeds the flip-flop clock pin is not an external input signal and thus it cannot be considered as a global clock.
- However, if the attribute reaches an external input pin (passes only through combinatorial logic, buffers and inverters), it is considered as a global clock – added to the list of global clocks (see Figure 5).

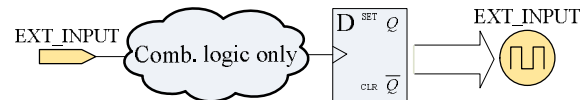


Figure 5. Global clock auto-detection

Extract clock domains. Clock domains can be detected when the list of global clocks is available; each global clock creates at least one separate clock domain. In order to detect clock domains, global clocks should be propagated through the design hierarchy (external input pins marked with the “DESIGN_CLOCK” attribute):

- Transparent logic. Combinatorial logic, latches and tri-states that happen on the attribute propagation path are considered as transparent objects.
- Flip-flops consideration. Each flip-flop that happens on the propagation path is added to the appropriate clock domain if

“DESIGN_CLOCK” attribute reaches its clock input pin; if a flip-flop clock pin is driven by the output of another flip-flop which already belongs to a clock domain, the flip-flop is also added to the same clock domain (Figure 6)

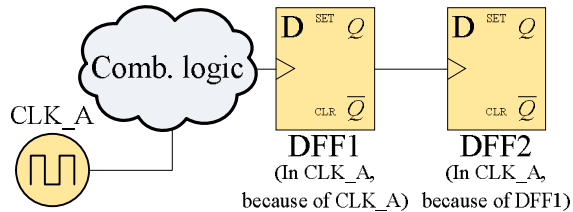


Figure 6. Flip-flops added to corresp. domains

- Derived domains. If two or more clock signals are propagated through the same combinatorial logic or multiplexer then the output of this logic or multiplexer derives a new clock signal that correspondingly results in a new clock domain for subsequent connections (see Figure 7). Also if a clock signal is connected to the multiplexer select pin then the output of this multiplexer derives a new clock signal.

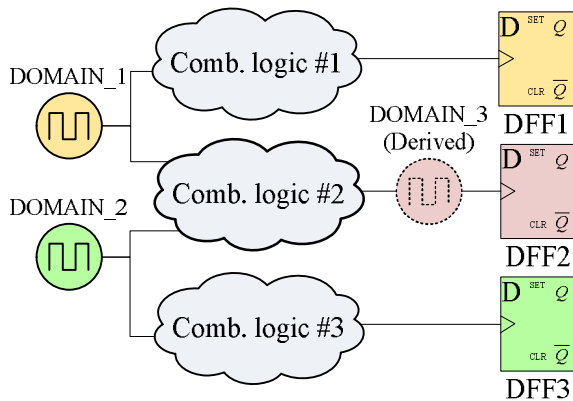


Figure 7. Derived domain

Design is considered to be in a single clock domain if clock domains were not detected.

3. Detecting potentially non-synchronized CDC paths

While the netlist is marked with clock domain-related attributes, the data about each flip-flop membership is available, it becomes possible to go

further and detect synchronized and potentially non-synchronized CDC paths.

Detect 2DFF synchronizers. In order to be considered as 2DFF synchronizer, a pair of flip-flops should comply with the following restrictions:

1. Each flip-flop should receive the data only from the same clock domain (correct case – FF#1 receives data from domain A and transmits it to FF#2; incorrect case – FF#1 receives data from domain A, FF#2 receives data from domain B).
2. The outputs of the first and second flip-flops should not be connected to external design output(s) (in each case, the propagation should be blocked by non-clock input of another flip-flop(s) from the same domain).

It should be noted, that for some very high speed designs, the MTBF of a two-flop synchronizer is too short and a third flop is added to increase the MTBF to a satisfactory duration of time [7].

The paths which does not pass through a 2DFF synchronizer upon arrival into the new clock domain can be considered as potentially non-synchronized and reported as the design rule violations (synchronization errors class, see Figure 8).

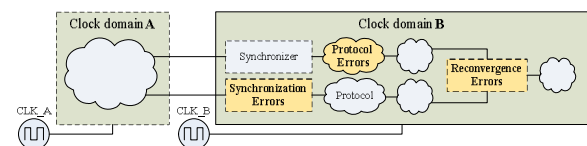


Figure 8. Synchronization and other CDC errors

4. Conclusion

Proposed structural analysis technique includes building of a netlist of the target design (lightweight synthesis is performed alongside with compilation) and performing further static analysis on this netlist. The novelty of the approach concerns propagation of various attributes through a design hierarchy: once the database with “netlist element”—“attribute(s)” relations is prepared, it can be used for SQL-like selections by attribute. The result of analysis is a summary of CDC paths in the design where the synchronization is potentially missing. Proposed technique deals only with the first of CDC problems list which can be detected with static analysis [8]:

1. Missing and incorrectly implemented synchronizers.
2. Correctly implemented synchronizer.

3. Complex synchronizers that require protocol verification.
4. Potential reconvergence problems.

To perform more complete CDC verification, formal analysis techniques should be used alongside with structural analysis (see Figure 9).

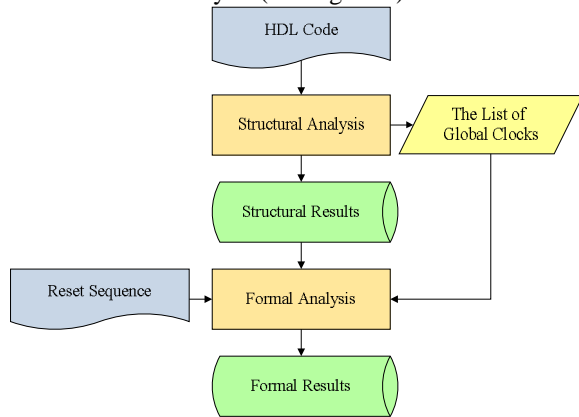


Figure 9. Structural and formal analysis

During the structural verification stage, it is possible to generate monitors for CDC transfer protocols. At the stage of formal verification [9], a simple reset sequence is used and cycle-based design analysis is performed (requires knowledge about clock periods of the asynchronous clocks). While a monitor is proven, it means that CDC protocol is followed.

5. References

[1] Sanjay Churiwala and Sapan Garg of Atrenta, and Chirag Gupta and Paresh Joshi of Texas Instruments, "Verification of

Clock Domain Crossing in SoCs: Part One — Tools and Needs". Downloadable from www.chipdesignmag.com.

[2] Cadence technical paper, "Clock Domain Crossing. Closing the Loop on Clock Domain Functional Implementation Problems". Downloadable from w2.cadence.com/whitepapers/cdc_wp.pdf.

[3] Mentor Graphics technical webinar, "Finding and Eliminating CDC Errors with 0-In CDC Verification". Downloadable from

www.mentor.com/player/2007/zero_in_cdc/index.html

[4] Michelle Lange of Mentor Graphics, "Automating Clock-Domain Crossing Verification for DO-254 (and other Safety-Critical) Designs". Downloadable from www.do254.com/documents/Papers/Mentor_CDC-for-DO254.pdf.

[5] Clifford E. Cummings, SNUG-2001, "Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs". Downloadable from www.sunburst-design.com/papers.

[6] Tai Ly, "The Need for an Automated Clock Domain Crossing Verification Solution". Downloadable from www.mentor.com/fv.

[7] Clifford E. Cummings, SNUG-2008, "Clock Domain Crossing (CDC) Design & Verification Techniques Using SystemVerilog". Downloadable from www.sunburst-design.com/papers.

[8] Ping Yeung of Mentor Graphics, "Five Steps to Quality CDC Verification". Downloadable from www.mentor.com/products/fv/techpubs/.

[9] Mentor Graphics, "Formal Verification User Guide V2.5". Feb 2007.

Camera-ready was prepared in Kharkov National University of Radio Electronics

by Dr. Svetlana Chumachenko

Lenin ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 31.08.2009. Format 60×84¹/₈.

Relative printer's sheets: . Circulation: 150 copies.

Published by SPD FL Stepanov V.V.

Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозиуму «Схід-Захід Проектування та Діагностування – 2009»

Макет підготовлено у Харківському національному університеті радіоелектроніки

Редактори: Володимир Хаханов, Світлана Чумаченко

Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 31.08.2009. Формат 60×84¹/₈.

Умов. друк. арк. . Тираж: 150 прим.

Видано: СПД ФЛ Степанов В.В.

Вул. Ак. Павлова, 311, Харків, 61168, Україна