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Abstract. One of the problems in the testbench generation for extended finite state machines (EFSM) is existence of internal variables. In fact the usage of these variables in the condition of transition increases real quantity of states by orders. Even for a variable with bit length 20 it leads to the state explosion problem [1]. But for some control unit it is possible to make redesign of the project by including state variables to state register. The transformation algorithm contains phases of state splitting, transition splitting, unreachable (dead) state reduction and equivalent states minimization. The results of such transformation can be used for design analysis, optimization, validation, verification, synthesis and implementation.

1. Introduction

This paper was motivated by author’s work in the project ASFTest – a testbench generator for Aldec finite state machines[2]. Graphical user interface used in state-of-the-art software allows to create environment for design entry with finite state machine abstract usage. Such form of design description is used in many software and hardware design tools like StatedCAD, FPGA Advantage, Stateworks, Stateflows, etc. The algorithm is described in the graphical way using the extended FSM notation. VHDL is chosen as target language. Synthesis is made by Xilinx synthesis tool which is included in Xilinx Webpack environment [3]. The target device is CPLD CoolRunner II.

2. Design entry

The quantity of the explicit states in the model A is 8. Quantity of bits in internal variables is 6. The total quantity of the states including implicit states in internal variables is \(8 \times 2^6 = 512\).

3. State splitting

After state splitting based on the boolean variable quantity of explicit states are multiplied by 2.

4. Dead state reduction

After design transformation we can see unreachable (dead) states. They are redundant for design and can be removed. It’s easy to find 2 kinds of dead states: without incoming transition and with unfeasible condition of transition.

5. Equivalent states reduction

Is is possible to make equivalent states reduction (hold_state and hold_state_ace in example). After transformation we obtain 12 explicit states and \(12 \times 2^5 = 384\) total states.
6. Design verification

The model behavior does not change during these transformations and we can use the same testbench for verification. But ATPG can give different sequence for Model A, B, and C depending on the quantity of the explicit states.

FSM testbenches metrics. After state splitting and reduction FSM contains 172 states and 562 transitions.

HDL level testbench metrics using CodeCoverage tool for different settings of FSM to VHDL transformation.

7. Implementation

Implementation for DEVICE XCR3032XL-5VQ44 using Xilinx synthesis tool (XST) gives different results for model A and B.

Model A. The best implementation result

<table>
<thead>
<tr>
<th>RESOURCE</th>
<th>AVAIL.</th>
<th>USED</th>
<th>UTILIZATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Inputs</td>
<td>4</td>
<td>1</td>
<td>25.00%</td>
</tr>
<tr>
<td>Global C-Terms</td>
<td>4</td>
<td>0</td>
<td>0.00%</td>
</tr>
<tr>
<td>Func Blocks</td>
<td>2</td>
<td>2</td>
<td>100.00%</td>
</tr>
<tr>
<td>I/O Pins</td>
<td>32</td>
<td>14</td>
<td>43.75%</td>
</tr>
<tr>
<td>Macro Cells</td>
<td>32</td>
<td>9</td>
<td>28.13%</td>
</tr>
<tr>
<td>PLA P-Terms</td>
<td>96</td>
<td>79</td>
<td>82.30%</td>
</tr>
<tr>
<td>PLA S-Terms</td>
<td>32</td>
<td>16</td>
<td>50.00%</td>
</tr>
<tr>
<td>Block C-Terms</td>
<td>16</td>
<td>0</td>
<td>0.00%</td>
</tr>
<tr>
<td>Fbk Nands</td>
<td>0</td>
<td>0</td>
<td>0.00%</td>
</tr>
</tbody>
</table>

Model B. The best implementation result

<table>
<thead>
<tr>
<th>RESOURCE</th>
<th>AVAIL.</th>
<th>USED</th>
<th>UTILIZATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Macro Cells</td>
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<td>13</td>
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<tr>
<td>Registers</td>
<td>32</td>
<td>9</td>
<td>28.13%</td>
</tr>
<tr>
<td>PLA P-Terms</td>
<td>96</td>
<td>60</td>
<td>62.50%</td>
</tr>
<tr>
<td>PLA S-Terms</td>
<td>32</td>
<td>13</td>
<td>40.63%</td>
</tr>
</tbody>
</table>

8. Summary

State splitting can be used for small control unit designs for design minimization, analysis, implementation, and testbench generation.

References: