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CONTENTS

HIGH LEVEL FSM DESIGN TRANSFORMATION USING STATE SPLITTING

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Abstract. One of the problems in the testbench generation for extended finite state machines (EFSM) is existence of internal variables. In fact the usage of these variables in the condition of transition increases real quantity of states by orders. Even for a variable with bit length 20 it leads to the state explosion problem [1]. But for some control unit it is possible to make redesign of the project by including state variables to state register. The transformation algorithm contains phases of state splitting, transition splitting, unreachable (dead) state reduction and equivalent states minimization. The results of such transformation can be used for design analysis, optimization, validation, verification, synthesis and implementation.

1. Introduction

This paper was motivated by author's work in the project ASFTest – a testbench generator for Aldec finite state machines[2].

Graphical user interface used in state-of-the-art software allows to create environment for design entry with finite state machine abstract usage. Such form of design description is used in many software and hardware design tools like StatedCAD, FPGA Advantage, Stateworks, Stateflows, etc.

The algorithm is described in the graphical way using the extended FSM notation. VHDL is chosen as target language. Synthesis is made by Xilinx synthesis tool which is included in Xilinx Webpack environment [3]. The target device is CPLD Coollrunner II.

2. Design entry

The quantity of the explicit states in the model A is 8. Quantity of bits in internal variables is 6. The total quantity of the states including implicit states in internal variables is $8 \cdot 2^6 = 512$.

3. State splitting

After state splitting based on the boolean variable quantity of explicit states are multiplied by 2.

4. Dead state reduction

After design transformation we can see unreachable (dead) states. They are redundant for design and can be removed. It's easy to find 2 kinds of dead states: without incoming transition and with unfeasible condition of transition.

5. Equivalent states reduction

Is is possible to make equivalent states reduction (hold_state and hold_state_ace in example). After transformation we obtain 12 explicit states and $12 \cdot 2^5 = 384$ total states.

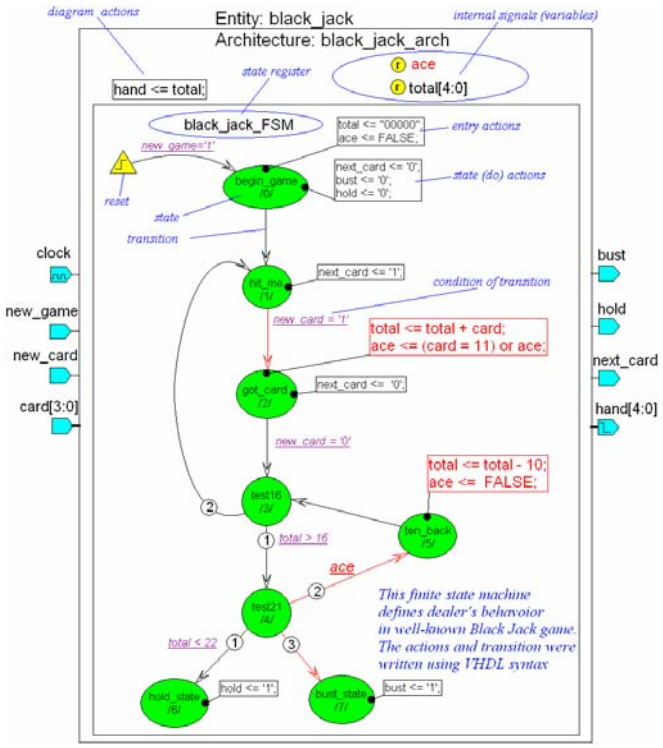

Fig.1. Model A. Initial design of black jack dealer

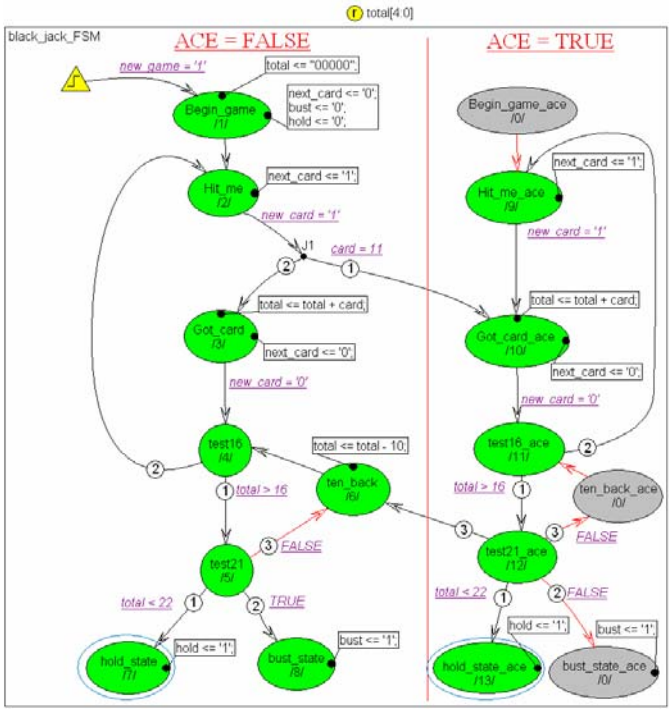

Fig. 2. State splitting based on boolean signal

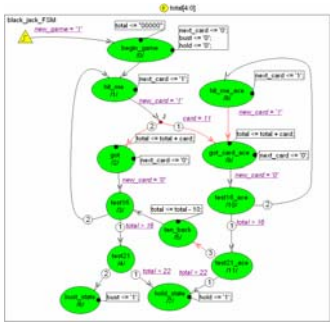

Fig. 3. Model B. Design after splitting and reduction

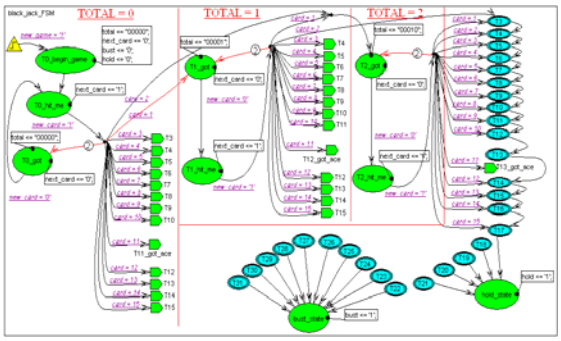

Fig. 3. Model C. Design after splitting on 5-bit signal

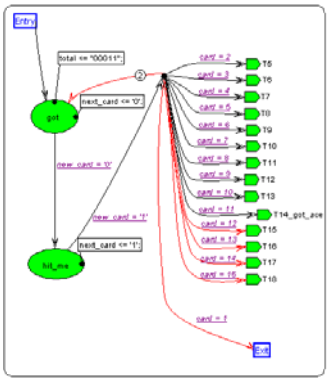

Fig. 4. Model C. Hierarchical state T3

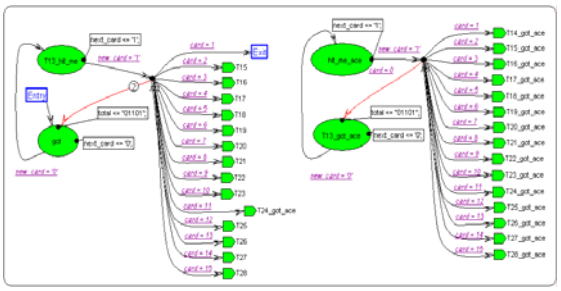

Fig. 5. Model C. Hierarchical state T13

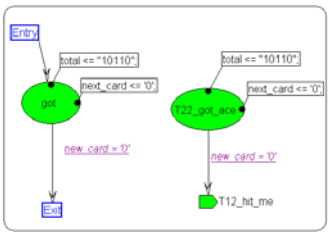

Fig. 6. Model C. Hierarchical state T22

6. Design verification

The model behavior does not change during these transformations and we can use the same testbench for verification. But ATPG can gives different sequence for Model A, B, and C depending on the quantity of the explicit states.

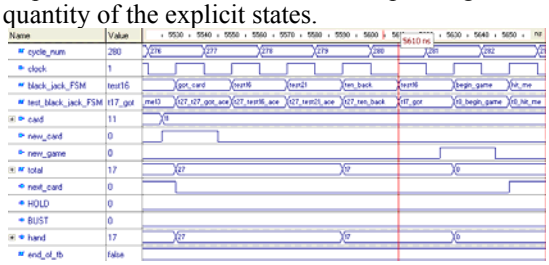

Fig. 7. Waveform with design error

FSM testbenches metrics. After state splitting and reduction FSM containes 172 states and 562 transitions.

Strategy / Metric	All nodes	All vertexes	Reset from all	Unit
States	100	100	100	%
Transitions	32.03	86.12	31.14	%
Test length	280	1927	1144	patterns
Time	0.1	0.9	0.4	seconds
Reset apllied	27	202	172	times

HDL level testbench metrics using CodeCoverage tool for different settings of FSM to VHDL transformation.

Strategy / Template	All nodes	All vertexes	Reset from all	Unit	Lines of code
1-process	48.03	99.92	40.96	%	1629
2-process	59.22	99.93	59.58	%	1653
3-process	67.70	100.00	67.98	%	2093

7. Implementation

Implementation for DEVICE XCR3032XL-5VQ44 using Xilinx synthesys tool (XST) gives different results for model A and B.

Model A. The best implementaton result

Total Device Resource Summary			
RESOURCE	AVAIL.	USED	UTILIZATION
Clock Inputs	4	1	25.00%
Global C-Terms	4	0	0.00%
Func Blocks	2	2	100.00%
I/O Pins	32	14	43.75%
Macro Cells	32	16	50.00%
Registers	32	9	28.13%
PLA P-Terms	96	79	82.30%
PLA S-Terms	32	16	50.00%
Block C-Terms	16	0	0.00%
Fbk Nands	0	0	0.00%

Model B. The best implementaton result

Macro Cells	32	13	40.63%
Registers	32	9	28.13%
PLA P-Terms	96	60	62.50%
PLA S-Terms	32	13	40.63%

8. Summary

State splitting can be used for small control unit designs for design minimization, analysis, implementation, and testbench generation.

References:

1. ***D.A. Stuart, M. Brockmeyer, A.K. Mok, and Farnam Jahanian.*** Simulation-Verification: Biting at the State Explosion Problem. IEEE Trans. on Software Engineering, vol. 27, №7, July 2001.

2. http://www.aldec.com/products/active-hdl/ Active-HDL FPGA verification environment.

3. http://www.xilinx.com/ - Xilinx Webpack man

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