Metastability Testing at FPGA Circuit Design using Propagation Time Characterization

Branka Medved Rogina, Peter Škoda, Karolj Skala, Ivan Michieli

Abstract—**This paper describes the measurement method and experimental technique with advanced instrumentation setup for analysing the metastability behavior and performance measurement of flip-flops used in programmable logic devices. In order to demonstrate this testing approach, the results for metastable characteristics parameters of one FPGA digital circuit fabricated commercially in 90 nm CMOS process are presented. The same test methods can also be used for evaluation of timing reliability in digital circuits as well.**

Index Terms—**FPGA, metastability, testing, propagation time**

I. Introduction

METASTABILITY is a central issue in the synchronization of two or more asynchronous signals. The standard method for accomplishing this task is to employ a D flip-flop (FF) as the synchronizing element. Metastability failure appears if data and clock input signals violate setup and hold times, as the output signal of the FF then becomes unpredictable [1]. The increased size of structural and functional complexity of today's digital circuits, such as FPGAs (Field Programmable Gate Array), has given rise to circuit designs with high numbers of asynchronous clock domains, where metastability problems occur most often, when the signal is transferred between circuitry in unrelated or completely asynchronous clock domains [2]. Concerning the reliability of digital circuit design, metastability is a problem that cannot be avoided It should be noted that manufacturers of digital circuits rarely give information about these parameters.

Different experimental procedures have been employed to accurately determine metastability characteristics, but the number of results cannot be compared because of different excitation and recording methods, so there is no standard test method. The results are very often presented through the MTBF value (Mean Time Between Failure) due to metastability, as an estimate of the average time between instances when signal transfers could cause metastability problems and design failure [3,4].

We have already presented a practical measurement technique to determine the MTBF characteristics of nonprogrammable and programmable logic devices using high accuracy time interval measurement setup [5,6,7]. Here we present a subsequent approach based on integrated propagation time characteristics, using a high speed digital storage oscilloscope for the acquisition, measurement and statistical timing of data analysis of metastable FF in FPGA devices. Although input (IOB) FFs are normally used to synchronize asynchronous input signals, the tests are performed both for FFs located in IOB (Input Logic Block) and CLB (Configurable Logic Block) areas .

II. Characterizing Metastability

A. Metastability equation

It is well known that the input to a synchronizing FF must be stable for a minimum time before the clock edge (setup time t_{SU}) and for a minimum time after the clock edge (hold time t_{HD}), in order to ensure reliable operation. The synchronizer output is then available after a specified clock-to-output propagation time (t_{CO}), as shown in Fig. 1.

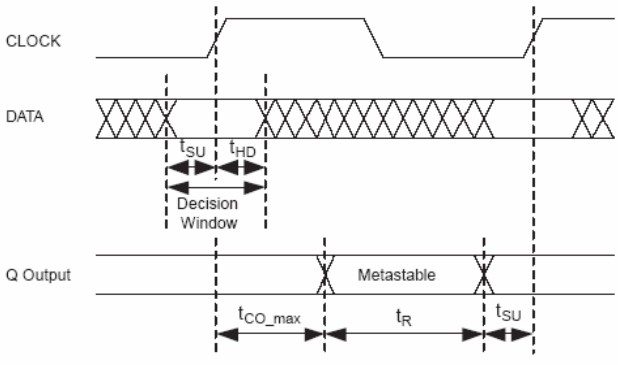

Fig. 1 A synchronizing FF must be stable for a minimum time before the clock edge (setup time t_{SU}) and for a minimum time after the clock edge (hold time t_{HD}), in order to ensure reliable operation

The problem with metastable events is not merely their occurrence, but when the event causes inconsistent values to

Manuscript received December 1, 2010.

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be latched into subsequent flip-flops. One manifestation of metastability behavior is excessive propagation time of this transition [8]. This increased delay will normally cause timing violations in the subsequent (synchronous) circuit if the output has not resolved itself by the time that it must be valid for use, for example, as an input to another stage. Because of the greater densities and more aggressive clocking strategies applied today, FPGAs have become more susceptible to these delay faults [9].

The metastability failure rate is usually calculated using the equation that relates mean time between two failures with operating conditions [10]:

$$\mathrm{MTBF} = \frac{10^{\frac{t_R}{\tau_d}}}{2 \cdot f_c \cdot f_d \cdot w} \qquad (1)$$

where:

- t_R is the resolve time or the maximum time a digital output can remain in a metastable state without causing a synchronization failure,
- w is the metastable window and represents the likelihood that a device enters into a metastable state,
- τ_d is the metastability resolution time constant and describes the speed at which the metastable condition is resolved,
- f_c is the frequency of the system clock,
- f_d is the frequency of the input signal.

Available resolve time is calculated in the following manner:

$$t_R = (1/f_c - t_{CO\_max} - t_{SU}) \qquad (2)$$

Therefore, the amount of resolve time t_R allowed for a device to settle plays a significant role in calculating its failure rate. In our practical measurement technique, we determine device depending characteristics, the metastability resolution time constant τ_d and the metastable window w, so that circuit's failure rate for different resolving time values at specific frequencies of clock and data signals can/may be calculated.

B. Metastability measurement method

Common methods for exploring MTBF use the stimulating data and clock signal out of phase, representing asynchronous signals that are most frequently used in real systems today [11]. However, the probability of an FF going into a metastable state will be higher if the input signal more often violates the setup time or hold time of the FF. Therefore, we use synchronous data and clock input signals to deliberately induce metastability in testing FF. However, it is necessary to consider the following. A MTBF parameter is used to calculate the mean time between synchronization failure events and is valid for random events, input events that are uniformly distributed over the clock period. Since we use a history-dependent method of generating input events, we must take care that it does not affect the data and still obtain the results that correspond to the excitation of random, asynchronous input signals.

As for the analysis of the results, we do not predetermine the time (after the clock signal) at which the output state of an FF is analyzed, as in the LTD (Late Transition Detection) method [11]. We simply measure clock-to-output propagation time at various setup, hold time values and store the data for later processing.

For example, Fig. 2 shows a propagation time characteristic measured for one general purpose FPGA circuit, Xilinx's 90 nm FPGA Spartan-3 within various setup and hold time relationships. It is evident that the clock-to-output propagation time starts to increase (black line) as the time interval between data and clock signals becomes less than 0.2 ns (setup time). At the same time, the number of output signals with increased propagation time but of regular voltage level (logical correct events) decreases (blue line). The largest measured increase in propagation time is 1.3 ns, with only 10 % of transitions occurred. The measurement results correspond to data listed in the manufacturer's specifications [12].

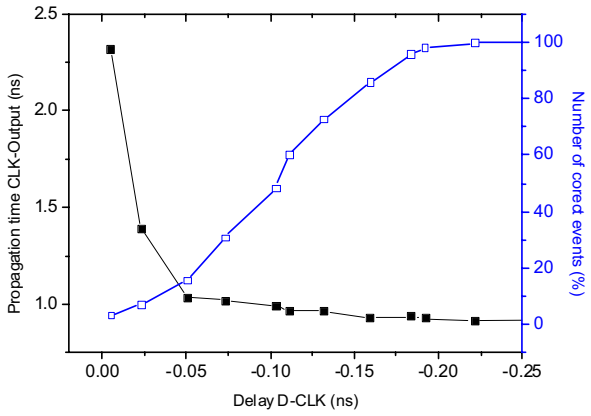

Fig. 2 A propagation time characteristic and number events measured for one general purpose FPGA circuit (Xilinx's 90 nm FPGA Spartan-3) within various setup and hold time relationships

To experimentally determine the metastability resolution time constant τ_d and the metastable window w, the edge of the data signal is set at the centre of the metastable window. This is usually adjusted, so the output signal of a FF favors both high and low logic data equally, corresponding to 50 % logically correct events [1]. (Using this Foley method type of excitation is simpler than the principle used in our original method [5].) The exact number of events is determined by DSO counting, or can be estimated upon the intensity of traces on the oscilloscope screen (as in Fig. 3).

Based on all measured results, it is possible to determine the decay function of this metastable state over time from the histogram of time propagation data. The metastability resolution time constant and the metastable window are calculated by applying the principle described by [13,14].

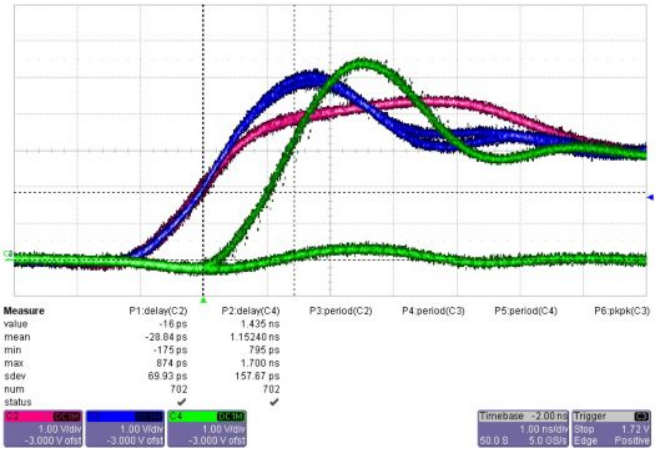

Fig. 3 Digital storage oscilloscope representation of data, clock and output signals waveforms and statistical data of propagation time, for IOB FF in Spartan-3 FPGA

III. Experimental Test Setup and Measurement Results

In our first measurement setup, time intervals are measured based on the start-stop principle, using a TAC (Time-to-Amplitude Converter). The time resolution of this analog method is very high (3.5 ps). Analog methods of time interval measurement give an excellent opportunity to analyze high-speed data signals with ps timing resolution [15]. For determining only the decay of the metastability state, such a sophisticated measurement setup might not always be necessary. Therefore, we propose a metastability test setup based on digital storage oscilloscope (DSO) for data acquisition. The DSO is capable of continuous measured data accumulation, storage and a statistical data mining analysis of the results [7].

The main parts of the measurement setup are shown in Fig. 4.

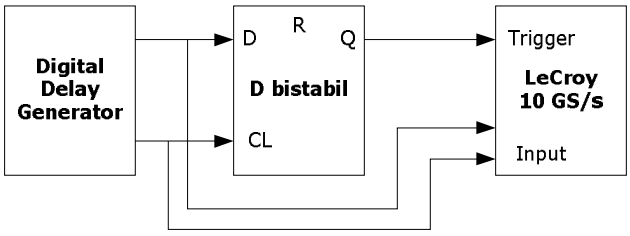

Fig. 4 Experimental metastability test setup based on digital storage oscilloscope for data acquisition

A digital delay generator (Stanford Research DG353) provides programmable clock and data fast pulse input signals for FF under testing. The trigger output signal of the generator is used as an external trigger input for a 10 GS/s digital storage oscilloscope (LeCroy WaveRunner 6100). The resolution of the signal generator (5 ps) is the only sizable limitation of the accuracy of the measurement method.

The logical connection of IOB and CLB test FFs in Spartan-3 FPGA is shown in Fig. 5. In each device, the same implementation tests the IOB and CLB FFs simultaneously.

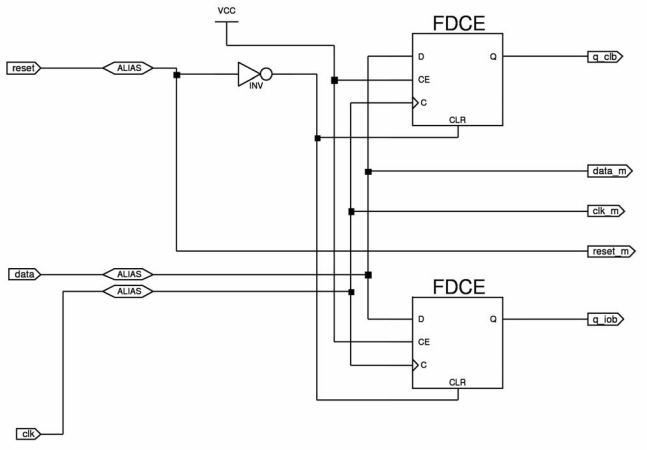

Fig. 5. Logical connection of IOB and CLB test FFs in Spartan-3 FPGA for metastability test

The time waveform diagram of reference signals for metastability test is shown in Fig. 6.

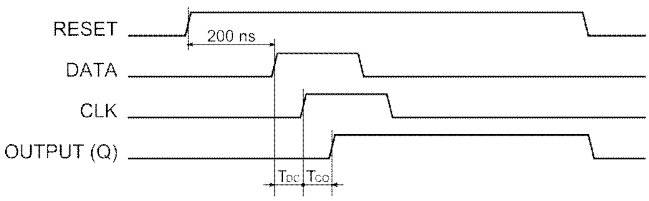

Fig. 6. The time waveform diagram of reference signals for metastability test

A. *Evaluating the metastability parameters*

In order to determine the statistical characteristics of logically correct events, the oscilloscope is triggered by the output signal of tested FF. A characteristic histogram of the measured propagation time of approximately 25 x 10^3 events is presented in Fig. 7. The horizontal time base represents the time from the moment of triggering the oscilloscope "back" to the edge of the clock signal; increasing settling time values are shown "from right to left."

In Fig. 8 the X-axis represents the time from triggering Q output back to the clock edge and, therefore, increasing metastability time is shown from left to right. The value of τ for the metastable region can be measured from the histogram. The slope of the metastable region starts at about -1.0 ns and ends at -1.15 ns. For this instance, τ is about 28 ps and is obtained from the reciprocal of the slope of the histogram. This particular device is quite fast and

metastable events cannot be observed as well as in slower devices.

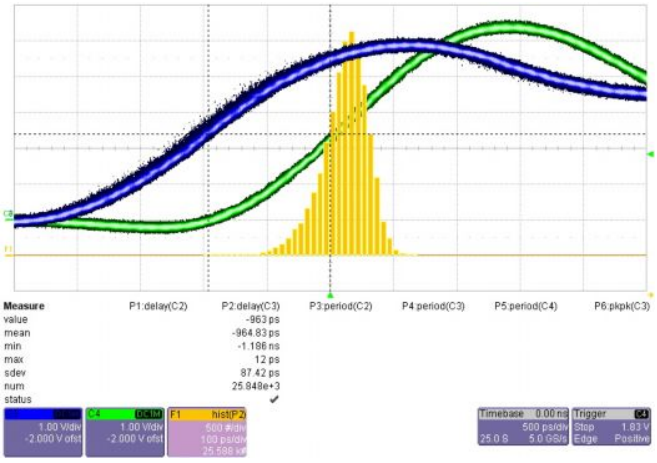

Fig. 7. Digital storage oscilloscope representation of propagation time histogram for IOB FF in Spartan-3 FPGA in metastability test

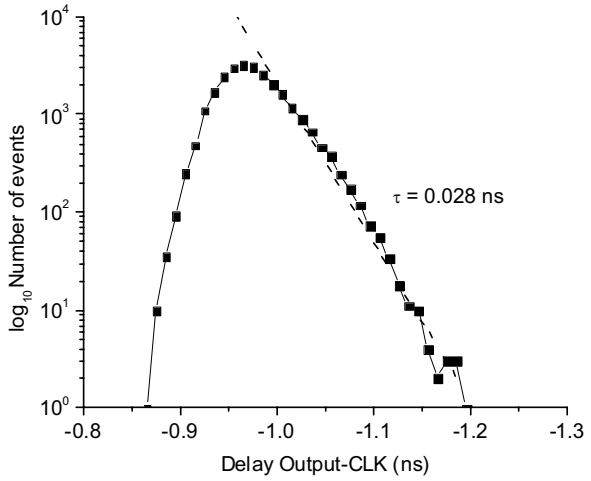

Fig. 8. Determination of resolution time constant τ for IOB FF in Spartan-3 FPGA in metastability test

The width of the metastable window w is determined for different propagation time values from the same histogram. It is first necessary to convert the vertical axis named by numbers of metastable events to a time scale representing the effective size of the metastable window for a given propagation time. In order to make this conversion, it is necessary to locate a point on the vertical axis which can be mapped to a propagation time parameter on the x-axis. Following the procedure in [14], events with normal propagation time (measured value 0.966 ns) are assigned to a metastable window that is equal to setup time (0.21 ns). The width of the metastable window (from t_{SU} to w) is reduced in the same proportion as the number of events (with larger propagation time). This is the basic idea that determines the parameters necessary to calculate the metastable window from the propagation time histogram. By applying this approach to the measured data histogram, metastable window values of 78.75, 7.88 and 0.65 ps are calculated for events with propagation time 50, 120 and 180 ps larger than the normal value. As expected, events with a large increase of propagation time are due to smaller metastable windows. For high speed technologies, like FPGAs, only events that occur as a result of small metastable window lead to "deep" metastability, while those for larger values constitute the area of "deterministic" metastability [13]. The results of these calculations for Spartan-3 FPGA IOB FF are shown in Fig. 9.

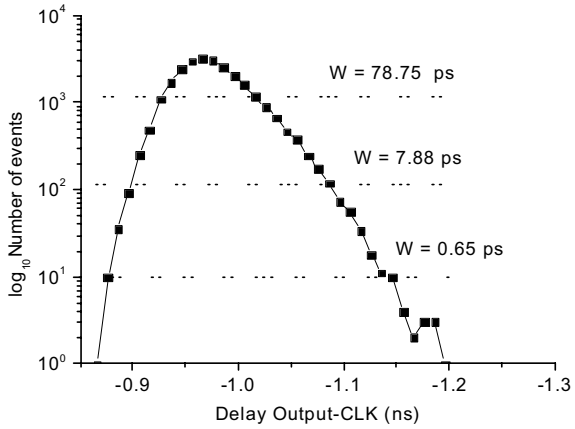

Fig. 9. Determnation of width of the metastable window T_w for IOB FF in Spartan-3 FPGA in metastability test

We present propagation time histogram results both for IOB and for CLB FFs in Spartan-3 FPGAs tested within three working regimes defined by the relation number of logical correct events and total number of events (100 %, 50 % and 10 %). The working regime is defined by setup time. The 100 % regime is derived from the 50 % regime by increasing its setup time by 2 ns, which puts the FF into an area of reliable/safe operation. The 10% regime is the area of deep metastability, with a small number of logically correct events, which are characterized by significantly increased propagation time. Approximately 5000 data points (propagation time) were collected for each working regime. The Spartan-3 FPGA showed little difference between IOB and CLB FF output behavior (Fig. 10. and Fig 11). the average value (mode) of propagation times is noted in the upper right corner of each histogram. The histograms clearly show an increase is propagation time and significant skewing of their distribution as FFs are driven into a metastable region of operation.

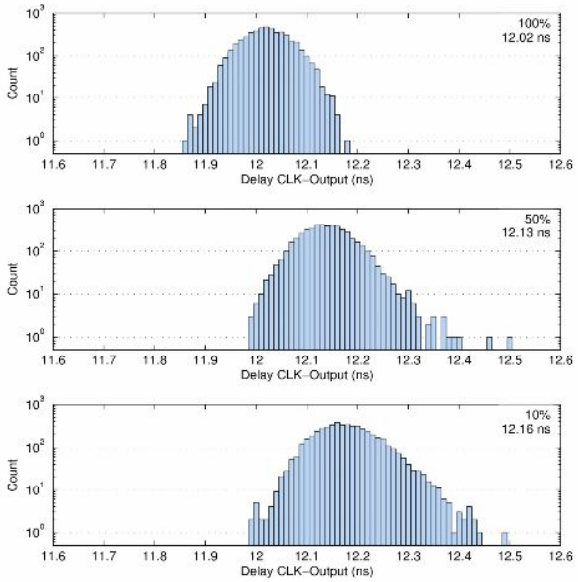

Fig. 10. Propagation time histogram for IOB FF in Spartan-3 FPGA at different stimulus (100%, 50%, 10%) in metastability test

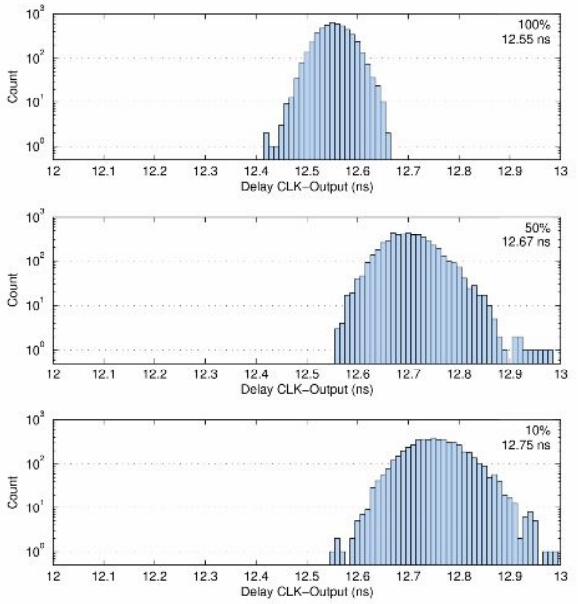

Fig. 11. Propagation time histogram for CLB FF in Spartan-3 FPGA at different stimulus (100%, 50%, 10%) in metastability test

IV. Discussion and Conclusion

In this paper, we have presented a modification of our experimental method for the measurement of metastability characteristics of synchronizing devices like FF using a digital storage oscilloscope for data measurement and analysis. By purposely changing parameters of input signals and by measuring the propagation time, one can monitor the entry of the FF into a metastable state, which is almost impossible in real-life (true) operation of digital circuits. The failures that we do detect provide us with a scaled estimate of the number of true failures. For the purpose of demonstration, the results are presented for IOB and CLB FF outputs fabricated in one process (90 nm) of FPGA devices.

Using the proposed experimental test setup based on a deliberately induced metastability method, we found the resolution time constant of Xilinx's 90 nm FPGA Spartan-3 to be less than 30 ps. In addition, there is no significant difference for the IOB and CLB FF outputs. The effective size of the metastable window depends on the propagation time of the metastable events, and changes by dropping from 0.1 ns to 1 ps.

Measurements on Spartan-3 using the LTD principle (to be announced) resulted in a 25 % higher value of τ. (Measurements were carried out with f_d = 10 MHz and f_c < 90 MHz signals and suggest an increase of MTBF with factor 2.4 x 10^6 for every additional 500 ps delay between the clock signal – At lower clock and asynchronous data frequencies MTBF increases inversely proportional to the product of these two frequencies).

Available data for FPGA devices fabricated in 90 nm processes yielded values of 20 to 50 ps (40 ps measured for Xilinx) and can be used for a comparison/verification with the results measured in our laboratory [16].

Acknowledgment

The authors wish to express their gratitude and satisfaction for being given free licenses from Mentor Graphics Inc. for the use of its advanced software package for rapid time analysis through the support of Academic Research Program.

References

[1] C. Foley, "Characterizing metastability", Proc. of the 2nd International Symposium on Advanced Research in Asynchronous Circuits and Systems, 1996, pp. 175-184.

[2] J. Stephenson, „Don't Let metastability cause problems in your FPGA-based design",(http://www.embedded.com/columns/technicalinsights/220300539?cid=RSSfeed_embedded_news).

[3] P. Afke, "Metastable recovery in Virtex-II Pro FPGAs", (http://china.xilinx.com/support/documentation/application_notes/xapp094.pdf).

[4] "Understanding metastability in FPGAs", (http://www.altera.com/literature/wp/wp-01082-quartus-ii-metastability.pdf).

[5] B. Medved Rogina, B. Vojnović, "Metastability evaluation method by propagation delay distribution measurement", Proc. of the Fourth Asian Test Symposium, 1995, pp. 40-44.

[6] B. Medved Rogina, K. Skala, B. Vojnović, "Metastability characteristics testing for programmable logic design", Lecture Notes in Computer Science 1142, Springer Verlag, 1996, pp. 381-388.

[7] B. Medved Rogina, I. Michieli, „Metastability paremeters evaluation by DSO aquisition", Proc. of the 12th International Workshop on Systems, Signals and Image Processing, 2005, pp. 397-40.

[8] A. Steininger, „Error containment in the presence of metastabiliy", Proc. Dagstuhl Seminar on Distributed Algorithms in VLSI Chips, 2009.

[9] C. Rockwood, "Keeping time with clock domain crossings in FPGAs", (http://chipdesignmag.com/display.php? articleId=903).

[10] R. Ginosar, „MTBF of a multi-synchronizer system on chip", (http://webee.technion.ac.il/~ran/papers/MTBFmultiSyncSoc.pdf).

[11] P. Kalisz, Z. Jachna, „Metastability tests of flip–flops in programmable digital circuits", Microelectronics Journal, (37), 2006, pp. 174-180.

[12] „Spartan-3 FPGA data sheets", (http://www.xilinx.com/support/documentation/spartan-3_data_sheets.htm).

[13] C. Dike, E. Burton, Miller and noise effects in a fynchronizing flip-flop, IEEE Journal of Solid.state Circuits, 34 (1999) 849-855.

[14] A. Cantoni, J. Walker, T.D. Tomlin, Characterization of a flip-flop metastability measurement method, IEEE Transactions on Cuircuits and Systems 54 (2007) 1032-1040.

[15] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution", Metrologia (41), 2004, pp. 17-32.

[16] S. Beer, R. Ginosar, M. Priel, R. Dobkin and A. Kolodny, „The Devolution of Synchronizers", (http://webee.technion.ac.il/~ran/papers/The%20devolution%20of%20synchronizers%20ASYNC%202010.pdf.