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10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Trades Committee of Kharkov National University of Radioelectronics and Trades Committee of Students, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University.

CONTENTS

Transaction Level Model of Embedded Processor for Vector-Logical Analysis

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Abstract

Transaction level model of embedded processor for improving the performance of logical relation analysis are proposed. It is based on the hardware implementation of vector operations. There are examples of the model using for the semantics analysis of Russian adjectives. The embedded processor was designed to be part of SoC that will be implemented on FPGA.

Introduction

With the increase in complexity and velocity of the modern digital devices its energy consumption and cost gross also. The division of tasks across multiple cores of the processor that leads to create some parallel systems using a coherent set of specialized calculators would be a trade-off in this situation. These structures could improve the performance of solving the computational problems, and could reduce the power consumption and the hardware implementation cost of the digital systems.

The special interest of electronic technology market is the scientific and technical direction of formalizing human mental activity to create the artificial intelligence components. These intelligent tools such as expert systems, image recognition and decision-making need creating effective and high-speed engines (multi-processor or specialized embedded processors). A typical example of this domain that requires a specialized processor is the analysis and synthesis of the natural language constructs. At the same time one of the main points of designing the word processor is the hardware implementation of the device that handle synthesis and analysis of the language constructs.

Purpose: Development of the transaction level model of the special embedded processor for hardware realization of the vector operations.

Objectives:

1. Analysis of publications about the specialized logic processor design [1-4].
2. Analysis of the syntactic and semantic models of word processing that implement for natural languages [5-6].
3. Creation of the architecture of the specialized embedded processor that analyze the logical net of the language constructs [6].
4. The hardware implementation of the transaction level model device that implements the grammatical analysis of the Russian adjectives.

The prototype design is used the specialized device that performed grammatical analysis of adjectives end was implemented in the FPGA [6]. The proposed model has more flexibility and can handle any logical net of syntactic and semantic relations. The use of the transaction level modes and design techniques allowed to focus on the order of the data processing and transmission, and reduce unimportant details.

1. Transaction level modeling

With the increasing complexity of software-hardware device such as SoC, designers need to use new digital system description models more abstract than register-transfer level (RTL) models. To address this problem, transaction level models (TLMs) were developed. TLM defines a transaction as the data transfer between sub-systems of a system. Throughout the SoC design cycle, TLM serves for three strategic activities: early software development; architecture analysis; functional verification. Modeling effort are vastly rationalized

A some variation of a model developed by Dan Gajski and Lucai Cai at CODES (HW/SW Co-design Conference) 2003 [1]. The first concept is that sub-system communication and functionality can be developed and refined independently. The communication and functionality components can be un-timed (UT), approximately-timed (AT), or cycle-timed (CT) (Fig. 1).

RTL model is cycle-timed accurate for communication and for functionality. System architectural model (SAM) is with un-timed communication and functionality. Approximately-timed models can rely on statistical timing, estimated

timing, or sub-system timing requirements derive from system requirements. A model with cycle-timed communication and approximately-timed functionality is Bus Functional Model (BFM). The three remaining TLM's don't have commonly accepted names. Gajski and Cai use following names:

1. Component Assembly Model - un-timed communication and approximately-timed functionality;
2. Bus Arbitration Model - approximately-timed communication and approximately-timed functionality;
3. Cycle-Accurate Computation - approximately-timed communication and cycle-timed functionality.

Using TLM for estimations of SoC performance enable the architect to perform initial estimates right in the beginning of the project without RTL or cycle-accurate models. Early estimations enabled by real software running on TLM of SoC before RTL is available to further assist the designer.

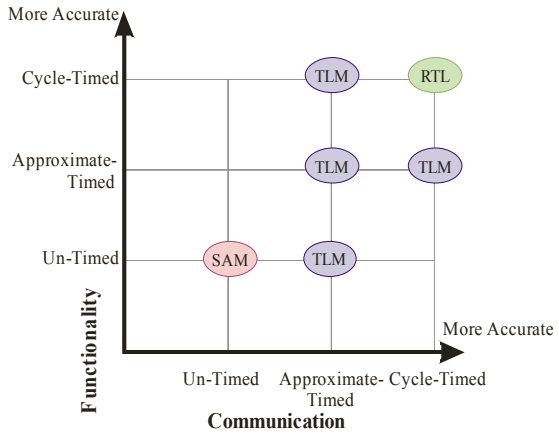

Figure 1. Models of digital systems

Very large Verilog or VHDL simulations along with emulation strategies have traditionally been used for system-level functional verification. With increasing system complexity, Verilog and VHDL simulations have become too slow for such verification. So it is better to use the transaction level simulation for this purpose.

In addition, classes that were included in hardware description language help to improve the productivity of designer and verificater teams by organizing the code in layers, separating model and testbench code.

2. Model of processor for logical relation analysis

This special processor was designed to handle the logical net, where each node is a set of attributes: A, B, C (fig. 3a), and each edge is a functional relation between two attributes that are defined as a binary table. For example, these ones could be a relation between grammatical forms of Russian adjective "stress" – "word stem" that belongs to adjective logical network [6].

Figure 2 shows the framework special embedded processor that consists of three main units: Control block (Control), Logical block (LE), and Memory block (Mem). In turn the last one includes following components: a command memory, a function memory, and a set memory.

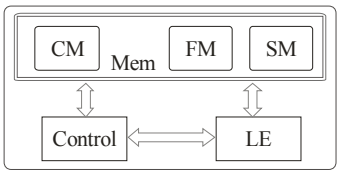

Figure 2. Processor framework

The advantage of the proposed embedded special processor model is that it was constructed to handle the logical nets of any dimensions and doesn't depend on the length of the set vectors and the sizes of the relation tables. It has only limitation that is defined by physical memory size.

The Logical block receives the data parts of a fixed size. If relation table or set vector has bigger size than memory buses dimension, they are broken apart. So there used window scrolling to traverse through whole table (fig 3). The size of scroll window is determined by the memory bus size that transferring data between memory and logic blocks. Process of table starts with the upper-left corner and finishes in the right-down corner. The number of steps for process a table with the NxM dimension are described by equations $N_R = Nn \cdot Nm$. Each relation table after dividing by 2D slice are stored in memory as 1D vectors. Similarly the set vectors are split on the memory words and stored in the memory by parts. Two separated memory blocks that storing relation tables and set vectors allow to read in one cycle two parts of date that are need to implement the elementary logical operation.

For example, if the size of the scrolling window equals 4x4, the relation table with the dimension 26x13 would be split on 28 blocks. It means the processing of this table would need 28 elementary logical operations that make up the processing cycle of the table.

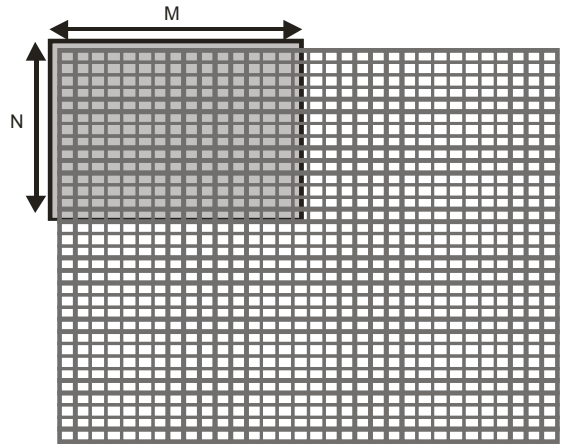

Figure 3. Relation table scrollig

Assume the relations table has a size of 2 to 7 and has following contents.

1	1	1	0	1	0	1	
0	0	0	1	0	1	0	
	1				2		

If size of the scrolling window is 4x4 so this table would take two 16 bit words (fig 4) of the Function memory.

The set vectors are binary where 1 means that the element is included in the set and 0 that it isn't. If relation table dimension is 2x7, the sizes of vectors are 2 and 7 bits, respectively. So R2 vector needs to store 1 memory word, and R1 vector needs 2 words (fig 5). For example,

R1	1	1	0	0	1	1	1

R2	1	0

Command memory uses following format of the word.

size_W	size_H	addr_R0	addr_R1	addr_R2

where size_W and size_H define the size of the relation table, addr_R0, addr_R1, and addr_R2 are start addresses of the date blocks. For the example above and according to Figure 6, the command memory word will have value

2	7	0	0	2

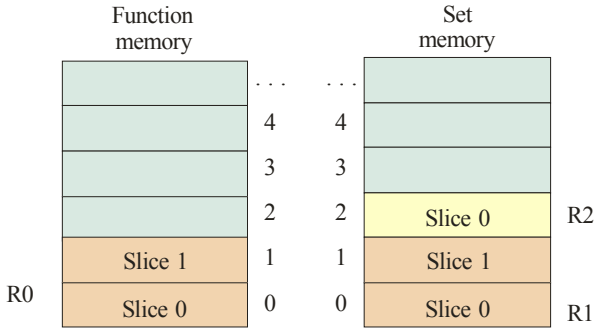

Figure 4. Memory that storing one relation table and its set vectors

3. The transaction level model of the processor

By the classification [1] the proposed model of the special embedded processor is with approximated time accurate for communication and for functionality, so it is the Bus Arbitration Model.

Object Oriented Programming (OOP) was used for developed the processor model. Each device unit was designed as class that communicates with the other ones through virtual interface. Then for refining design these classes could be replaced by a description of RTL-level, and the virtual interface could be changed to interface block.

For the developing of transaction level model are used object-oriented language features of the SystemVerilog hardware description and verification. Figure 6 shows the structure of the classes.

TLM_model includes objects of three classes: Control_block, LE_block, and Top_mem, which describe the three units of the embedded processor framework (fig. 2): Control block (Control), Logical block (LE), and Memory block (Mem).

Base class is DUT_object class (fig. 6). Other classes expanded upon its through inherence. The Configuration class is designed to control the constraint random generation of the input stimuli that is used at the verification stage.

Micro_command encapsulate the data together with the routines that describe and manipulate processor commands. Mem_object class is blueprint The classes that describe memory have the methods: for variable value initial (read and write), for output data to the consol (print); for output data to text file (fprint); for work starting (run). In addition to these methods the Control block that is described as the class control_block, has routines: for reading a command (read_command), for generating the control signal

sequences for memory and logic unit (gen), for transmitting control signals through the interface (drive). Stable_check () method checks the time of the finishing of the logical net processing.

An object of the TLM_model class is implemented in the Top module that includes the bus interface also. The last one is a model of the special embedded processor bus. The SystemVerilog code of the interface is shown on listing 1. Also it has variable that describe transmitting data as well as events that synchronize the work of individual blocks of the system.

Listing 1. SystemVerilog model of the interface

```
interface interf;
  bit clk = 0;
  initial  forever #5 clk = ~clk;

   //command
  event command_request;
  event command_resp;
  event PC_clear_e;
  event pass_end; // pass all commands
  event work_stop; //
  bit [7:0] size_r1, size_r2;

bit [7:0] start_R0, start_R1, start_R2;
    clocking cb@(posedge clk);

  // output size_r1, size_r2;
    // output start_R0, start_R1, start_R2;

 endclocking: cb
    always @(pass_end)
      $display("1 pass command memmory have finished");

    // memmory
  event data_read, data_send, pass_start;
  bit [7:0] addr_R0, addr_R1, addr_R2;
  bit first_block, line_end, last_block, direction;
  logic [(`block_size*`block_size)-1:0] R0;
  logic [`block_size-1:0] R1;
  logic [`block_size-1:0] R2;
  bit R3;
    event data_write;
  bit [7:0] addr_R2_w;
  logic [`block_size-1:0] R2_w;
    // stop

 event simul_finish;
endinterface
```

4. Conclusion

Scientific novelty. The transaction level model of the special embedded processor for logical analysis of the Russian adjectives was developed. The model allows creating the hardware implementation for any logical relations graph for natural language structure analysis. This device requires more time for processing of the system than one that was presented earlier [6], but exceeds it in versatility.

The object-oriented programming has been used to reduce the design time of creating the SystemVerilog transaction level model. This modern approach of the development of the digital systems significantly improves the design process performance.

Further studies are associated with the creating the generators of the complex architecture of the logical relations, with the possibility of combining several logic blocks to improve the functional performance.

5. References

[1] David C. Black, Jack Donovan. SystemC: from the ground up. Kluwer Acad. Publishers, 2004. 263p.

[2] Bergeron, Janick. Writing testbenches: functional verification of HDL models. Boston: Kluwer Academic Publishers, 2001. 354 c.

[3] Donald E. Thomas. Philip R. Moorby. The Verilog Hardware Description Language. New York, Boston, Dordrecht, London, Moscow: Kluwer Academic Publishers. 2002. 404 p.

[4] Hahanov V.I., Hahanova I.V. and others. Verilog&SystemVerilog. Kharkov: New word, 2010. 528c.

[5] General algebra. Handbook. V.2. Ed. Skornyakova. 1991. chapter 7. Categories. M. Nauka. 1991. P.368-460.

[6] Bondarenko M.F., Hahanova I.V. Logic networks application for computing process organization. Radioelectronics & Informatics, 2003. P. 150-156.

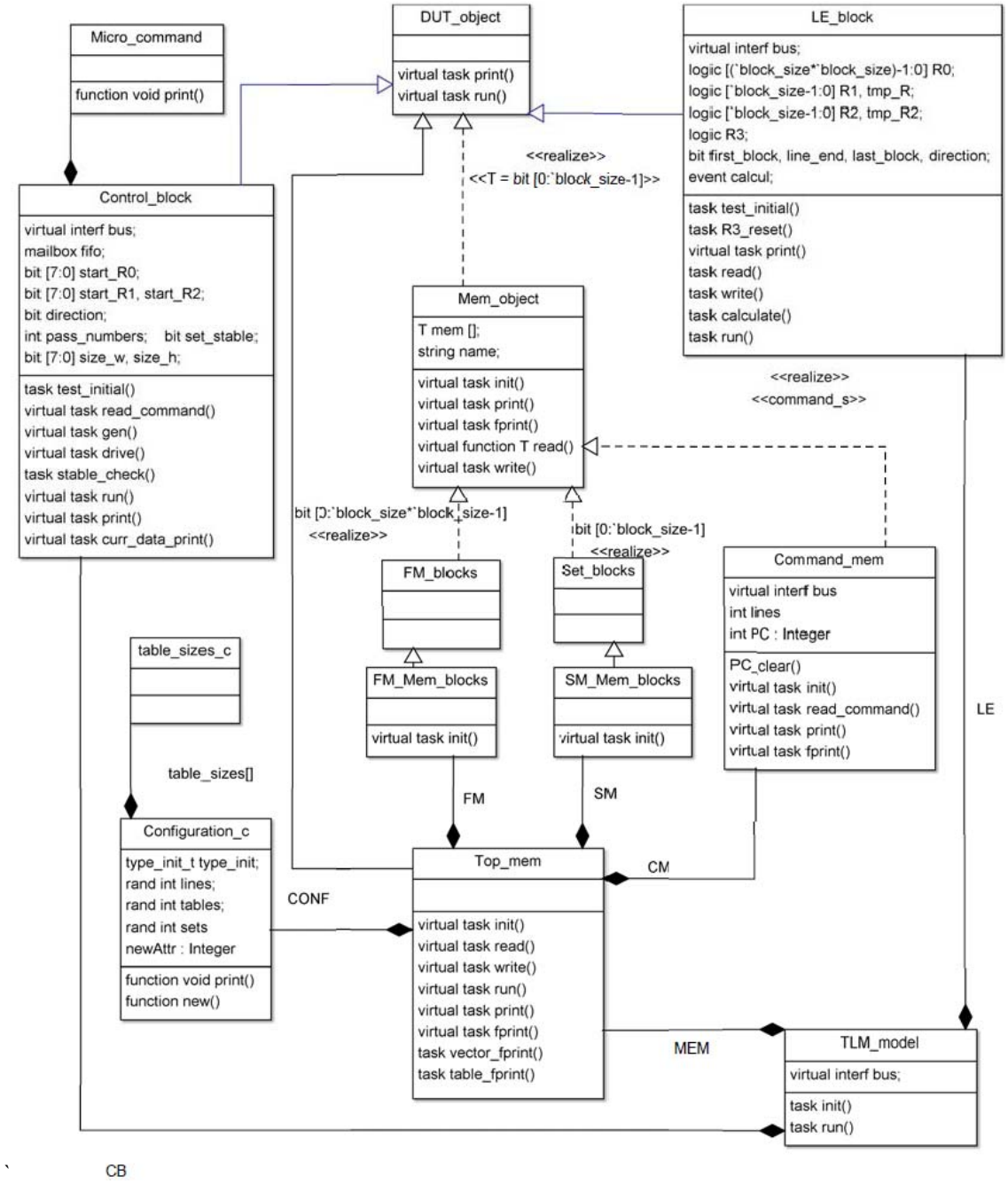

Figure 5. Model of classes

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