

KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2014)

Copyright © 2014 by The Institute of Electrical and Electronics Engineers, Inc.

**SPONSORED BY
IEEE Computer Society Test Technology Technical Council**



Kiev, Ukraine, September 26 – 29, 2014

IEEE EAST-WEST DESIGN & TEST SYMPOSIUM 2014 COMMITTEES

General Chairs

V. Hahanov – Ukraine
Y. Zorian – USA

General Vice-Chairs

R. Ubar - Estonia
P. Prinetto - Italy

Program Chairs

S. Shoukourian – Armenia
D. Speranskiy – Russia

Program Vice-Chairs

Z. Navabi – Iran
M. Renovell – France

Publicity Chair's

G. Markosyan - Armenia
S. Mosin - Russia

Public Relation Chair

V. Djigan - Russia

Program Committee

J. Abraham - USA
M. Adamski - Poland
A.E.Mohamed Mohamed - Egypt
A . Barkalov - Poland
R. Bazylevych - Ukraine
A. Chaterjee - USA
V. Djigan - Russia
A. Drozd - Ukraine
D. Efanov - Russia
E. Evdokimov - Ukraine

E. Gramatova - Slovakia
A. Ivanov - Canada
M. Karavay - Russia
V. Kharchenko - Ukraine
K. Kuchukjan - Armenia
W. Kuzmicz - Poland
A. Matrosova - Russia
V. Melikyan - Armenia
L. Mikleu - Romania
O. Novak - Czech Republic
Z. Peng - Sweden
A. Petrenko - Ukraine
J. Raik - Estonia
A. Romankevich - Ukraine
A. Ryjov - Russia
R. Seinauskas - Lithuania
S. Sharshunov - Russia
A. Singh - USA
J. Skobtsov - Ukraine
V. Tverdokhlebov - Russia
V. Vardanian - Armenia
V. Yarmolik - Byelorussia

Steering Committee

V. Hahanov - Ukraine
R. Ubar - Estonia
Y. Zorian - USA

Organizing Committee

V. Andrushchenko - Ukraine
A. Kudin - Ukraine
S. Chumachenko - Ukraine
E. Litvinova – Ukraine

EWDTS CONTACT INFORMATION

Prof. Vladimir Hahanov
Design Automation Department
Kharkov National University of Radio Electronics,
14 Lenin ave,
Kharkov, 61166, Ukraine.
Tel.: +380 (57)-702-13-26
E-mail: hahanov@kture.kharkov.ua
Web: www.ewdtest.com/conf/

12th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2014) Kiev, Ukraine, September 26-29, 2014

The main target of the **IEEE East-West Design & Test Symposium (EWDTS)** is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'14 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- Power Issues in Design & Test
- On-Line Testing
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- Optical signals in communication and Information Processing
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The symposium is organized by Kharkov National University of Radio Electronics, National Pedagogical Dragomanov University and Science Academy of Applied Radio Electronics <http://anpre.org.ua/> in cooperation with Tallinn University of Technology.



CONTENTS

Extending Fault Periodicity Table for Testing Faults in Memories under 20nm Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.	12
Modified Fast PCA Algorithm on GPU Architecture Vazgen Melikyan, Hasmik Osipyan	16
Design of Low-Ripple Multi-Topology Step-Down Switched Capacitor Power Converter with Adaptive Control System Vazgen Melikyan, Vache Galstyan	20
Resistance Calibration Method Without External Precision Elements Vazgen Melikyan, Arthur Sahakyan, Mikayel Piloyan	24
An Efficient Signature Loading Mechanism for Memory Repair Vrezh Sargsyan	28
Dual Interpolating Counter Architecture for Atomic Clock Comparison Jiřr'ı Dost'al, Vladim'ır Smotlacha	32
Communication with Smart Transformers in Rural Settings Cornel Verster, Males Tomlinson, Johan Beukes	36
Scalable Contention-free Routing Architecture for Optical Network on-chip Elham Shalmashi, Samira Saiedi, Midia Reshadi	41
The Concept of Green Cloud Infrastructure Based on Distributed Computing and Hardware Accelerator within FPGA as a Service Yanovskaya O., Yanovsky M., Kharchenko V.	45
Cyber Physical System – Smart Cloud Traffic Control Vladimir Hahanov, Wajeb Gharibi, Abramova L.S., Svetlana Chumachenko, Eugenia Litvinova, Anna Hahanova, Vladimir Rustinov, Vladimir Miz, Aleksey Zhalilo, Artur Ziarmand	49
Cyber Physical Social Systems – Future of Ukraine Vladimir Hahanov, Wajeb Gharibi, Kudin A.P., Ivan Hahanov, Ngene Cristopher (Nigeria), Tiekura Yeve (Côte d'Ivoire), Daria Krulevska, Anastasya Yerchenko, Alexander Mishchenko, Dmitry Shcherbin, Aleksey Priymak	67
The Cooperative Human-Machine Interfaces for Cloud-Based Advanced Driver Assistance Systems: Dynamic Analysis and Assurance of Vehicle Safety Vyacheslav Kharchenko, Alexandr Orehov, Eugene Brezhnev, Anastasiya Orehova, Viacheslav Manulik	82
Multichannel Fast Affine Projection Algorithm with Gradient Adaptive Step-Size and Fast Computation of Adaptive Filter Output Signal Victor I. Djigan	87
Qubit Method for Diagnosing Digital Systems Baghdadi Ammar Awni Abbas (Baghdad University), Farid Dahiri, Anastasiya Hahanova	93
Method for Diagnosing SoC HDL-code Vladimir Hahanov, Sergey Zaychenko, Valeria Varchenko	97

Smart traffic light in terms of the Cognitive road traffic management system (CTMS) based on the Internet of Things Volodymyr Miz, Vladimir Hahanov	103
Partitioning of ECE Schemes Components Based on Modified Graph Coloring Algorithm Kureichik V.V., Kureichik VI.VI., Zaruba D.V.	108
Neighborhood Research Approach in Swarm Intelligence for Solving the Optimization Problems Kuliev E.V., Dukhardt A.N., Kureychik V.V., Legebokov A.A.	112
On the Synthesis of Unidirectional Combinational Circuits Detecting All Single Faults Valery Sapozhnikov, Vladimir Sapozhnikov, Dmitry Efanov, Anton Blyudov	116
Combinational Circuits Checking on the Base of Sum Codes with One Weighted Data Bit Valery Sapozhnikov, Vladimir Sapozhnikov, Dmitry Efanov, Dmitry Nikitin	126
The Novel Compact Multilevel SIW-Filter for Microwave Integrated Circuits Zemlyakov V.V., Zargano G.F., Shabarshina I.S.	137
A Technique to Analyze the Impact of NBTI effect on Oscillator Behavior Gourary M.M., Rusakov S.G., Ulyanov S.L., Zharov M.M.	140
Control Vector Structure for Circuit Optimization Zemliak A., Reyes F., Markina T.	143
Theory of Bionic Optimization and its Application to Evolutionary Synthesis of Digital Devices Sergey Rodzin, Lada Rodzina	147
Broken Bar Fault Diagnosis for Induction Machines under Load Variation Condition using Discrete Wavelet Transform Pu Shi, Zheng Chen, Yuriy Vagapov, Anastasia Davydova, Sergey Lupin	152
Modeling of MOSFETs Parameters and Volt-Ampere Characteristics in a Wide Temperature Range for Low Noise Amplifiers Design Alexandr M. Pilipenko, Vadim N. Biryukov	156
Active-Mode Leakage Power Optimization Using State-Preserving Techniques Andrey V. Korshunov, Pavel S. Volobuev	160
Partially Programmable Circuit Design Matrosova A., Ostanin S., Kirienko I., Singh V.	164
Combinational Part Structure Simplification of Fully delay Testable Sequential Circuit Matrosova A., Mitrofanov E., Roumjantseva E.	168
Decomposition Tree - based Compaction Procedure with Iteration Steps for Interconversional Layouts of Tasks Valentina Andreeva, Kirill A. Sorudeykin	173
Combinational Circuits without False Paths Matrosova A., Kudin D., Nikolaeva E.	179

The Levels of Target Resources Development in Computer Systems Drozd J., Drozd A., Maevsky D., Shapa L.	185
Deriving complete finite tests based on state machines Igor Burdonov, Alexander Kossatchev, Nina Yevtushenko	190
Microwave Selective Amplifiers with Paraphase Output Sergey G. Krutchinsky, Petr S. Budyakov, Nikolay N. Prokopenko, Vladislav Ya. Yugai	194
The Multichannel High-Frequency Compensation of the Analog Sections of Flash ADCs with the Differential Input at the Cascade Connection of the Reference Resistors Nikolay N. Prokopenko, Alexander I. Serebryakov, Vladislav Ya. Yugai	198
Selftest ADCs for Smart Sensors Sergei G. Krutchinsky, Evgeniy A. Zhebrun	201
Algorithmic Design Technique for Increase ADC Fault Tolerance Victor Chapenko	205
Manufacturing Scheduling Problem Based on Fuzzy Genetic Algorithm Leonid Gladkov, Nadezhda Gladkova, Sergey Leiba	209
Assessment of Survivability of Complex Control Systems using Simulation Methods Anastasia Davydova, Sergey Lupin, Yuriy Vagapov	213
The Impact of Sensors' Implementation on Lift Control System Sergey Lupin, Kyaw Kyaw Lin, Anastasia Davydova, Yuriy Vagapov	217
Threshold Method of Measurement of Extended Objects Speed of Radio Engineering Devices of Short-Range Detection Artyushenko V. M., Volovach V. I.	220
Frequency reference on the basis of photonic crystal for the system of stabilizing of frequency of solid-state lasers Machekhin Y.P., Khorolets L.S.	224
Stable fiber ring laser for DWDM systems and information processing Alexander Gnatenko, Yuri P. Machekhin	228
A New Method of Length Measurement with Subpicometer Resolution A. Danelyan, V. Danelyan, M.Lashauri, S. Mkrtychyan, S. Shotashvili, V. Sikharulidze, G. Tatishvili, T. Chichua, D. Garibashvili, I. Lomidze, Yu. Machekhin	231
Magnetoresonance study of Co-Ni nanowires array Arthur Vakula, Liubov Ivzhenko, Anastasiia Moskaltsova, Sergey Nedukh, Sergey Tarapov, Mariana Proenca, Joao Araujo	235
Finite Layered Periodical Chiral Metamaterial with Band Structure of Spectra for Extra High Frequency Contemporary Electronics Polevoy S. Yu., Tarapov S. I.	238
The Formulation of Criteria of BIBO Stability of 3rd-order IIR Digital Filters in Space of Coefficients of a Denominator of Transfer Function Lesnikov V., Naumovich T., Chastikov A.	240

Test Generation for Digital Circuits Based on Continuous Approach to Circuit Simulation Using Different Continuous Extensions of Boolean Functions Kascheev N., Kascheev P.	243
Qubit Modeling Digital Systems Hahanova Irina, Emelyanov Igor, Tamer Bani Amer	246
Repair of Combinational Units Yulia Hahanova, Armen Bayadzhan	249
Analysis of State Assignment Methods for FSM Synthesis Targeting FPGA Alexander Barkalov, Irina Zelenyova, Ievgen Tatolov	252
Malicious Hardware: Characteristics, Classification and Formal Models Valeriy Gorbachov	254
Self-Testing Checker Design for Incomplete m-out-of-n Codes Butorina N.	258
Profiling of MES software requirements for the pharmaceutical enterprise Fedoseeva A., Kharchenko V.	262
Cyber security of smart substations with critical load via cyber diversity: strategies and assessment Eugene Brezhniev, Vyacheslav Kharchenko, Jüri Vain	266
A New Technique for Layout Based Functional Testing of Modules in Digital Microfluidic Biochips Pranab Roy, Samadrita Bhattacharya, Hafizur Rahaman, Parthasarathi Dasgupta	272
The Propagation of Electromagnetic Millimeter Waves in Heterogeneous Structures Based on Wire Metamaterial Liubov Ivzhenko, Sergey Tarapov	278
Discovering New Indicators for Botnet Traffic Detection Alexander Adamov, Vladimir Hahanov, Anders Carlsson	281
Expert evaluation model of the computer system diagnostic features Krivoulya G., Shkil A., Kucherenko D., Lipchansky A., Sheremet Ye.	286
Construction of Adaptive Artificial Boundary Conditions Using the Invariant Ratios for Schrödinger Equation Vyacheslav A. Trofimov, Evgeny M. Trykin	290
Comparative Analysis of Interference Immunity of Adaptive Information Transmission System with Hybrid Spectrum Spreading and Nonadaptive Systems Nechaev Y.B., Kashenko G.A., Plaksenko O.A.	294
On Fuzzy Expert System Development Using Computer-Aided Software Engineering Tools Polkovnikova N. A., Kureichik V. M.	298
Incoming inspection of FPGAs Alexander Ogurtsov, Andrey Koulibaba, Ivan Bulaev	302

Set Covering on the Basis of the ant Algorithm Lebedev B.K., Lebedev O.B., Lebedeva E.M.	305
Two-channel real-time steganographic system Shakurskiy M.V., Shakurskiy V.K., Volovach V.I.	309
Mobile Health Applications to Support Diabetic Patient and Doctor Petrenko A.I.	312
Temperature Aware Test Scheduling by Modified Floorplanning Indira Rawat, M.K. Gupta, Virendra Singh	318
Functional Transformation for Direct Embedding Steganographic Methods Barannik Vladimir, Bekirov Ali, Roman Tarnopolov	322
Method of Increase of Safety of Video Information of Aero Monitoring of Emergency Situations Barannik V., Kulica O., Shadi Othman	325
Assessment of Video Information Resource Security of Videoconferencing in Public Administration Vlasov A.V., Sidchenko Sergey, Komolov Dm., Saprykina T.	329
Video Decompression Technology in Information and Communication Technologies Ryabukha Yu., Krivonos Vladimir, Hahanova Anna	332
Compact Vector Representation Method of Semantic Layer Barannik Vladimir, Shiryayev Andrey, Krasnorutskij Andrey, Tretyak V.	335
Control of Video Compression Parameters with Regard to the Particular Characteristics of Block Content Dvukhglavov Dmitry, Tverdokhlebo Vitaliy, Kharchenko N., Shadi Othman	338
Processing Method of a Flow of the Differential Provided Frames in Objective Video Inspection Telecommunication Systems Lekakh A., Turenko S., Akimov Ruslan, Yurchenko Konstantin	341
Factors Influencing User Satisfaction of E-tax Filing in Thailand The Study of Small and Medium Enterprises (SMEs) Nakanya Chumsombat	344
The Linear Logic Synthesis of k-Valued Digital Structures in the Analogous Circuitry Basis Nikolay N. Prokopenko, Nikolay I. Chernov, Vladislav Ya. Yugai	348
The Precision Voltage References for the Radiation-Hardened Bi-FET Technological Process Evgeniy I. Starchenko, Nikolay N. Prokopenko, Vladislav Ya. Yugai	352
Squaring in Reversible Logic using Iterative Structure Arindam Banerjee and Debesh Kumar Das	356
AUTHORS INDEX	360

Qubit Modeling Digital Systems

Irina Hahanova, Igor Emelyanov, Tamer Bani Amer
National University of Radioelectronics, Kharkov, Ukraine,
hahanov@kture.kharkov.ua

Abstract

The data structures, effective from the viewpoint of software or hardware implementation of fault-free interpretative modelling discrete systems described in the form of qubit vectors of primitive output states are considered.

1. A model for analyzing digital system

To describe digital circuit shown in Fig. 1, the structure of interrelated elements and cubic coverage (truth tables) of logic elements are used [1-2].

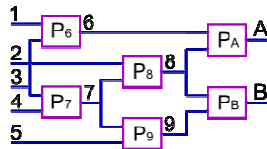


Figure 1. Fragment of digital circuit

The aim of the proposed method for qubit simulation is to replace the truth tables of digital device components by vectors of output states. Let functional primitive with number P_6 has the following truth table:

$$P_6 = \begin{array}{|c|c|c|} \hline X_1 & X_2 & Y \\ \hline 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ \hline \end{array}$$

This coverage of a logic element can be transformed by unitary encoding input vectors based on the use of two-stroke alphabet [4-7]. Symbols and their codes for describing automaton variables are the power set (the set of all subsets) on the universe of four primitives that corresponds to the format of vector containing two qubits:

$B^*(Y) = \{Q=(1000), E=(0100), H=(0010), J=(0001), O=\{Q,H\}=(1010), I=\{E,J\}=(0101), A=\{Q,E\}=(1100), B=\{H,J\}=(0011), S=\{Q,J\}=(1001), P=\{E,H\}=(0110),$

$C=\{E,H,J\}=(1110), F=\{Q,H,J\}=(1011), L=\{Q,E,J\}=(1101), V=\{Q,E,H\}=(1110), Y=\{Q,E,H,J\}=(1111), U=(0000)\}.$

By using two-stroke alphabet any coverage of the functional primitive can be represented by two or one cube through encoding input sets and subsequent combining symbols, given that the cubes are mutually inverse:

$$P_6 = \begin{array}{|c|c|} \hline 00 & 1 \\ 01 & 1 \\ 10 & 1 \\ 11 & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline Q & 1 \\ E & 1 \\ H & 1 \\ J & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline V & 1 \\ J & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline 1110 & 1 \\ 0001 & 0 \\ \hline \end{array} \rightarrow \begin{array}{|c|c|c|c|} \hline 1 & 1 & 1 & 0 \\ \hline \end{array}$$

Two cubes show not only all the solutions, but also the inverse output signal that is interesting from the point of activation of all logical paths in the circuit structure, when synthesizing tests. For example, to change the output state we can create a pair of

consecutive terms $\begin{array}{|c|c|} \hline 1110 & 1 \\ 0001 & 0 \\ \hline \end{array}$, where in the first cycle

the first three input vectors 00, 01, 10 are written in the form of qubit (11101), and in second one - fourth vector (00010) formed by values 11 of two input variables.

To simulate fault-free behaviour it is enough to have a single cube (zero or unit), since the second one is always a complement to the first cube. Consequently, focusing, for example, to the unit cube, forming 1 at the output, we can remove a bit of primitive output state, reducing the dimension of the cube or primitive model up to the number of addressable primitive states, where address is a vector composed of the binary values of the input variables, which identifies the primitive state of the output.

Qubit Q-coverage is the vector form of interpretative description of the functionality where the coordinate value determines the state of the function output corresponding to the binary input word, forming a cell address. Q-coverage of 1-output primitive is always represented by two mutually inverse cubes (vectors) whose dimension is equal to a power of two the number of input variables, where a

single coordinate value defines the usage of the address of considered bit in the formation of the corresponding (0,1) state of the primitive output. Qubit models of primitives require the creation of a novel theory for modelling, direct and inverse implication, test synthesis, fault simulation, fault detection. Here and below we present the main procedures for fault-free simulation based on manipulating addresses implicitly represented in cube coordinates of Q-coverage.

Model for analyzing digital system based on the use of qubit data structures can be described by four components:

$$\begin{aligned} F &= \langle L, M, X, Q \rangle, \\ L &= (L_1, L_2, \dots, L_j, \dots, L_n); \\ M &= (M_1, M_2, \dots, M_j, \dots, M_n); \\ X &= (X_{n_x+1}, X_{n_x+2}, \dots, X_{n_x+i}, \dots, X_n); \\ Q &= (Q_{n_x+1}, Q_{n_x+2}, \dots, Q_{n_x+i}, \dots, Q_n). \end{aligned}$$

The following designations are used here: L - vector of identifiers for equipotential lines of digital circuit, which, because of its triviality can be excluded from the model, but it is necessary to know a number of input variables of a device and total number of lines; M - state modeling vector for all circuit lines; X - the ordered set of input variable vectors for each circuit primitive associated with the output numbers; Q - a set of Q-coverages for the primitives, strictly associated with the output numbers and the input variables of the primitives; n - the number of lines in the circuit; n_x - the number of input variables.

As an example of qubit model of digital device $F = \langle L, M, X, Q \rangle$ represented in Fig. 3 a variant of the circuit description table for analyzing fault-free behavior (fault free simulation) is given below:

L	1	2	3	4	5	6	7	8	9	A	B
M	1	1	1	1	1	0	1	0	1	1	0
X	.	.	.	.	.	13	34	27	75	68	89
Q	.	.	.	.	.	1	0	1	1	1	1
	.	.	.	.	.	1	1	0	0	0	0
	.	.	.	.	.	1	1	0	0	1	1
	.	.	.	.	.	0	1	0	1	0	1

The method of qubit fault-free simulation is reduced to the definition of output value for the element at the address generated by concatenation of binary states of input variables for each primitive of digital circuit $M(Y_i) = Q_i[M(X_{i1} * X_{i2} \dots * X_{ij} \dots * X_{ik_i})]$. Here k_i - a number of input lines in the primitive i .

If the variables create non-binary address, in this case, there is a possibility of forming non-binary

output state of the primitive, which is defined in the ternary alphabet by symbol X. The output states are formed by consistent modeling, based on simple iterations or Seidel iterations [1]. In the second case a preprocessor procedure for ranking lines and circuit primitives is necessary, which considerably reduces the number of passes on the circuit primitives to achieve convergence when the equality of the states of all circuit lines in two adjacent iterations is fixed. In addition, the ranking of primitives on the levels of forming outputs allows significantly improving the performance of simulation due to parallel processing functional elements of one level. For example, for the circuit shown in Fig. 3, we can handle concurrently the elements with the numbers 6, 7, and then - 8, 9 and beyond - A, B. In the first case, when simple iterations are used ranking is not required, but cost for simplicity of simulation algorithm is significantly greater number of iterative passes through the circuit primitives to achieve the convergence criterion.

Because of the outputs of processed primitives uniquely identify numbers of non-input lines of the vector L, the formula for modeling can be reduced to the loop determining the status of all non-input variables:

$$\begin{aligned} M_i &= Q_i[M(X_{i1} * X_{i2} \dots * X_{ij} \dots * X_{ik_i})] = Q_i[M(A_i)], \\ i &= \overline{n_x + 1, n}. \end{aligned}$$

Here the modeling process is associated with obtaining bit address in a functionality qubit by concatenation and determining the status of the primitive or non-input line of a digital structure, starting with the number $i = n_x + 1$. If the variables create non-binary address, in this case, there is possibility of forming the output state of the logic element in the ternary alphabet by symbol X. The output states are formed by the primitive procedure for processing a primitive qubit $M_i = Q_i[M(X_i)]$, based on simple iterations or Seidel iterations [1]. In the second case a preprocessor procedure for ranking lines and circuit primitives is necessary, which considerably reduces the number of passes on the circuit primitives to achieve convergence when the equality of the states of all circuit lines in two adjacent iterations is fixed. In addition, the ranking of primitives on the levels of forming outputs allows significantly improving the performance of simulation due to parallel processing functional elements of the same level. For example, for the circuit shown in Fig. 1, we can handle concurrently the elements with the numbers 6, 7, and then - 8, 9 and beyond - A, B. In the first case, when simple iterations are used ranking is not required, but cost for simplicity

of simulation algorithm is significantly greater number of iterative passes through the circuit primitives to achieve the convergence criterion. Computational complexity of the proposed Q-method for modeling based on qubit functionalities is determined by the procedures for generating an address (input vector), containing k_i variables for each i -th primitive $(r+w) \times k_i$, reading a bit from qubit vector at concatenated address and writing $(r+w)$ for given bit to the modeling vector:

$$\begin{aligned} \eta &= \sum_{i=n_x+1}^n \{[(r+w) \times k_i] + (r+w)\} = \sum_{i=n_x+1}^n [(r+w) \times (k_i + 1)] = \\ &= \sum_{i=n_x+1}^n (k_i + 1) \end{aligned}$$

The modeling time for a test vector by the Q-method at the condition that a digital circuit composed of 900 4-input primitives is characterized by the parameters: $r=w=5\text{ns}$, $k_i = 4$, $n_x = 100$, $n=1000$, is equal to 45 microseconds:

$$\begin{aligned} \eta &= (r+w) \times \sum_{i=n_x+1}^n (k_i + 1) = (5+5) \times 900 \times (4+1) = \\ &= 45000\text{ns} = 45\mu\text{s} \end{aligned}$$

This means that the performance of an interpretative Q-method for modeling allows processing 22 222 input vectors per second for a given circuit. At that a digital device has a significant advantage - the service function for repairing failure primitive online by re-addressing it on the spare element.

For the synthesis of quasi-optimal data structures of a combinational device it is necessary to use the following rules:

1) To simulate by using Seidel's method, the ranked circuit of a digital device on the structural depth must have the same type of primitives as possible in each level (layer) of operation.

2) It is desirable to have the same number of primitives at each level that means - synthesis of digital device has to be focused on creating a rectangular or matrix like structure of similar logical elements.

3) Implementation of the combinational primitives provides for using addressable memory elements existing in programmable logic devices (FPGA, CPLD), widely used for prototyping.

4) Providing spare primitives for each level of the combinational device for online repairing - one spare element for each type of component that is used in the level.

5) Hardware cost for implementing high-performance combinational device should be determined by the sum of all the primitives associated with the levels of combinational device, extended by set of spares, one for each layer (assuming the existence of the same primitives in each layer):

$$Q = \sum_{i=1, n}^{j=1, m} P_{ij} + n.$$

6) Implementation of the combinational device based on minimizing hardware cost is determined by the sum of all types of primitives, which are invariant to the levels of combinational device and extended by set of spares, one for each type:

$$Q = \sum_{i=1}^m P_i + m.$$

7) Processing the matrix of the combinational elements by using the processor line of primitives, the number of which is equal to the power of maximum level or layer in rectangular structure, which provides the possibility for parallel processing all primitives in each element level in order to improve the performance of the combinational prototype, implemented in the PLD.

3. Conclusion

The novelty of the proposed Q-method for interpretative fault-free simulating digital circuits lies in significantly increasing the performance and reducing the volume of data structures through replacing the truth tables by the Q-coverage that provides the competitiveness of the proposed development in comparison with compilation simulation.

4. References

- [1] Hahanov V.I. *Digital System-on-Chip Design and Test*, Kharkov: Novoye Slovo, 2009, 484 p.
- [2] Hahanov V.I., Murad Ali A., Litvinova E.I., Guz O.A., Hahanova I.V. "Quantum models of computing processes", *Radioelectronics & Informatics*, 2011, No 3, P.35-40.

Camera-ready was prepared in Kharkov National University of Radio
Electronics by Dr. Svetlana Chumachenko
Lenin ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 20.09.2014. Format 60×84¹/₈.
Relative printer's sheets: . Circulation: 50 copies.
Published by SPD FL Stepanov V.V.
Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозиуму «Схід-Захід Проектування та Діагностування – 2014»
Макет підготовлено у Харківському національному університеті
радіоелектроніки Редактор: Світлана Чумаченко
Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 20.09.2014.
Формат 60×84¹/₈. Умов. друк. арк. . Наклад: 50 прим.
Видано: СПД ФЛ Степанов В.В.
Вул. Ак. Павлова, 311, Харків, 61168, Україна