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The main target of the **IEEE East-West Design & Test Symposium (EWDTS)** is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'14 which covers (but is not limited to) the following topics:

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Method for Diagnosing SoC HDL-code

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Abstract

This article describes technology for diagnosis SoC HDL-models, based on Code-Flow Transaction Graph. Diagnosis method is focused to decrease the time of fault detection and memory for storage of diagnosis matrix by means of forming ternary relations between test, monitor, and functional component. The following problems are solved: creation of digital system model in the form of transaction graph and multi-tree of fault detection tables, as well as ternary matrices for activating functional components of the selected set of monitors by using test patterns; development of a method for analysis the activation matrix to detect the faulty blocks with given depth and synthesis logic functions for subsequent embedded hardware fault diagnosis.

1. TAB-model for diagnosing faulty SoC components

The goal is creation TAB-matrix model (Tests – Assertions – Blocks functional) model and diagnosis method to decrease the time of testing and memory for storage by means of forming ternary relations (test – monitor – functional component) in a single table.

The problems are: 1) development of digital system HDL-model in the form of a transaction graph for diagnosing functional blocks by using assertion set [1-6,15]; 2) development method for analyzing TAB-matrix to detect minimal set of fault blocks [4-7,13]; 3) Synthesis of logic functions for embedded fault diagnosis procedure [8-11,14].

Model for testing a digital system HDL-code is represented by the following xor-relation between the parameters <test – functionality – faulty blocks B*>:

$$T \oplus B \oplus B^* = 0; B^* = T \oplus B = \{T \times A\} \oplus B,$$

which transformed the relationship of the components in the TAB-matrix:

$$M = \{\{T \times A\} \times \{B\}\}, M_{ij} = (T \times A)_i \oplus B_j.$$

Here, the coordinate of the matrix is equal to 1, if the pair test-monitor $(T \times A)_i$ detects or activates some faults of the functional block $B_j \in B$.

An analytical model for verification by using a temporal assertion (additional observation statements or lines) is focused to achieve the specified diagnosis depth and presented as follows:

$$\begin{aligned} \Omega &= f(G, A, B, S, T), G = (A * B) \times S; S = f(T, B); \\ A &= \{A_1, A_2, \dots, A_i, \dots, A_n\}; B = \{B_1, B_2, \dots, B_i, \dots, B_n\}; \\ S &= \{S_1, S_2, \dots, S_i, \dots, S_m\}; T = \{T_1, T_2, \dots, T_i, \dots, T_k\}. \end{aligned}$$

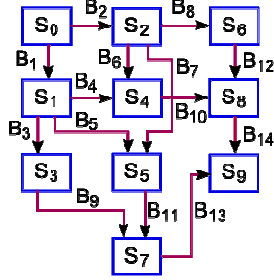
Here $G = (A * B) \times S$ is functionality, represented by Code-Flow Transaction (CFT) Graph (Fig. 1); $S = \{S_1, S_2, \dots, S_i, \dots, S_m\}$ are nodes represented by software variables states when simulating test segments (patterns). Otherwise the graph can be considered as an ABC-graph – Assertion Based Coverage Graph. Each state $S_i = \{S_{i1}, S_{i2}, \dots, S_{ij}, \dots, S_{ip}\}$ is determined by the values of design variables (Boolean, registers, memory). The oriented graph arcs are represented by a set of software blocks:

$$B = \{B_1, B_2, \dots, B_i, \dots, B_n\}; \bigcup_{i=1}^n B_i = B; B_i \cap B_j = \emptyset.$$

The assertion $A_i \in A = \{A_1, A_2, \dots, A_i, \dots, A_n\}$ can be inserted to the end of each block B_i – a sequence of code statements which determines the state of the graph node $S_i = f(T, B_i)$ depending on the test pattern $T = \{T_1, T_2, \dots, T_i, \dots, T_k\}$. The monitor, uniting an assertions of incoming arcs $A(S_i) = A_{i1} \vee A_{i2} \vee \dots \vee A_{ij} \vee \dots \vee A_{iq}$ can be put on each node.

The model of HDL-code, represented in the form of the ABC-graph, describes not only software structure, but also test segments of the functional coverage, generated by using software blocks, incoming to the

given node. The ABC-graph makes possible the following: 1) to estimate the software quality via diagnosability design; 2) to minimize the costs for generating tests, diagnosing and correcting the functional failures by using assertions; 3) to optimize test synthesis via coverage all arcs and nodes by a minimum set of activated test paths. For instance, the minimal test for the above mentioned ABC-graph has six segments, which activate all existent arcs and nodes, shown in Fig. 1.



$$\begin{aligned}
 B &= (B_1 B_3 B_9 \vee (B_2 B_7 \vee B_1 B_5) B_{11}) B_{13} \vee \\
 &\vee ((B_1 B_4 \vee B_2 B_6) B_{10} \vee B_2 B_8 B_{12}) B_{14} = \\
 &= B_1 B_3 B_9 B_{13} \vee B_2 B_7 B_{11} B_{13} \vee B_1 B_5 B_{11} B_{13} \vee \\
 &\vee B_1 B_4 B_{10} B_{14} \vee B_2 B_6 B_{10} B_{14} \vee B_2 B_8 B_{12} B_{14}.
 \end{aligned}$$

Figure 1. Example of ABC-graph for HDL-code

2. Design for diagnosability

Diagnosability is the relationship $D = N_d / N$ between the recognized faulty blocks amount N_d , (when there are not equivalent components, or the diagnosis depth is equal to 1), and the total number N of HDL-blocks.

For the expense E evaluation of the TAB-matrix model for detecting functional failures, it can use the pair test-assertions efficiency for a given diagnosis depth. Criterion E functionally depends on the relation between the ideal $\lceil \log_2 N \rceil \times N$ and real $|T| \times |A| \times N$ memory sizes or resources (where $|T|$ – the test length, $|A|$ – a number of assertions) for the corresponding TAB-matrices, which compose the relative expense reduced to 0-1 intervals:

$$E = \frac{\lceil \log_2 N \rceil \times N}{|T| \times |A| \times N} = \frac{\lceil \log_2 N \rceil}{|T| \times |A|}.$$

The general diagnosis quality criterion depends on expense E and diagnosability D :

$$Q = E \times D = \frac{\lceil \log_2 N \rceil}{|T| \times |A|} \times \frac{N_d}{N}.$$

The TAB-matrix diagnosis quality is the ratio of the bit number needed for identification (recognition) of all blocks $\lceil \log_2 N \rceil$ related to the real number of code bits, presented by the product of test length and number of assertions $|T| \times |A|$. If the first part E of quality criterion Q is equal to 1 and every block with functional failures is recognized in the field of the rest components $N_d = N$, it means a test and assertions are optimal, that gives the best quality criterion of diagnosis model $Q=1$.

The purpose of the ABC-graph analysis is structured evaluation of assertion monitor placement, which make possible to obtain maximal diagnosis depth of faulty blocks. Diagnosability of the ABC-graph is a function depending on the number N_n of transit not ended nodes where only two adjacent arcs exist, one of which is incoming, other one is outgoing. Such arcs form paths though the node without fan-in and fan-out branches (N is the total arcs number in the graph):

$$D = \frac{N - N_n}{N}.$$

The estimation N_n is the number of unrecognizable or equivalent functional blocks. Potential installation of additional monitors for improving diagnosability of failure blocks is pure transit nodes composed N_n . The diagnosis quality criterion of the ABC-graph takes the form:

$$Q = E \times D = \frac{\lceil \log_2 N \rceil}{|T| \times |A|} \times \frac{N - N_n}{N}.$$

The last expression produces some practical rules for synthesis of diagnosable HDL-code: 1) Test or testbench must create a minimal number of single activation paths, covered all the nodes and arcs in the ABC-graph. 2) The base number of monitors equals to the end node number of the graph with no outgoing arcs. 3) An additional monitor can be placed on each not ended node, which has one incoming and one outgoing arc. 4) Parallel independent code blocks must have n monitors and a single concurrent test, or one integrated monitor and n serial tests. 5) Serially connected blocks have one activation test for serial path and $n-1$ monitor, or n tests and n monitors. 6) The graph nodes, which have more than 1 number of input and output arcs, create good conditions for the diagnosability of the current section by single path activation tests without installation additional monitors. 7) The test pattern or testbench has to be 100% functional coverage for the nodes of the ABC-

graph. 8) Diagnosis quality criterion as a function depending on the graph structure, test and assertion monitors can always be increased close to the 1-value. For this purpose there are two alternative ways. The first one is increasing test segments by activating new paths for recognition equivalent faulty blocks without increasing assertions, if the software graph structure allows the potential links. The second way is adding assertion monitors on transit nodes of the graph. A third so called hybrid variant is possible, based on the joint application of two above-mentioned ways.

3. Multilevel diagnosis method of digital system

Multilevel model of the multi-tree B (Fig. 2) is shown, where each node is represented by digital or computer system component, which has a three-dimensional activation TAB-matrix of functional unit subcomponents.

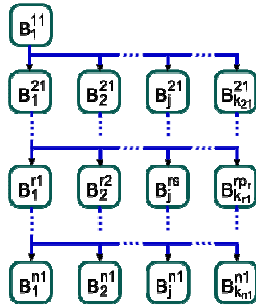


Figure 2. Diagnosis multitree model

The outgoing from the node arcs are transitioning to a lower detailed level in diagnosing process, when replacing faulty block is too expensive:

$$B = [B_{ij}^{rs}], \text{card}B = \sum_{r=1}^n \sum_{s=1}^{m_r} \sum_{i=1}^{p_{rs}} \sum_{j=1}^{k_{rs}} B_{ij}^{rs},$$

where n is a number of diagnosis multi-tree levels; m_r is a number of functional units or components at the level r ; k_{rs} (p_{rs}) is a number of components (test length) in the table B^{rs} ; $B_{ij}^{rs} = \{0,1\}$ is a component of an activation table, which is defined by 1-unit the detected faulty functionality under the test segment T_{i-A_i} relatively to the observed monitor-assertion A_i . Each node-table has the number of outgoing down arcs equal to the number of functional components, which are represented by activation TAB-matrixes as well.

Method for faulty blocks diagnosis Hardware-Software HS-system, based on multi-tree model,

allows creating the universal engine in form of algorithm (Fig. 3, block 6) for traversal of tree branches on the depth, specified a priority:

$$B_j^{rs} \oplus A^{rs} = \begin{cases} 0 \rightarrow \{B_j^{r+1,s}, R\}; \\ 1 \rightarrow \{B_{j+1}^{rs}, T\}. \end{cases}$$

Here xor-vector-operation is executing the matrix columns with the assertion (output) response vector A^{rs} , which is determined by the real (m) and gold (g)

functionality responses under test patterns based on xor-operation: $A_i^{rs} = m_i^{rs} \oplus g_i^{rs}, i = \overline{1, k_{rs}}$. If all

coordinates of vector xor-sum $B_j^{rs} \oplus A^{rs} = 0$ is equal

to zero then one of the following action is performed: the transition to the activation matrix of the lower level

$B_j^{r+1,s}$ or repair of the functional block $B = B_j^{rs}$.

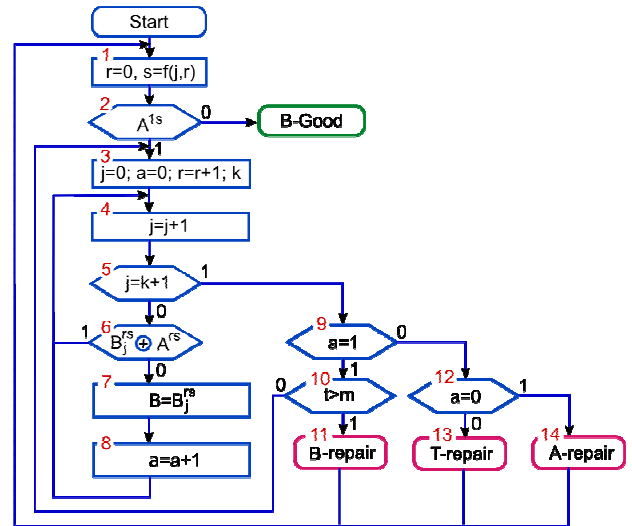


Figure 3. Engine for traversal of diagnosis multitree

One of two analysis ways is executed, what is the most important: 1) the time ($t > m$, block 10) – then repair of faulty block is performed; 2) the money ($t < m$) – then a transition down is specify more exact fault location, because replacement of smaller block decreases the repair cost. If at least one coordinate of the resulting xor-sum vector is equal to one $B_j^{rs} \oplus A^{rs} = 1$, then transition to the next matrix column is performed. When all coordinates of the assertion vector are equal to zero $A^{1s} = 0$, fault-free

state of a HS-system is defined. If all vector sums by executing TAB-matrix column are not equal to zero $B_j^{rs} \oplus A^{rs} \neq 0$, it means a test, generated for detecting

the given component of functionality has to be corrected. If more than one vector sum obtained by executing TAB-matrix column are equal to zero $B_j^{rs} \oplus A^{rs} = 0$, it means an assertion engine, created

for detecting the given component of functionality on the represented test has to be supplemented an extra assertion monitor. So, the TAB-engine has four end-nodes, where one of them is B-good which indicates successful finishing of the testing. Another three means the intermediate results in the test process, which is necessary to take into account for the increasing a test quality and diagnosis depth by using extra assertions and/or additional test segment generation.

Thus, the graph shown in the Fig. 2, allows realizing efficient infrastructure IP for the complex technical systems. The advantages of the TAB-engine, which is invariant to the hierarchical levels, are the simplicity of preparation and presentation of diagnostic information in the form of minimizing activation table of functional blocks on the test segments.

Technological model of infrastructure for embedded testing, diagnosis and repairing of faulty blocks (Fig. 4) has three components: 1. Block testing (Unit Under Test – UUT) by using a reference gold model (Model Under Test – MUT) for generating the assertion response vector m_a which dimension corresponds to the number of test patterns. 2. Searching faulty blocks based on analysis of the TAB-matrix. 3. Repairing faulty blocks by replacing the good components from the Spare Primitives.

Process model of embedded IP service operates in real time and allows supporting good state of the HS-system without human actions distantly. The proposed algorithm or TAB-engine for analysis of TAB-matrix, as well as the introduced diagnosis quality criteria allow solving the problems of quasi-optimal coverage for software and hardware blocks by test and assertions. The model shown in Fig. 4 allows effectively servicing complex HS-system. The advantages of this functionality that is invariant to the hierarchical levels, lies in simplification of preparation and presentation of diagnostic information in the form of minimizing activation table for functional blocks by using test segments.

Practical implementation of models and verification methods is integrated into the simulation environment Riviera of Aldec Inc., Fig. 5. New assertion and

diagnosis modules, added into the system, improved the existing verification process, which allowed 15% reduces the design time of digital product.

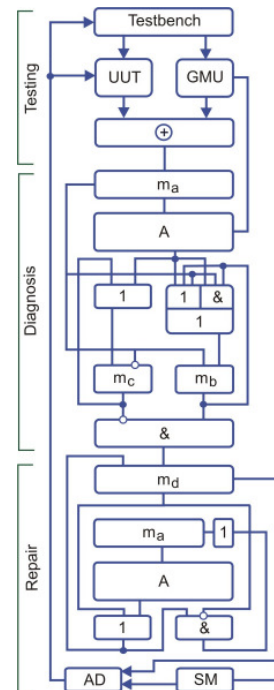


Figure 4. Model for embedded testing HS-components

Actually, application of assertions makes possible to decrease the length of test-bench code and considerably reduce (x3) the design time (Fig. 6), which is the most expensive. Assertion engine allows increasing the diagnosis depth of functional failures in software blocks up to level 10-20 HDL-code statements.

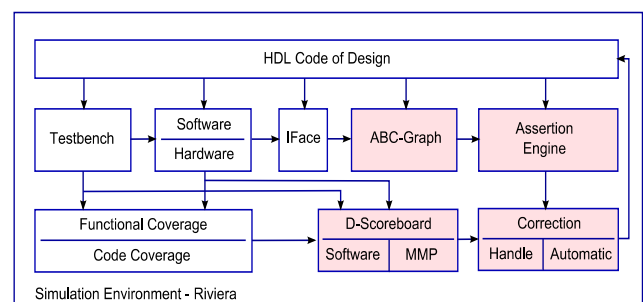


Figure 5. Implementation of results in the system Riviera

Due to the interaction of simulation tools and assertion engine, automatically placed inside the HDL-code, an access of diagnostic tools to the values of all

internal signals is appeared. This allows quickly identifying the location and type of the functional failure, as well as reduce the time of error detection in the evolution of product with top-down design. Application of assertion for 50 real-life designs (from 5 thousand up to 5 million gates) allowed obtaining hundreds of dedicated solutions, included in the verification template library VTL, which generalizes the most popular on the market EDA (Electronic Design Automation) temporal verification limitations for the broad class of digital products. Software implementation of the proposed system for analyzing assertions and diagnosing HDL-code is part of a multifunctional integrated environment Aldec Riviera for simulation and verification of HDL-models.

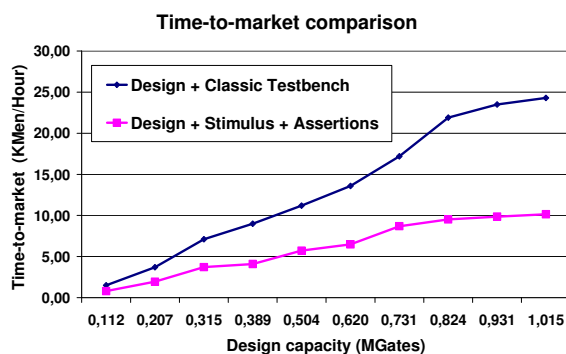


Figure 6. Comparative analysis of verification methods

High performance and technological combination of assertion analysis system and HDL-simulator of Aldec Company is largely achieved through integration with the internal simulator components, including HDL-language compilers. Processing the results of the assertion analysis system is provided by a set of visual tools of the Riviera environment to facilitate the diagnosis and removal of functional failures. The assertion analysis model can also be implemented in hardware with certain constraints on a subset of the supported language structures. Products Riviera including the components of assertion temporal verification, which allow improved the design quality for 3-5%, currently, occupies a leading position in the world IT market with the number of system installations of 5,000 a year in 200 companies and universities in more than 20 countries.

4. Conclusion

1. Infrastructure and technology for digital systems analysis are presented. Proposed transactional graph model and method for diagnosis of digital systems-on-

chips are focused to considerably reducing the time of faulty block detection and memory for storing the diagnosis compact matrix describing ternary relations in format: the monitor-oriented test-segments which detect faulty functional components of the Hardware-Software system.

2. New diagnosis quality criterion as a function depending on the graph structure, test, and assertion monitors is proposed. For this purpose there are two alternative ways. It allows making good choices in diagnosability improving by increasing test segments set for recognition equivalent faulty blocks or adding assertion monitors on transit nodes of the activation HDL-code graph.

3. An improved TAB-engine or algorithm for functional failure detection in software or hardware is proposed. It is characterized by using the xor-operation, which makes possible to improve the diagnosis performance for single and multiple faulty blocks on the basis of parallel analysis of the TAB-matrix, boundary scan standard IEEE 1500, and vector operations called and, or, xor.

4. A model for diagnosing the functionality of system-on-chip in the form of multi-tree and method for tree traversal, implemented in the engine for detecting faulty blocks with given depth, are developed. They considerably increase the performance of software and hardware Infrastructure IP.

5. Test verification of the diagnosis method is performed by three real case studies, presented by SoC components of a cosine transform filter, which showed the consistency of the results in order to minimize the time of faulty blocks detection and memory for storing diagnostic information, as well as increase the diagnosis depth of digital unit.

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