Adjustable Output Voltage-Range and Slew-Rate Trapezoidal Waveform Generator with Harmonics-Reduction Ability

Mariusz Jankowski

Abstract— **The paper presents a circuit designed to provide trapezoidal output voltage signal, scalable in term of output voltage-range and slew-rate value. Additionally, the circuit is endowed with signal edge rounding functionality, realized by output voltage buffer itself. Schematics, way of operation, and simulation results are presented.**

Index Terms — **Trapezoidal waveform generator, voltage discriminator, slew-rate control, edge rounding.**

I. Introduction

ANALOG signal generation may be a complex task, depending on analog system requirements. Process of signal forming tends to be a multi-step operation due to special features imposed on the generated signal. On the other hand, complicated multi-stage signal forming circuitry imprints its own non-idealities into the resulting output signal.

Thus, it is good approach to reduce number of signal processing stage, e.g. by making them multi-role ones. One such solution is presented in the paper. The described circuit generates trapezoidal voltage signal with adjustable slew-rate and voltage-range. Such signals are used e.g. by wireless transmission systems, including automotive applications. Signal rounding enables avoiding of high frequency noise at the moments of rapid slew-rate value changes of transmitted signals. Such occurrence may violate transmission and EMC rules and eliminate circuit from commercial use.

II. Circuit Structure Overview

The presented circuit consists of two main stages. The first one provides trapezoidal constant slew-rate voltage signal ranging from ground to supply voltage.

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M. Jankowski is with the Department of Microelectronics and Computer Science, Technical University of Lodz, ul. Wolczanska 221/223, B18, 90-924 Lodz, POLAND; e-mail: jankowsk@dmcs.p.lodz.pl.

The following stage serves as: a buffer for current-mode output of the preceding stage, an output signal voltage-range limiter and edge-rounder. Fig. 1 presents general view of the circuit structure, with additional OPAMPs serving as sources of virtual ground and supply voltages.

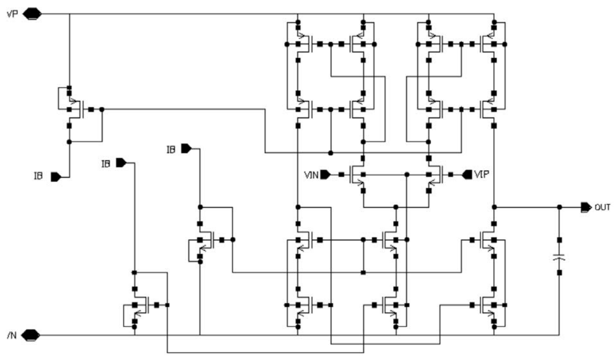

Fig. 1. General view of the waveform generator

III. Trapezoidal Signal Generation

Trapezoidal signal generation used in the circuitry is based on principle of consecutive charging and discharging of capacitor with constant value currents. Such operation can be performed by a variety of circuits [1]. The commonly used structure is the output stage consisting of current mirrors and load capacitors.

Exemplary solutions are shown in paper [2]. One of them is just a kind of modified OTA circuit [4], presented in Fig. 2. It is equipped with two bias current inputs – one for general circuitry biasing and other for defining slew-rate value. Another solution presented in [2] consists of current mirrors and current-flow cutting switches.

In the solution presented in this paper a similar solution is used. The one difference is that the new generation stage utilizes current-flow bypassing switches, which do not force current-flow extinguishing process during switching, but just reroute it, additionally switching down inputs of corresponding mirror inputs (Fig. 3). Such approach makes the circuitry power consumption more stable.

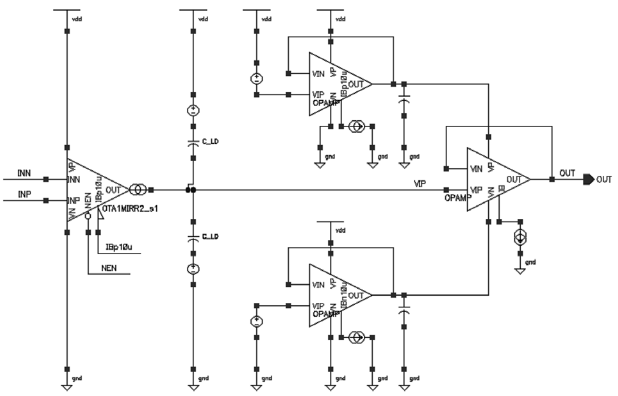

Fig. 2. Modified OTA serving as capacitor feeding circuitry

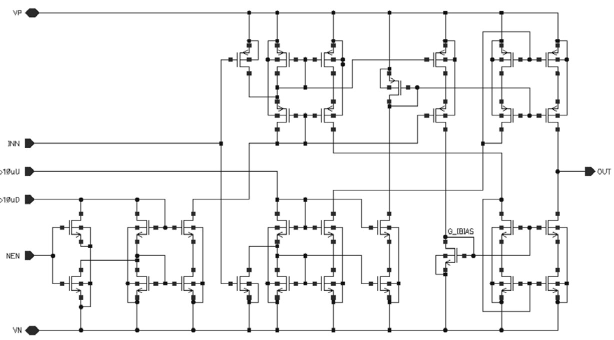

Fig. 3. Trapezoidal signal generation circuitry

Other modification is presence of two slew-rate defining inputs, which enables generation of non-symmetrical signal shapes like triangle or saw-tooth – like. The stability of slew-rate value of the output signal depends on output impedance of current mirrors utilized in the output stage as well as quality of available capacitors. In presented solution cascode mirrors are used. If higher quality output signal is required, regulated-cascode circuits can be used.

IV. Signal Rounding and Voltage-range Limitation

The signal rounding and voltage-range limiting procedures are in fact performed by one stage. The stage is a direct concatenation of two simple OPAMPs, one equipped with NMOS differential pair and one with PMOS differential pair. These OPAMPs are connected at inputs and output points.

In a way they form a kind of simple pseudo rail-to-rail OPAMP (Fig. 4), which is used as a simple non-inverting buffer. Another modification is power connection of the concatenated OPAMP to two voltage regulators, which provide virtual supply and ground voltages equal to limits that are to be imposed on the output voltage.

The virtual supply and ground regulators can be provided by quite simple OPAMP structures. Simple OPAMP solution presented in [3] and shown in Fig. 5, is enough for supplying the concatenated OPAMP due to its low power consumption level. Also simpler specialized solutions can be used, because full voltage-range operation of these OPAMP voltage-regulators is not required in presented application.

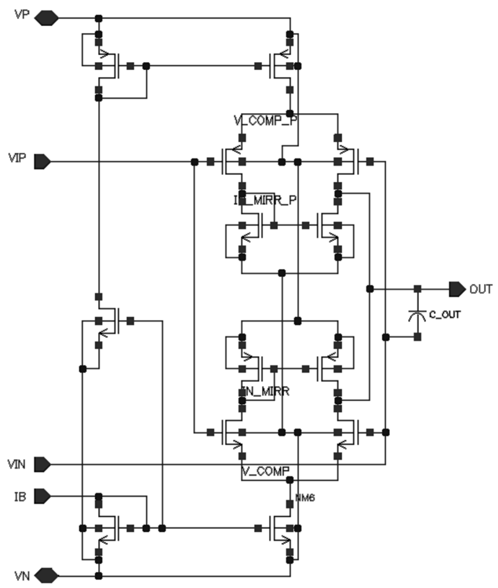

Fig. 4. Simple pseudo rail-to-rail OPAMP

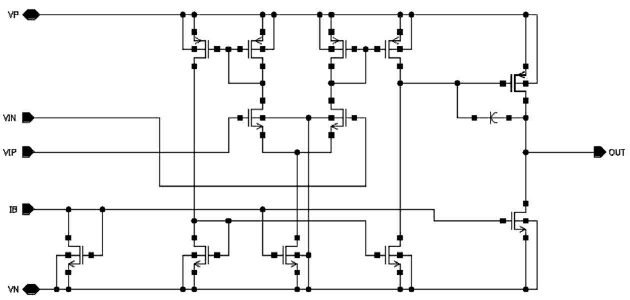

Fig. 5. Virtual ground and supply voltage-regulator

The voltage-limiting effect in the presented OPAMP is due to fact, that its input is fed with signal that over- and undershoots levels of, respectively, virtual supply and ground voltage. The input signal cannot pass supply voltage levels of the concatenated OPAMP and finally output signal stops following the input signal and stays blocked at virtual supply and ground levels.

Signal voltage rounding effect is achieved because when input voltage approaches one of virtual power levels, one of simple OPAMPs starts to gradually switch itself off, due to extinguishing of the current source that feeds OPAMP's differential pair. The distraction effect is deepened by input voltage to power voltage over- and undershoots. If these voltage level excesses are high enough, gradually more distorted output signal reaches level of virtual ground or virtual supply. The rounding effect is in fact a side effect related to non-ideal operation of simple OPAMPs inside the concatenated OPAMP.

Time domain simulation results are presented in Fig. 6. Output signals of both signal generation stages are shown.

The required rounding and voltage-range limiting functionality can be easily observed. It can be seen that the original trapezoidal signal also gets rounded but only when it reaches its maximum of minimum voltage level. When it leave its extreme voltage levels, no rounding happens.

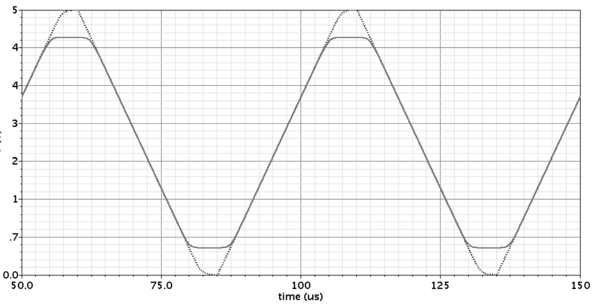

Fig. 6. Original (dotted line) and rounded (solid line) signal of the circuit

Fig. 7 shows first derivatives of the trapezoidal and rounded signal. It can be observed that the rounded signal is slightly deteriorated my means of slew-rate value. This phenomenon is related to fact that during operation of the concatenated OPAMP, its inside OPAMPs go off and on according to input voltage values, which influence the operating OPAMP part of the circuit. For numerous applications such signal behavior is acceptable, because it does not produce high frequency harmonics in rounded voltage signals. Critical points in original signal and their absence in the rounded signal can be observed in Fig. 8. It shows second derivatives of voltage signals.

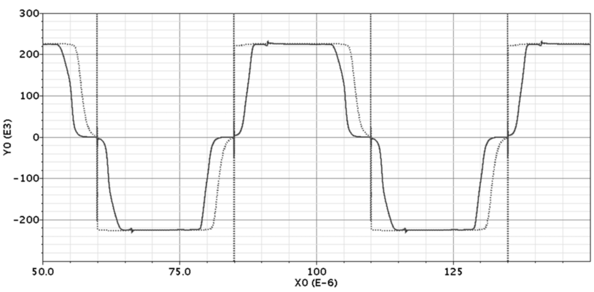

Fig. 7. Derivatives of original (dotted line) and rounded (solid line) signal of the circuit

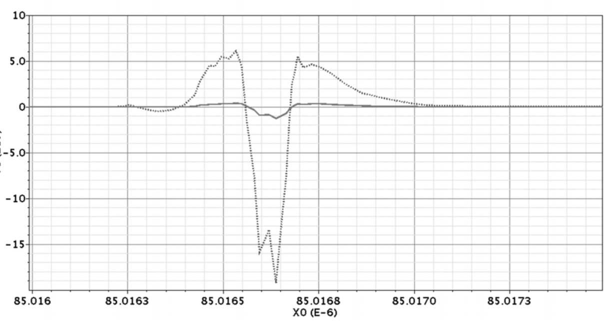

Fig. 8. Close-in view of derivatives of original (dotted line) and rounded (solid line) signals of the circuit

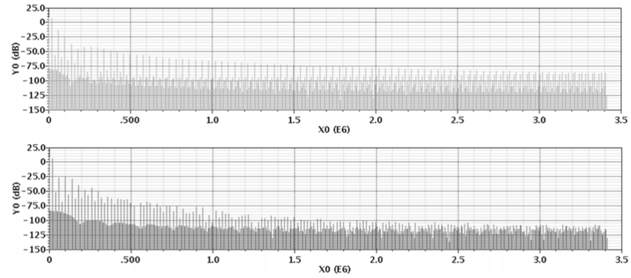

Fig. 9. DFTs of original (upper) and rounded (lower) generator signals

High value of second derivative marks time-points where high frequency harmonics in the voltage signals appear. It can be observed that maximum value of original signal second derivatives 15-20 time exceeds values observed for rounded signal.

Improvement in signal quality, understood as absence of high frequency incursions can be observed in the rounded output voltage signal.

More precise comparison of both signals is made my means of Discreet Fourier Transform (Fig. 9). The figure shows lower level of harmonics for the rounded signal.

V. Conclusion

The presented circuit shows simple but way of producing limited voltage-range regulated slew-rate trapezoidal signal generator equipped with signal rounding ability.

Structure of the proposed circuit is simple and consists of only two modules due to making them a multi-role blocks.

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Mariusz Jankowski received the M.Sc. and Ph.D. degrees in electronics engineering from the Technical university of Lodz, Lodz, Poland, in 1998 and 2003, respectively.
He is an Assistant Professor with the Department of Microelectronics and Computer Science at Technical University of Lodz, Poland. His research interests include analysis and design of mixed signal integrated circuits, including high-voltage applications, design of integrated 3D circuits, at present he works on 3D circuits and EMC issues. He is the author or coauthor of more than 30 publications, including two chapters in books.