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7th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)

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The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

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CONTENTS

Early Detection of Potentially Non-synchronized CDC Paths Using Structural Snalysis Technique

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Abstract

The number of independent clock domains found on the typical today's device is continuously growing. According to the latest industry research, the average number of clock domains on a single device is >15—20 and it becomes higher and higher from day to day. The CDC-related design flaws are also growing exponentially, appearing to be very dangerous as the roots of intermittent chip failures (can be found only in the silicon). Static CDC verification is considered as one of the first de-facto steps in today's SoC design methodology; only static techniques can work as soon as the RTL starts taking shape [1]. This paper discusses early detection of potentially missing synchronizers on clock domain crossing paths, using structural static analysis.

1. Introduction

The sections of logic elements that driven by clocks coming from different sources are called clock domains [2]. The signals that interface between asynchronous clock domains are called the clock domain crossing (CDC) signals (see Figure 1). The DATA_A signal is considered as an asynchronous signal into the receiving clock domain (no constant phase and time relationship exists between CLK_A and CLK_B).

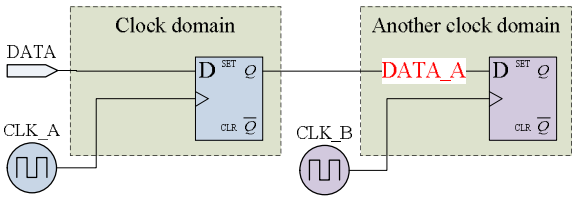

Figure 1. Clock domains and CDC signal

The nature of CDC bugs is intermittent; it simply means that a test suite can be successfully completed on a chip in the morning, but the same tests will complete with errors for the same chip in the afternoon [3]. Consider the simplest flip-flop example: such a flip-flop is located anywhere in the chip; the data signal for this flip-flop comes from the domain #A but the clock signal — from the domain #B... so whenever the setup or hold condition is violated, the flip-flop can go to one or to zero and it cannot be predicted (see Figure 2).

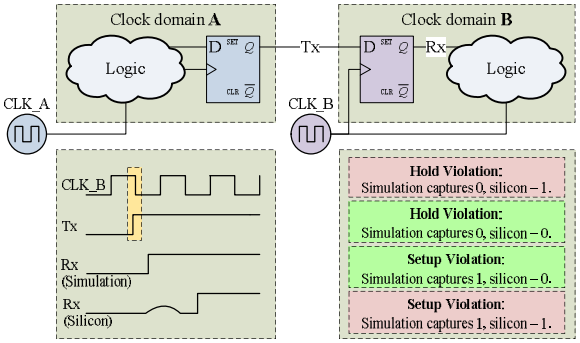

Figure 2. Possible metastability effects

The metastability term is used to describe what happens in digital circuits when the clock and data inputs of a flip-flop change values at approximately the same time. As shown in the Figure 2, it leads to the flip-flop output oscillating and not settling to a value within the appropriate delay window [4]. Such glitches happen in every design wherein two or more discrete systems communicate (the number of clock domains is greater than two).

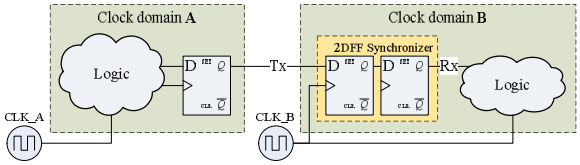

Figure 3. Simplest synchronizer (2 DFF in series)

Designers have actually found a solution to this and most of them is aware that metastability can be controlled using synchronizers on CDC signals (outputs of metastable registers are isolated so that the metastable value does not propagate to downstream logic) [5, 6]. Whenever there is a domain crossing signal, two flip-flops are placed one next to the other clocked by the same clock (see Figure 3). Such a synchronization structure decreases the MTBF (see Formula 1, where the f_{clk} – clock frequency, f_{in} – input signal frequency, t_d – duration of critical time window) from hours to thousands years [4].

$$MTBF = \frac{1}{f_{clk} \times f_{in} \times t_d}$$

Formula 1. Mean (average) time between failures.

Recent trends have been in favor of using static analysis tools [1]. But the biggest disadvantage of this approach is that it comes pretty late in the game — after the design has been synthesized, and the gate-level netlist is available (finding a CDC at this stage — which needs to be fixed — could set the design schedule totally off). So there is a need in static analysis tool that:

1. Performs lightweight synthesis (netlist synthesis emulation) directly from the RTL description — alongside with Verilog, VHDL or SystemVerilog compilation;
2. Reports domain crossing paths with potentially missing synchronizers, thus providing an obvious advantage in the form of early checking.

2. Automatic clock domains extraction

Clock domains extraction with further synchronizers detection is illustrated by the dataflow that is shown in the Figure 4. It involves several steps, starting with the compilation of the RTL description and creation of the database with netlist elements (lightweight synthesis), proceeding with special attributes assignment and their propagation through a design hierarchy (global clocks detection), and further manipulations with global clocks (clock domains look up).

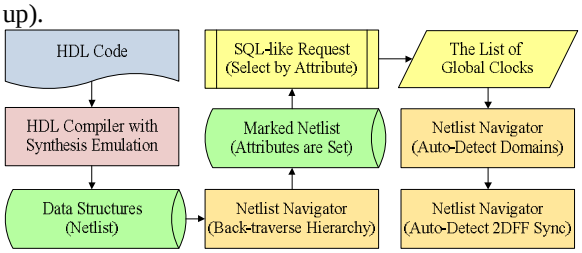

Figure 4. Clock domains and sync. detection dataflow

Detect global clocks in a design. Attributes are distributed through the design hierarchy (netlist): "DESIGN_CLOCK" attribute is back-propagated from each flip-flop clock pin. Since all the netlist elements were added to the database, it further can be used for selection by the particular attribute(s) presence (SQL-like request).

- The back-propagation of the attribute is terminated on the storage elements (flip-flops and latches) and tri-states. While back-propagation is stopped, it means that the signal which feeds the flip-flop clock pin is not an external input signal and thus it cannot be considered as a global clock.
- However, if the attribute reaches an external input pin (passes only through combinatorial logic, buffers and inverters), it is considered as a global clock – added to the list of global clocks (see Figure 5).

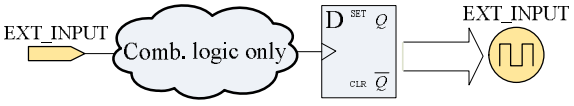

Figure 5. Global clock auto-detection

Extract clock domains. Clock domains can be detected when the list of global clocks is available; each global clock creates at least one separate clock domain. In order to detect clock domains, global clocks should be propagated through the design hierarchy (external input pins marked with the "DESIGN_CLOCK" attribute):

- Transparent logic. Combinatorial logic, latches and tri-states that happen on the attribute propagation path are considered as transparent objects.
- Flip-flops consideration. Each flip-flop that happens on the propagation path is added to the appropriate clock domain if

"DESIGN_CLOCK" attribute reaches its clock input pin; if a flip-flop clock pin is driven by the output of another flip-flop which already belongs to a clock domain, the flip-flop is also added to the same clock domain (Figure 6)

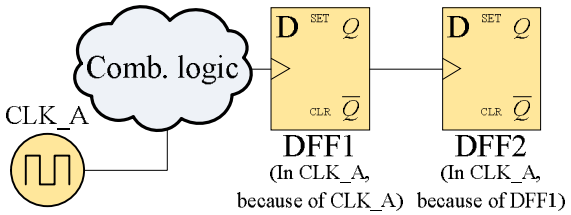

Figure 6. Flip-flops added to corresp. domains

- Derived domains. If two or more clock signals are propagated through the same combinatorial logic or multiplexer then the output of this logic or multiplexer derives a new clock signal that correspondingly results in a new clock domain for subsequent connections (see Figure 7). Also if a clock signal is connected to the multiplexer select pin then the output of this multiplexer derives a new clock signal.

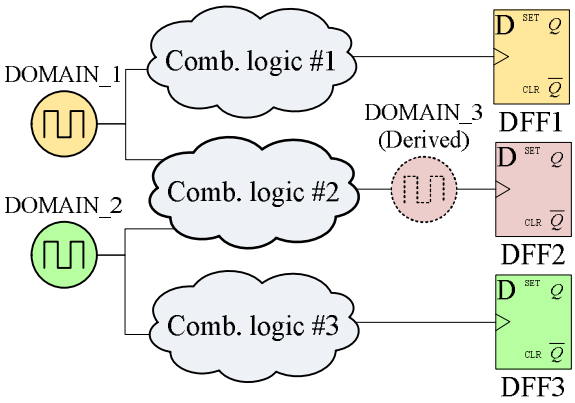

Figure 7. Derived domain

Design is considered to be in a single clock domain if clock domains were not detected.

3. Detecting potentially non-synchronized CDC paths

While the netlist is marked with clock domain-related attributes, the data about each flip-flop membership is available, it becomes possible to go further and detect synchronized and potentially non-synchronized CDC paths.

Detect 2DFF synchronizers. In order to be considered as 2DFF synchronizer, a pair of flip-flops should comply with the following restrictions:

1. Each flip-flop should receive the data only from the same clock domain (correct case – FF#1 receives data from domain A and transmits it to FF#2; incorrect case – FF#1 receives data from domain A, FF#2 receives data from domain B).
2. The outputs of the first and second flip-flops should not be connected to external design output(s) (in each case, the propagation should be blocked by non-clock input of another flip-flop(s) from the same domain).

It should be noted, that for some very high speed designs, the MTBF of a two-flop synchronizer is too short and a third flop is added to increase the MTBF to a satisfactory duration of time [7].

The paths which does not pass through a 2DFF synchronizer upon arrival into the new clock domain can be considered as potentially non-synchronized and reported as the design rule violations (synchronization errors class, see Figure 8).

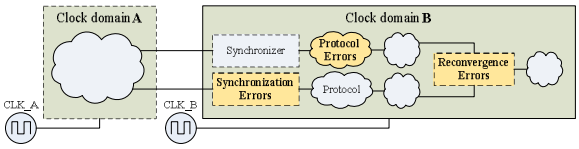

Figure 8. Synchronization and other CDC errors

4. Conclusion

Proposed structural analysis technique includes building of a netlist of the target design (lightweight synthesis is performed alongside with compilation) and performing further static analysis on this netlist. The novelty of the approach concerns propagation of various attributes through a design hierarchy: once the database with "netlist element"—"attribute(s)" relations is prepared, it can be used for SQL-like selections by attribute. The result of analysis is a summary of CDC paths in the design where the synchronization is potentially missing. Proposed technique deals only with the first of CDC problems list which can be detected with static analysis [8]:

1. Missing and incorrectly implemented synchronizers.
2. Correctly implemented synchronizer.

3. Complex synchronizers that require protocol verification.
4. Potential reconvergence problems.

To perform more complete CDC verification, formal analysis techniques should be used alongside with structural analysis (see Figure 9).

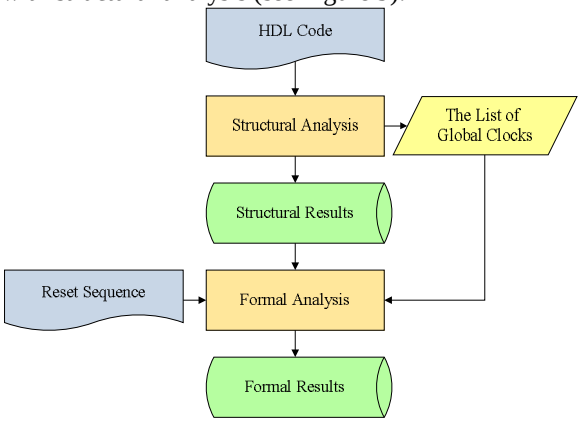

Figure 9. Structural and formal analysis

During the structural verification stage, it is possible to generate monitors for CDC transfer protocols. At the stage of formal verification [9], a simple reset sequence is used and cycle-based design analysis is performed (requires knowledge about clock periods of the asynchronous clocks). While a monitor is proven, it means that CDC protocol is followed.

5. References

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