

On the Problem of Selection of Modified Code with Summation of On-Bits for Logical Devices Test

Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov, Anton Bliudov

Abstract—Characteristics of modified codes with summation of on-bits (modified Berger codes) are analyzed during the experiment with the set of benchmarks. It is shown that the way of calculation of correction factor of modified Berger code has the fundamental importance and determines different properties of diagnostic system (both complexity of technical implementation and error detection on the outputs of checked device). Authors have developed the algorithm of selection of modified Berger code for diagnostic system formation that allows maximizing the error detection factor and minimizing the diagnostic system technical realization complexity factor.

Keywords—concurrent error detection system; code with summation; Berger code; modified Berger code; benchmarks; structural redundancy.

I. INTRODUCTION

Different methods of check circuits synthesis are used for the formation of reliable control systems on microelectronic and microprocessor component base [1 – 8]. In such circuits an emerging fault of the given class (the most often is the class of *stuck-at faults* [9]) appears on the outputs in the form of protective combination at least on one input combination [10] as they should be designed in self-checking way.

Classic codes with summation (Berger codes) [11] are often used for self-checking circuits synthesis as well as their modifications [12 – 15]. It is shown in [16] that code's characteristics of detection of errors in data bits determine properties of error detection on the outputs of tested object. In case of impossibility of detection of 100% of the given class faults methods of selection of groups of testable outputs [17] and of diagnostic object structure modification [18] are applied. Structural redundancy added to the diagnostic object or to the

check circuit depends on the rules of formation of check vector bits of code with summation [19].

The *modified code with summation of on-bits*, also known as $RS(m,k)$ -code (where m and $k = \lceil \log_2(m+1) \rceil$ – lengths of data and check vectors respectively) seems to be perspective for the task of check circuits organization [20].

First the way of $RS(m,k)$ -code formation was offered in [15]. It is based on the calculation of modified weight of data vector using the following formula:

$$W = r(\text{mod } M) + \alpha M, \quad (1)$$

where r – weight of data vector (number of on-bits); $M = 2^{\lceil \log_2(m+1) \rceil - 1}$ – modulo of weight calculation; expression $r(\text{mod } M)$ determines the smallest nonnegative residue of the value of weight by modulo M ; α – special correction factor – XOR sum of previously chosen data vector bits.

First papers in the field of $RS(m,k)$ -codes research concerned the analysis of characteristics of error detection in data vector with the only way of correction factor calculation: $\alpha = f_{k+1} \oplus f_{k+2} \oplus \dots \oplus f_{m-1} \oplus f_m$, where f_i ($i \in \{1; 2; \dots; m\}$) – data vector bit [15, 21, 22].

It is offered in [23] to form modulo modified codes with summation, also known as $RSM(m,k)$ -codes, that assume calculation of summary weight using formula (1) but with modulo value chosen from variety $M \in \{2; 4; \dots; 2^{\lceil \log_2(m+1) \rceil - 2}\}$.

Correction factor could be calculated as XOR sum of any bits of data vector, and total number of code formation ways is equal to $\sum_{j=1}^{m-1} \binom{m}{j} = 2^m - 2$ [20, 24]. In [25] describes the family of modulo modified codes with summation of on-bits with different methods of correction factor calculation.

It is stated in [20] that it does not matter which bits exactly are used for correction factor calculation in general case that considers all data vectors; only number of such bits acts. $RS(m,k)$ -codes have the same characteristics of error detection in data vectors in case of the same number of bits in correction factor calculation formula. Minimum number of undetectable errors as well as the minimum number of twofold undetectable errors has the $RS(m,k)$ -code, that uses $\frac{m}{2}$ data bits for α calculation (in case of even m) and $\frac{m+1}{2}$ – if m is odd.

It is stated in [20] that it does not matter which bits exactly are used for correction factor calculation in general case that considers all data vectors; only number of such bits acts. $RS(m,k)$ -codes have the same characteristics of error detection in data vectors in case of the same number of bits in correction factor calculation formula. Minimum number of undetectable errors as well as the minimum number of twofold undetectable errors has the $RS(m,k)$ -code, that uses $\frac{m}{2}$ data bits for α calculation (in case of even m) and $\frac{m+1}{2}$ – if m is odd.

The key properties of $RS(m,k)$ -codes should be stated; it is expedient to consider them during check system organization [26]:

Manuscript received November 18, 2016.

Dmitry Efanov with the “Automation and Remote Control on Railways” department, Emperor Alexander I St. Petersburg State Transport University, Russian Federation (corresponding author e-mail: tres-4b@yandex.ru).

Valery Sapozhnikov with the “Automation and Remote Control on Railways” department, Emperor Alexander I St. Petersburg State Transport University, Russian Federation.

Vladimir Sapozhnikov with the “Automation and Remote Control on Railways” department, Emperor Alexander I St. Petersburg State Transport University, Russian Federation.

Anton Bliudov with the “Automation and Remote Control on Railways” department, Emperor Alexander I St. Petersburg State Transport University, Russian Federation.

1. $RS(m,k)$ -codes detect all errors with odd multiplicity.
2. $RS(m,k)$ -codes do not detect about one half of possible symmetric errors in data vectors, also having some symmetric errors with even multiplicity undetectable.
3. $RS(m,k)$ -codes detect any monotonous errors except for some with multiplicity $d=M$.
4. $RS(m,k)$ -codes detect asymmetric errors with any multiplicities $d \leq M$ and does not detect some with multiplicities $d = M + 2j$, $j = 1, 2, \dots, q$, $q \leq \left\lfloor \frac{m-M}{2} \right\rfloor$.

All possible data vectors are rarely formed on the outputs of real circuits; this is explained by their functioning conditions (input combinations set) and their topology. So the rules of correction factor calculation are significant and have an influence on every particular case. Authors have posed the following problem: analyze the influence of correction factor calculation rules on the properties of error detection on benchmark outputs and on structural redundancy of diagnostic systems based on $RS(m,k)$ -codes.

II. STRUCTURAL SCHEME OF DIAGNOSTIC SYSTEM

Structural scheme of a diagnostic system of logical device $F(x)$ realizing the set of Boolean functions f_1, f_2, \dots, f_m is shown on Fig. 1.

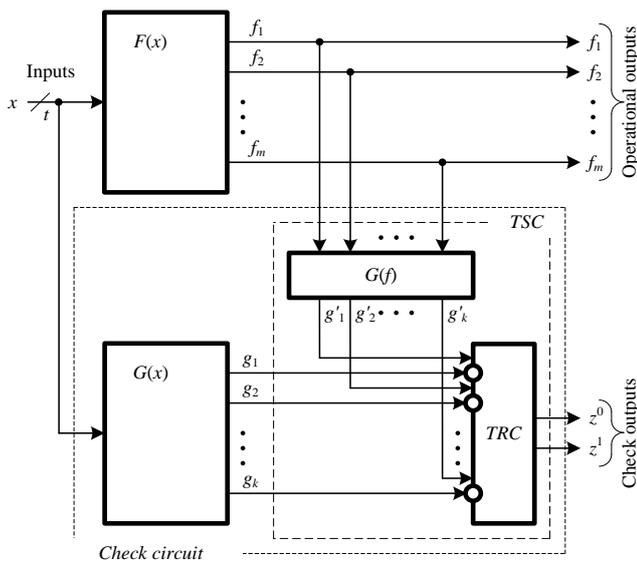


Fig. 1. Diagnostic system structural scheme

For the possibility of fault detection during operation it is added with on-line diagnostic system, which consists of check logic block, that calculates the set of check functions g_1, g_2, \dots, g_k , and checker TSC , comparing functions f_1, f_2, \dots, f_m and g_1, g_2, \dots, g_k [27, 28]. The simplest way of TSC implementation (for identifying if code words belong to the chosen code) is a cascade connection of check bits generators $G(f)$ [29] and comparator TRC . $G(f)$ calculates alternative check functions g'_1, g'_2, \dots, g'_k on the base of primary system functions; TRC compares signals of the same name g_j and g'_j ($j \in \{1; 2; \dots; k\}$) and forms the single check signal $\langle z^0 z^1 \rangle$ [30]. In case of correct operation of all system blocks a two-rail signal $\langle 01 \rangle$ or

$\langle 10 \rangle$ is formed; presence of in-phase signal $\langle 00 \rangle$ or $\langle 11 \rangle$ shows that a fault occurred in one of diagnostic system parts.

Comparator circuit of checker is standard; it is formed as compression scheme of two-rail signals. $k-1$ standard modules of two-rail signals compression (so-called two-rail checker, TRC , shown on Fig. 2) are needed for comparator circuit formation. Structure of other blocks of diagnostic system depends on the type of code it is based on. $G(f)$ is the coder of this code, that calculates check vector bits based on the values of operative outputs; $G(x)$ also forms check vector, but on the base of diagnostic system inputs.

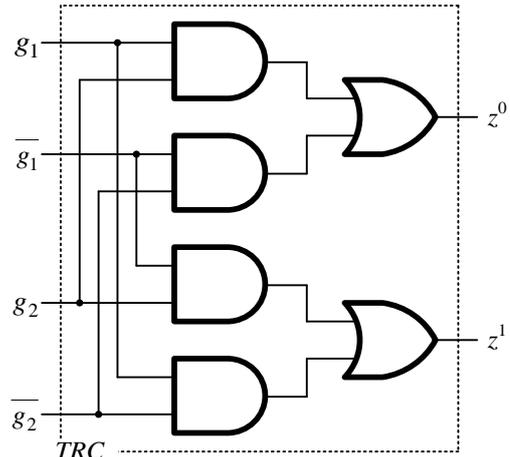


Fig. 2. Two-rail checker

III. INSTRUMENTAL BASE FOR EXPERIMENTS

The special software that allows to form descriptions of $G(x)$ and $G(f)$ blocks for the given circuit in *.pla format [31] was developed during experimental researches of characteristics of modified codes with summation. Then files were analyzed using *SIS* interpreter and complexity of their technical realization was determined; it was measured in standard conventional units of area occupied by the device on the chip with the use of *stdcell2_2.genlib* library of standard gates. Area of diagnostic system could be determined using the following formula:

$$L_{CED} = L_{F(x)} + L_{G(x)} + L_{G(f)} + 16k + 192(k-1), \quad (2)$$

where values $L_{F(x)}$, $L_{G(x)}$ and $L_{G(f)}$ characterize areas of respective blocks of diagnostic system, value $16k$ corresponds to the area occupied by inverter cascade, $192(k-1)$ – area of TRC comparator in *stdcell2_2.genlib* library.

Some benchmarks from *LGSynth 89* [32] base were analyzed. Circuits from this set are stored in *.netblif format which contains data about the circuit structure. This allowed analyzing of an influence of single stuck-at faults of inner gates on the outputs of the circuit and possible coding methods. All possible single stuck-at faults of inner gates were consistently set in the structure of circuit during the experiment; then all possible input combinations were set on its inputs. This allowed forming the varieties of data vectors containing an error (detectable or undetectable) and not containing. Then the total number of vectors containing an unde-

tectable error was determined. As a result a statistics was obtained for every circuit; it contained all undetectable errors with their multiplicities $d \in \{1;2;\dots;m\}$ and type (single, monotonous, symmetric, asymmetric [33]).

IV. RESULTS OF EXPERIMENTS FOR THE ANALYSIS OF CHARACTERISTICS OF ERROR DETECTION

The influence of single stuck-at faults of inner gates' outputs on the outputs of benchmarks was determined during the experiment for the analysis of characteristics of error detection using $RS(m,k)$ -codes. Stuck-at faults of inner gates were set in the structure consistently; then all possible input combinations were set. The way of correction factor α calculation for the $RS(m,k)$ -code corresponding to the given number of circuit outputs, and distributions of undetectable errors by type and multiplicity were formed.

Analyze the experiment results on the illustrative example of check of combinational circuit «cm162a» having 14 inputs and 5 outputs. Experiment has shown that 314067 monotonous, 1920 symmetric and 1344 asymmetric errors (total 317331) are formed on its outputs. Table 1 contains data about error detection characteristics of $RS(m,k)$ -codes with different ways of correction factor calculation.

TABLE I. ERROR DETECTION INDEXES OF $RS(m,k)$ -CODES APPLIED TO «CM162A» CIRCUIT

№	α	Undetectable errors			Error detection indexes		
		Uni-directional, $d=4$	Symmetrical, $d=2$	Total	$\nu_4, \%$	$\sigma_2, \%$	$\gamma_m, \%$
1	0, 31	6493	1920	8413	100	100	2.65117
2	1, 30	5597	1920	7517	86.201	100	2.36882
3	2, 29	224	1920	2144	3.45	100	0.67564
4	3, 28	672	1920	2592	10.35	100	0.81681
5	4, 27	224	1536	1760	3.45	80	0.55463
6	5, 26	672	1536	2208	10.35	80	0.6958
7	6, 7	6045	1536	7581	93.1	80	2.38899
8	8, 23	224	0	224	3.45	0	0.07059
9	9, 22	672	0	672	10.35	0	0.21177
10	10, 11	6045	0	6045	93.1	0	1.90495
11	12, 13	6045	384	6429	93.1	20	2.02596
12	14, 17	672	384	1056	10.35	20	0.33278
13	15, 16	224	384	608	3.45	20	0.1916
14	18, 19	6045	384	6429	93.1	20	2.02596
15	20, 21	6045	0	6045	93.1	0	1.90495
16	24, 25	6045	1536	7581	93.1	80	2.38899

Classic Berger codes does not detect all symmetric errors. For example it is 1920 errors for «cm162a» circuit (0.6% of all errors arising). Some $RS(m,k)$ -codes detect part of symmetric errors on the outputs of real combinational circuits. It should be noted that $RS(m,k)$ -code with data vector length $m=5$ (equal to the number of example circuit outputs) has only monotonous errors with multiplicity $d=4$ undetectable i.e. detects all asymmetric errors [26]. That is why some ways of correction factor calculation may cause worsening of $RS(m,k)$ -code error detection properties comparing to the Berger code.

Nevertheless such way of $RS(m,k)$ -code formation could be selected for any circuit that allows to detect more errors on its outputs than Berger code.

For the simplification of notations special designations for $RS(m,k)$ -codes correction factor calculation formulas are introduced in Table 1. Formulas are designated with decimal equivalents of binary values that define positions of bits used in correction factor calculation process. On-bits in this binary values correspond to the used bits. For example, decimal value 27 correspond to binary value <11011>; that means that $\alpha = f_1 \oplus f_2 \oplus f_4 \oplus f_5$. So the decimal value presented in table 1 uniquely determines one code from $RS(m,k)$ -codes with given data vector length.

Despite the fact that use of $RS(m,k)$ -codes does not ensure detection of 100% errors, change of correction factor calculation formula may minimize the number of undetectable errors and decrease the probability of their appearance for the given circuit by that. The following error detection indexes are determined in table 1:

- ν_d – ratio of multiplicity d unidirectional undetectable errors to the total number of given multiplicity monotonous errors in given circuit;
- σ_d – ratio of multiplicity d symmetrical undetectable errors to the total number of given multiplicity symmetric errors;
- γ_m – ratio of undetectable by the given code errors to the total number of possible errors of the outputs of the circuit.

Index γ_m allows to analyze the effectiveness of error detection by $RS(m,k)$ -codes with different way of correction factor calculation for any circuit (Fig. 3). Values of this index for «cm162a» circuit is from 2.65117% to 0.07059% for different ways of α calculation (Fig. 3).

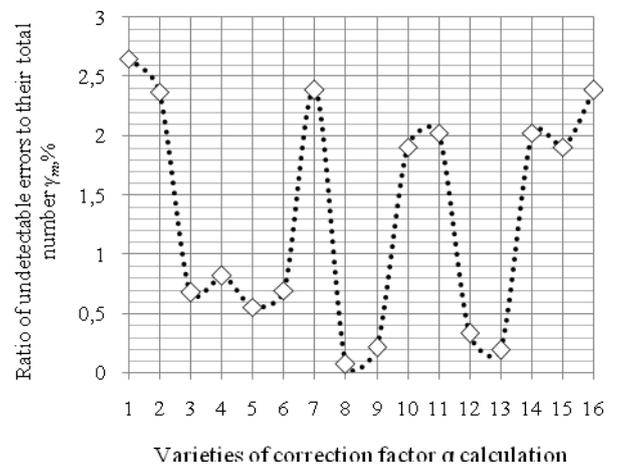


Fig. 3. Value of γ_m index for the benchmark «cm162a»

As an experiment has shown, this index is much less for other circuits: for example for the circuit «alu2» minimum value of γ_m is 0.01645%, and maximum – 0.12441%; for the circuit «x2» minimum is 0%, maximum – 0.73067%.

Let's mark some regularities that determine ways of formation of $RS(m,k)$ -codes with different error detection properties:

1) unlike in theoretical results in [20, 24 – 26], experiments have shown that for every benchmark the choice of specific bits of data vector matters and allows to decrease the number of undetectable errors even with the same number of them in correction factor calculation formula;

2) same distributions of undetectable errors on types and multiplicities are always obtained for the pairs of decimal equivalents of correction factor calculation and there is no case when the same distribution is obtained for odd types of correction factor calculation ways.

Item 1 could be illustrated with the following example. In table 1 the option with correction factor calculation using decimal equivalent 1 gives more undetectable errors than an option with decimal equivalent 8. In the first case $\alpha = f_1$, in the second $\alpha = f_4$. So the separate check of the fourth bit allows reducing the number of undetectable errors significantly.

The feature stated in the item 2 allows selecting from chosen ways of code formation the one that will improve system characteristics by one more criterion, for example, by technical implementation complexity.

V. RESULTS OF EXPERIMENTS WITH BENCHMARKS STRUCTURAL REDUNDANCY

Complexity of concurrent error detection system technical realization is evaluated by the area occupied by the device on chip (see formula 2). Authors have obtained description files of all diagnostic system components (Fig. 1) using the specially developed software complex. Then using the widely known interpreter SIS and standard gates library *stdcell2_2.genlib* [31] authors have got areas of diagnostic systems based on different modified codes with summation. Table 2 and Fig.4 contains results for the diagnostic system for the circuit «cm162a». Here L_{RS} is area total area of diagnostic system based on current $RS(m,k)$ -code; L_S – area of system based on Berger code. The last column is comparison of this two values; one can see that most $RS(m,k)$ -codes has about 5-10% advantage by this parameter. Experiments with other benchmarks have shown similar results.

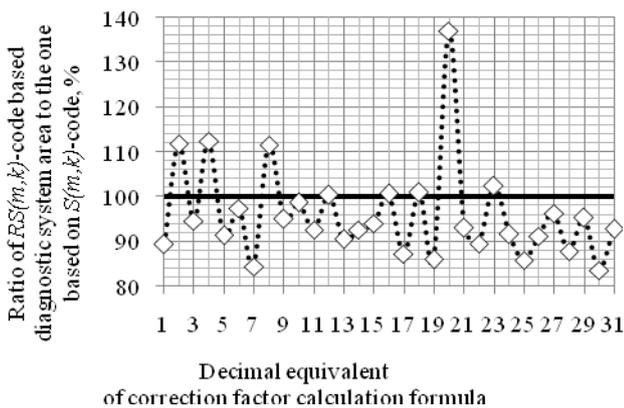


Fig. 4. Decrease of $RS(m,k)$ -code based diagnostic system area comparing to the use of Berger code

It should be noted that (unlike for error detection characteristics) different ways of correction factor calculation lead to different areas of diagnostic system. It is illustrated on Fig. 4:

axis of abscissa is for the decimal equivalent of α , axis of ordinates corresponds to the decrease of diagnostic system technical implementation area comparing to the use of Berger code. Most varieties of code formation give both effects of decrease of undetectable errors and area on the chip.

TABLE II.
AREAS OF DIAGNOSTIC SYSTEMS FOR THE CIRCUIT «CM162A»

α	$L_{RS(m,k)}$	$L_S(m,k)$	$\frac{L_{RS(m,k)}}{L_S(m,k)}, \%$
1	4320		89.404
2	5408		111.921
3	4576		94.702
4	5432		112.417
5	4416		91.391
6	4712		97.517
7	4080		84.437
8	5392		111.589
9	4592		95.033
10	4768		98.675
11	4480		92.715
12	4856		100.497
13	4376		90.563
14	4480		92.715
15	4544		94.04
16	4864	4832	100.662
17	4216		87.252
18	4880		100.993
19	4160		86.093
20	6624		137.086
21	4496		93.046
22	4328		89.57
23	4952		102.483
24	4432		91.722
25	4152		85.927
26	4408		91.225
27	4656		96.358
28	4248		87.914
29	4608		95.364
30	4040		83.609
31	4488		92.881

VI. ALGORITHM OF CODE CHOICE FOR DIAGNOSTIC SYSTEMS ORGANIZATION

Taking error detection features of $RS(m,k)$ -codes in diagnostic systems into account authors have developed the algorithm of choice of correction factor calculation rules. It allows forming the diagnostic system with minimum hardware redundancy and maximum error detection (Fig. 5).

Use of this algorithm allows simplification of diagnostic object topology analysis while choosing of modified code with summation for its check. Algorithm also considers minimization of probability of undetectable error appearance on its outputs. All distortions are detected after the transformation of diagnostic object topology into testable one. Use of $RS(m,k)$ -code property to detect all monotonous errors with multiplicities $d < 2^{\lceil \log_2(m+1) \rceil}$ it is possible to decrease the area of concurrent error detection system implementation comparing to known methods applied for transformation of circuits into

ones with monotonically independent outputs [18]. Considering properties of $RS(m,k)$ -code allows decreasing number of elements that should be reserved in the structure of diagnostic object. However, every certain case needs additional analysis of such transformation.

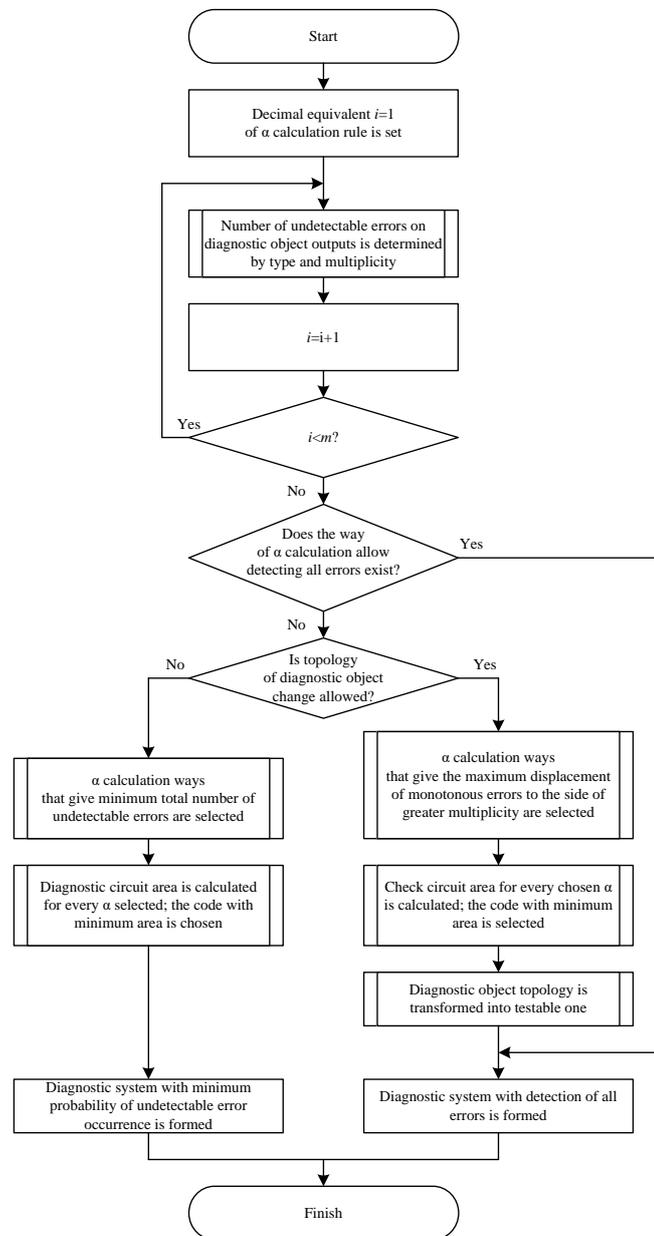


Fig. 5. Algorithm of $RS(m,k)$ -code choice

VII. CONCLUSIONS

Choice of correction factor calculation rules during $RS(m,k)$ -code formation has the fundamental importance for real logical devices: different distributions of undetectable errors could be obtained even with the same number of data bits used for this operation. Wherein because of better properties of symmetric errors detection of $RS(m,k)$ -codes comparing to Berger codes the total number of undetectable errors could be decreased in many cases. For some certain cases of logical

device topologies 100% error detection on its outputs could be gained by the use of $RS(m,k)$ -codes.

Also use of $RS(m,k)$ -codes in diagnostic system formation leads to decreasing of its area comparing to the use of Berger code, The algorithm developed by the authors allows synthesizing the diagnostic system for the given logical device considering minimum probability of appearance of undetectable errors on its outputs as well as 100% detection of any failures of inner gates of diagnostic object.

The presented results allow expanding the theory of logical devices concurrent error detection based on the use of anti-jamming codes with summation and to offer the designer a wider range of codes with simple formation rules.

REFERENCES

- [1] E.S. Sogomonyan, and E.V. Slabakov "Self-Checking Devices and Fault-Tolerant Systems" (in Russ.), Moscow: Radio & Communication, 1989, 208 p.
- [2] D.K. Pradhan "Fault-Tolerant Computer System Design", New York: Prentice Hall, 1996, 560 p.
- [3] M. Goessel, and E.S. Sogomonyan "Construction of Code-Disjoint Self-Parity Combinational Circuits for Self-Testing and Functional Diagnosis", *Automation and Remote Control*, 1996, vol. 57, issue 11, pp. 1660-1667.
- [4] R. Ubar, J. Raik, and H.-T. Vierhaus "Design and Test Technology for Dependable Systems-on-Chip (Premier Reference Source)", Information Science Reference, Hershey, New York, IGI Global, 2011, 578 p.
- [5] G.P. Aksjonova "Localization of faulty multi-output unit in discrete device", *Automation and Remote Control*, 2015, vol. 76, issue 2, pp. 304-310, doi: 10.1134/S0005117915020095.
- [6] G.P. Aksjonova "Increasing Resolvability for the Matrix Fault Localization Method", *Automation and Remote Control*, 2016, vol. 77, issue 8, pp. 1447-1452, doi: 10.1134/S0005117916080105.
- [7] S. Ostanin, A. Matrosova, N. Butorina, and V. Lavrov "A Fault-tolerant Sequential Circuit Design for Soft Errors Based on Fault-Secure Circuit", *Proceedings of 14th IEEE East-West Design & Test Symposium (EWDTS'2016)*, Yerevan, Armenia, October 14-17, 2016, pp. 607-610, doi: 10.1109/EWDTS.2016.7807676.
- [8] A. Matrosova, S. Ostanin, I. Kirienco, and E. Nikolaeva "A Fault-tolerant Sequential Circuit Design for SAFs and PDFs Soft Errors", *2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS)*, 4-6 July 2016, pp. 1-2, doi: 10.1109/IOLTS.2016.7604658.
- [9] P.P. Parkhomenko, and E.S. Sogomonyan "Technical Diagnosis Fundamentals (Diagnostic Algorithm Optimization, Apparatus Means)" (in Russ.), Moscow: Energoatomizdat, 1981, 320 p.
- [10] V.V. Saposhnikov, and V.I.V. Saposhnikov "Self-Checking Discrete Devices" (in Russ.), St. Petersburg: Energoatomizdat, 1992, 224 p.
- [11] J.M. Berger "A Note on Error Detecting Codes for Asymmetric Channels", *Information and Control*, 1961, vol. 4, issue 1, pp. 68-73, doi:10.1016/S0019-9958(61)80037-5.
- [12] H. Dong "Modified Berger Codes for Detection of Unidirectional Errors", *IEEE Transactions on Computers*, vol. C-33, June 1984, pp. 572-575.
- [13] B. Parhami "New Class of Unidirectional Error-Detection Codes", *Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Processors*, 14-16 Oct 1991 (ICCD '91), Cambridge, MA, pp. 574-577.
- [14] D. Das, and N.A. Touba "Weight-Based Codes and Their Application to Concurrent Error Detection of Multilevel Circuits", *Proceedings of 17th IEEE Test Symposium*, California, USA, 1999, pp. 370-376, doi: 10.1109/TEST.1999.766691.
- [15] V.B. Mekhov, V.V. Saposhnikov, and V.I.V. Saposhnikov "Checking of Combinational Circuits Basing on Modification Sum Codes", *Automation and Remote Control*, 2008, vol. 69, issue 8, pp. 1411-1422, doi: 10.1134/S0005117908080134.
- [16] D.V. Efanov, V.V. Sapozhnikov, and V.I.V. Sapozhnikov "On Summation Code Properties in Functional Control Circuits", *Automation and*

- Remote Control*, 2010, vol. 71, issue 6, pp. 1117-1123, doi: 10.1134/S0005117910060123.
- [17] M. Goessel, A.A. Morozov, V.V. Sapozhnikov, and VI.V. Sapozhnikov "Investigation of Combination Self-Testing Devices Having Independent and Monotone Independent Outputs", *Automation and Remote Control*, 1997, vol. 58, issue 2, pp. 299-309.
- [18] A. Morosow, V.V. Sapozhnikov, VI.V. Sapozhnikov, and M. Goessel "Self-Checking Combinational Circuits with Unidirectionally Independent Outputs", *VLSI Design*, 1998, vol. 5, issue 4, pp. 333-345, doi: 10.1155/1998/20389.
- [19] V.V. Sapozhnikov, VI.V. Sapozhnikov, D.V. Efanov, and M.R. Cherepanova "Modulo Codes with Summation in Concurrent Error Detection Systems. II. Decrease of Hardware Redundancy of Concurrent Error Detection Systems" (in Russ.), *Electronic Modeling*, 2016, vol. 38, issue 3, pp. 47-61.
- [20] A.A. Blyudov, D.V. Efanov, V.V. Sapozhnikov, and VI.V. Sapozhnikov "Formation of the Berger Modified Code with Minimum Number of Undetectable Errors of Data Bits" (in Russ.), *Electronic Modeling*, 2012, vol. 34, issue 6, pp. 17-29.
- [21] A.A. Blyudov, V.V. Sapozhnikov, and VI.V. Sapozhnikov. "A Modified Summation Code for Organizing Control of Combinatorial Circuits", *Automation and Remote Control*, 2012, vol. 73, issue 1, pp. 153-160, doi: 10.1134/S0005117912010122.
- [22] A. Blyudov, D. Efanov, V. Sapozhnikov, and VI. Sapozhnikov "Properties of Code with Summation for Logical Circuit Test Organization", *Proceedings of 10th IEEE East-West Design & Test Symposium (EWDTS'2012)*, Kharkov, Ukraine, September 14-17, 2012, pp.114-117, doi: 10.1109/EWDTS.2013.6673150.
- [23] A.A. Blyudov, D.V. Efanov, V.V. Sapozhnikov, and VI.V. Sapozhnikov "The Summation Codes for Organization of Control of Combinational Circuits", *Automation and Remote Control*, 2013, vol. 74, issue 6, pp. 1020-1028, doi: 10.1134/S0005117913060118.
- [24] D. Efanov, V. Sapozhnikov, VI. Sapozhnikov, and A. Blyudov "On the Problem of Selection of Code with Summation for Combinational Circuit Test Organization", *Proceedings of 11th IEEE East-West Design & Test Symposium (EWDTS'2013)*, Rostov-on-Don, Russia, September 27-30, 2013, pp. 261-266, doi: 10.1109/EWDTS.2013.6673133.
- [25] A.A. Blyudov, D.V. Efanov, V.V. Sapozhnikov, and VI.V. Sapozhnikov "On Summation Code of Unit Bits in Concurrent Error Detection Systems", *Automation and Remote Control*, 2014, vol. 75, issue 8, pp. 1460-1470, doi: 10.1134/S0005117914080098.
- [26] V.V. Sapozhnikov, VI.V. Sapozhnikov, and D.V. Efanov "Application of Codes with Summation for the Synthesis of Railway Automation and Remote Control Systems Based on Field-Programmable Gate Arrays" (in Russ.), *Automation on Transport*, 2015, vol. 1, issue 1, pp. 84-107.
- [27] M. Nicolaidis, and Y. Zorian "On-Line Testing for VLSI – A Compendium of Approaches", *Journal of Electronic Testing: Theory and Application*, 1998, vol. 12, issue 1-2, pp. 7-20, doi: 10.1023/A:1008244815697.
- [28] S. Mitra, and E.J. McCluskey "Which Concurrent Error Detection Scheme to Choose?", *Proceedings of International Test Conference*, 2000, USA, Atlantic City, NJ, 03-05 October 2000, pp. 985-994, doi: 10.1109/TEST.2000.894311.
- [29] D.V. Efanov "Synthesis of Modified Berger Code Checker Generators, on The Basis of Using the Properties of Linear and Simple Symmetric Functions" (in Russ.), *Proceedings of Petersburg Transport University*, 2014, issue №4, pp. 99-109.
- [30] P.K. Lala "Self-Checking and Fault-Tolerant Digital Design", San Francisco: Morgan Kaufmann Publishers, 2001, 216 p.
- [31] S. Yang "Logic Synthesis and Optimization Benchmarks: User Guide: Version 3.0", Microelectronics Center of North Carolina (MCNC), 1991, 88 p.
- [32] Collection of Digital Design Benchmarks [<http://ddd.fit.cvut.cz/prj/Benchmarks/>].
- [33] V.V. Sapozhnikov, VI.V. Sapozhnikov, and D.V. Efanov "Classification of Errors in Data Vectors of Systematic Codes" (in Russ.), *Izvestiya Vysshikh Uchebnykh Zavedeniy. Priborostroenie*, 2015, vol. 58, issue 5, pp. 333-343, doi: 10.17586/0021-3454-2015-58-5-333-343.