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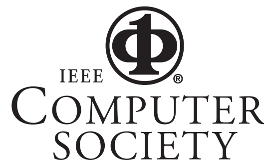

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CONTENTS

A Systematic Approach for Evaluating Satellite Communications Systems
Stefano Di Carlo, Paolo Prinetto, Alessandro Savino, Gabriele Tiotto, Paola Elia 13

Facilitating Testability of TLM FIFO: SystemC Implementations
Homa Alemzadeh, Marco Cimei, Paolo Prinetto, Zainalabedin Navabi 17

A Model for Resistive Open Recursivity in CMOS Random Logic
M. Renovell, M. Comte, N. Houarche, I. Polian, P. Engelke, B. Becker 21

An Optimized CLP-based Technique for Generating Propagation Sequences
F. Fummi, V. Guarnieri, C. Marconcini, G. Pravadelli 25

Validation of a Mixed-Signal Board ATPG Method
Val´erie-Anne Nicolas, Bertrand Gilles, Laurent Nana 29

A Low-Cost Optimal Time SICP air Generator
I. Voyiatzis, H. Antonopoulou 35

Selected Cost Factors in Modeling and Testing Hardware and Semiconductor Defects by Dynamic Discrete Event Simulation
Jack H. Arabian 41

HotSpot : Visualising Dynamic Power Consumption in RTL Designs
T. English, K.L. Man, E. Popovici and M.P. Schellekens 45

Characterization of CMOS Sequential Standard Cells for Defect Based Voltage Testing
A. Wielgus and W. A. Pleskacz 49

Testing the Control Part of Peripheral Interfaces
S. Zielski, J. Sosnowski 55

Concurrent Processes Synchronisation in Statecharts for FPGA implementation
Grzegorz Łabiak, Marian Adamski 59

Parallel Fault Simulation on Multi-core Processors
Dmitry E. Ivanov 65

Synthesis of control unit with code sharing and chain modifications
Alexander Barkalov, Larysa Titarenko, Jacek Bieganowski 68

FSMs Implementation into FPGAs with Multiple Encoding of States
Arkadiusz Bukowiec, Alexander Barkalov and Larysa Titarenko 72

Reduction in the number of PAL macrocells for the effective Moore FSM implementation
A. Barkalov, L. Titarenko, S. Chmielewski 76

Partial Reconfiguration of Compositional Microprogram Control Units implemented on an FPGA
R. Wisniewski, Alexander A. Barkalov, Larysa Titarenko 80

Coverage-Directed Verification of Microprocessor Units Based on Cycle-Accurate Contract Specifications
Alexander Kamkin 84

Code-Probability Entities for Constrained-Random Verification
Diana Bodyan, Ghennady Bodyan 88

Multidimensional Loop Fusion for Low-Power
Dmytro Lazorenko 92

A Synthesis of Common Models of Finite State Machines Using Input and Output Registers of Programmable Logic Devices
Adam Klimowicz, Valeri Soloviev 96

An advanced Method for Synthesizing TLM2-based Interfaces
Nadereh Hatami, Zainalabedin Navabi 104

Testing Combinational QCA Circuits
Mehdi Azimipour 108

Dependability and Complexity Analysis of Inter-channel Connection Schemes for "N out of M" System-on-Chip
Vyacheslav Kharchenko, Vladimir Sklyar, Georgiy Chertkov, Yuriy Alexeev, Ladislav Novy 113

Safety-Critical Software Independent Verification Based on Measurement of Invariants during Static Analysis
Sergiyenko Volodymyr, Zavolodko Valeriy 117

Designing High Productivity Parallel Algorithms with Algebraic and Heuristic Programming Techniques
Anatoliy Doroshenko, Mykola Kotyuk, Sergiy Nikolayev, Olena Yatsenko 121

Multiple Run Memory Testing for PSF Detection
I. Mrozek , V.N. Yarmolik, E. Buslowska 125

The analysis of the start up control parameters of the asynchronous electric traction motors
Gabriel Popa, Razvan A. Oprea, Sorin Arsene 131

A novel timing-driven placement algorithm using smooth timing analysis
Andrey Ayupov, Leonid Kraginskiy 137

Digital Lock Detector for PLL
Vazgen Melikyan, Aristakes Hovsepyan, Mkrtich Ishkhanyan, Tigran Hakobyan 141

Diagnosis of SoC Memory Faulty Cells for Embedded Repair
Vladimir Hahanov, Eugenia Litvinova, Karina Krasnoyaruzhskaya, Sergey Galagan 143

Testing Challenges of SOC Hardware-Software Components
Vladimir Hahanov, Volodimir Obrizan, Sergey Miroshnichenko, Alexander Gorobets 149

SoC Software Components Diagnosis Technology
Svetlana Chumachenko, Wajeb Gharibi, Anna Hahanova, Aleksey Sushanov 155

Vector-Logical Diagnosis Method for SOC Functionalities
Vladimir Hahanov, Olesya Guz, Natalya Kulbakova, Maxim Davydov 159

Testability analysis method for hardware and software based on assertion libraries
Maryna Kaminska, Roman Prikhodchenko, Artem Kubirya, Pavel Mocar......................... 163

Different observation time strategies of outputs in diagnostics of sequential digital circuits
Yu. A. Skobtsov, V. Yu. Skobtsov 168

Design and Implementation of a Parallel Adaptive Filter Using PBS-LMS Algorithm in a Convex Structure
Ali Fathiyan, M. Eshghi.. 173

An IEEE 1500 Compatible Wrapper Architecture for Testing Cores at Transaction Level
Fatemeh Refan, Paolo Prinetto, Zainalabedin Navabi 178

Power-Aware Embedded Software Design
Fabian Vargas, Cláudia A. Rocha, Luís Fernando Cristófoli, Luciano Rocha.................. 182

System Level Hardware Design and Simulation with System Ada
Negin Mahani, Parnian Mokri, Zainalabedin Navabi 190

Automating Hardware/Software Partitioning Using Dependency Graph
Somayyeh Malekshahi, Mahshid Sedghi, Zainalabedin Navabi 196

Reliable NoC Architecture Utilizing a Robust Rerouting Algorithm
Armin Alaghi, Mahshid Sedghi, Naghmeh Karimi, Mahmood Fathy,
Zainalabedin Navabi 200

Method for Modeling and Fault Simulation using Volterra kernels
Pavlenko V., Fomin O. 204

Parity Prediction Method For On-Line Testing a Barrel-Shifter
Drozd A., Antoshchuk S., Rucinski A., Martinuk A.. 208

RTL-TLM Equivalence Checking Based on Simulation
Nicola Bombieri, Franco Fummi, Graziano Pravadelli.. 214

Estimation of the FPAA specification with use of the Artificial Neural Network
Damian Grzechca, Tomasz Golonek 219

TUFFAN: A TLM Framework for Fast Architecture Exploration of Digital Systems
Sheis Abolmaali, Parisa Razaghi and Zainalabedin Navabi 223

Code Optimization for Enhancing SystemC Simulation Time
Homa Alemzadeh, Soheil Aminzadeh, Reihaneh Saberi, Zainalabedin Navabi 227

Automatic Test Pattern Generation Algorithm for Bridging Faults in Sequential Circuits
F. Podyablonsky, N. Kascheev 231

Test Suite Consistency Verification
Sergiy Boroday, Alexandre Petrenko, Andreas Ulrich 235

A 403-MHz Fully Differential Class-E Amplifier in 0.35 µm CMOS for ISM Band Applications
Ghulam Mehdi, Naveed Ahsan, Amjad Altaf, Amir Eghbali 239

Signal Processing Verification System for the Programmable Digital Matched Filter
Kharchenko H.V., Makovetskiy S.O., Tkalich I.O., Tsopa O.I., Vdovychenko Y.I 243

Building a Research Framework for Integrated Circuit Physical Design
Andrey Kamaev, Kirill Kornyakov, Iosif Meyerov, Alexey Sidnev, Artem Zhivoderov 251

A High-speed and High Precision IDDQ Measurement for Consumer and Communication SoCs
Yoshihiro Hashimoto, Yasuo Furukawa, Nguyen Ngoc Mai Khanh 254

Creating Test Environment for Consumer Video Devices
Andrew Johnson, Oleksandr Yegorov 258

An Efficient Inner (De)Interleaver Architecture for DVB-T systems
Mojtaba Rezayi, Mohammad Eshghi, and Hamid Reza Tanhaei 259

Redundant tests optimization
Dmitriy Speranskiy, Ekaterina Ukolova 263

Sensor Web and Grid Technologies for Flood Applications
N. Kussul, A. Shelestov, S. Skakun, Yu. Gripich 267

Persian Digit Recognition by Fourier Coefficients and Neural Networks
Nasim Kazemifard, Pedram Azimi, Saeed Mozaffari 271

Deterministic Distinguishing Tests for Given Fault of Discrete Device Synthesis
Dmitriy Speranskiy, Ivan Ukolov 276

Digital Implementation of General Regression Neural Network for Function Approximation
Applications **Saber Moradi, Mahmoud Tabandeh, Nasser Sadati** 281

Hardware Implementation of Exponential Function Using a Mathematical approach
Saber Moradi, Mahmud Tabandeh, Nasser Sadati 285

Automated Generation of Register Transfer Graph for Processors
Victor Belkin 289

One Approach to Fault Dictionary Size Reduction
Sergey Mironov, Dmitriy Speranskiy 295

Software engineering for recognition of electronic elements on the circuit board
Dmitry Bagayev, Pavel Khrustalev 301

Automatic Identification of Radiotelephone Transmissions in the Maritime Communication
Aleksandr V. Shishkin 306

QCA Parallel Prefix Adder Design
S. Arab, H. Aghababa, B. Forouzandeh 310

Simple march tests for PSF detection in RAM
Ireneusz Mrozek, Eugenia Buslowska 314

Improved Digital Signature Protocols On Elliptic And Hyperelliptic Curves
Dolgov V.I., Nelasa G.V 320

Cascade Structural Encoding of Binary Arrays
Vladimir Barannik, Anna Hahanova 322

Mapping DSP Algorithms into FPGA
Oleg Maslennikow, Anatolij Sergiyenko, Tatyana Lesyk 325

Precision of FTMpS reliability evaluation based on statistical experiments
Romankevych A., Romankevych V., Chernyavskaya K 331

Discrete model for dynamics analysis of the nonlinear oscillating systems with long transient processes and complicated nature
Zayats Vasyl 332

Deriving test suites for timed Finite State Machines
M. Gromov, D. Popov, N. Yevtushenko 339

Checker Design for Arbitrary Subset of Unordered Code Words
A. Matrosova, A. Malgin, N. Butorina 346

Multiple Stuck-at Fault and Path Delay Fault Testable Circuits
A. Matrosova, V. Andreeva, A. Melnikov, E. Nikolaeva 356

Minimizing Path Length in Digital Circuits Based on Equation Solving
N.Kushik, G.Sapunkov, S.Prokopenko, N.Yevtushenko 365

Utilizing HDL Simulation Engines for Accelerating Design and Test Processes
Najmeh Farajipour, S. Behdad Hosseini and Zainalabedin Navabi 371

Performance evaluation of In-Circuit Testing on QCA based circuits
Nasim Kazemifard, Maryam Ebrahimpour, Mostafa Rahimi, Mohammad Tehrani, Keivan Navi 375

Partitioning, Floor planning and detailed placement and routing techniques for schematic generation of analog netlist
Bikram Garg, Rajeev Sehgal, Ashish Agrawal, Amarpal Singh, Manish Khanna 379

Parallel computer emulator for digital devices modeling
Alexander Chemeris, Svetlana Reznikova 383

The Oscillations of an Overhead Contact Line Due to the Pantograph Raising
R.A. Oprea, G.C.Popa, S.Arsene 387

Reverse Semantic Quality Control Methods in Software Engineering
Vladimir L. Pavlov, Anatoliy Doroshenko, Konstantin Zhereb, Olexii Kuchaev 393

The Interplay of Reliability and Power Consumption in Design of SEU-Tolerant Latches for DSM Technology
M. Fazeli, S. G. Miremdi, A. Patooghy 399

Evaluation of a Concurrent Error Detection Technique Using Power Supply Disturbance Fault Injection
M. Fazeli, A. Patooghy and S.G. Miremadi 405

Embodying of High Performance Computation in Matlab Parallel Computing Toolbox for Detection of Spread Spectrum Signals
Bohdan Yavorskyy 411

Implementation of Finite State Machines on the Basis of anEmbedded Memory Block
V. Chapenko, K. Boule 414

On Macroplaces in Petri Nets
Andrei Karatkevich 418

Testing of hardware and software for FPGA-based critical systems
Yuliya Prokhorova, Sergey Ostroumov, Vladimir Sklyar 423

Luxury Wallet – new generation of the SoC based consumer products
Mikhail Lodygin 427

Descriptor Neural Networks And Singular Implicit Dynamic Systems
Rutkas A.A 429

Tools of the Computer Testing of Knowledge in Mathematical Disciplines
Shkil A.S., Naprasnsk S.V., Tsimbaluyk E.S., Garkusha E.V. 431

Software for problem components estimation in photometric stereo reconstruction
Bohdan Rusyn, Yuriy Lysak, Oleksiy Lutsyk 434

Method of Digital Treatment of the Information Received by Space Diversity Radars
Dmitriy Vasiliev 436

Verification Challenges of Clock Domain Crossings
D. Melnik, S. Zaychenko, O. Lukashenko........ 438

AUTHORS INDEX 441

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Vector-Logical Diagnosis Method for SOC Functionalities

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Abstract

Models and methods of vector-logical diagnosis of SoC functionalities in real time are proposed. Algebra-logical procedures of embedded fault diagnosis by means of DNF synthesis that forms all functionality diagnosis solutions are described. The method is based on use the fault detection table that is result of fault simulation.

1. Introduction

The research aim is development of embedded diagnostic service method of digital system-on-a-chip functionalities that is intended for faulty SoC component detection in real time.

The problems: 1) The state of the SoC I-IP market technology [1-5]; 2) Vector-logical (VL) method of the embedded service on basis of the coverage matrix [6,7]; 3) VL-method application for the diagnosis of SoC components; 4) Practical results of the investigations.

Modern technologies for the design of digital systems on chip [8-11] offer, along with the functional blocks of F-IP, the development of service modules I-IP oriented on the integrated solution of the problem of improving the project quality and Yield increasing in the manufacturing process, which is defined by implementation to silicon the following services [2,4,5]:

1) Monitoring the internal and output lines in the operation, verification and testing of functional blocks on the basis of IEEE 1500 boundary scan standard [12];

2) Testing the functional modules by applying different test generators, targeting fault detection or behaviour checking;

3) Diagnosis failures and defects by analyzing the information received from testing phase and by using the special embedded methods for troubleshooting based on the IEEE 1500 standard [12];

4) Repair of functional modules and memory after fixing a negative test result and determination the type and location of a defect at the executing diagnosis phase;

5) Built-in-measurement the main parameters and characteristics of SoC operation, allowing the temporal and volt-ampere measurements;

6) The reliability and fault tolerance of SoC in the operation, which are achieved by using diversification of functional blocks, duplication of them and recovery SoC efficiency in real time.

Subject to the SoC testing problem's state the fault diagnosis problem is considered below, defined by item 3; its solving enables to raise the quality of designed device essentially due to technological method of a single and multiple faults detection.

2. Vector-logical fault diagnosis method

The general role is assigned to the boundary scan technology [12] that is implemented into a chip now has to simplify solution of practically all problems of SoC Functional Intellectual Property Infrastructure. The access controller to internal lines and ports of the boundary scan register uses a cell or a stage of the register. In the aggregate a number of such cells, which provide monitoring in this case, must be equal to the quantity of problem observable lines of a project, which are necessary for exact establishment of a diagnosis.

An interesting solution of the diagnosis problem cab be obtained by means of the Boolean algebra and the fault detection table (FDT) M that is the Cartesian product of test T on a set of given faults F in the aggregate with the output response vector (ORV) V, where solving of the covering problem gives maximal exact result in the form of DNF and every term is possible variant of faults existance in a device. The diagnosis model is represented by the components:

$$A = \langle T, F, M, V \rangle,$$
$$T = (T_1, T_2, ..., T_i, ..., T_n);\ F = (F_1, F_2, ..., F_j, ..., F_m);$$
$$M = \left| M_{ij} \right|, i = \overline{1, n};\ j = \overline{1, m};\ V = (V_1, V_2, ..., V_i, ..., V_n);$$
$$V_i = R(T_i) \oplus R^*(T_i);\ \{V_i, T_i, M_{ij}, F_j\} \in \{0,1\}.$$

Coordinate value of the vector V is result of XOR operation execution at generalized model and real output responses.

The fault detection table processing for diagnosis obtainment is carried out by the algorithm, based on use of vector conjunction, disjunction and negation operations at FDT rows. Conjunction of the generalized vector that respects to "1" ORV coordinates and inverse generalized vector relative to zero ORV coordinates:

$$F = M^1 \wedge \overline{M}^0 = \left(\bigvee_{V_i=1} M_i \right) \wedge \left(\overline{\bigvee_{V_i=0} M_i} \right).$$

A single fault diagnosis differs by performing of conjunction operation (instead of disjunction) at all vectors, which correspond to "1" ORV coordinates.

$$F^S = M^1 \wedge \overline{M}^0 = \left(\bigwedge_{V_i=1} M_i \right) \wedge \left(\overline{\bigvee_{V_i=0} M_i} \right).$$

Example 1. Diagnose the multiple faults in a circuit by the vector-logical method; the fault detection table and the output response vector for a circuit are given:

M =

T_i / F_j	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}	V
T_1				1						1	1
T_2		1					1				0
T_3			1			1			1		0
T_4	1										0
T_5					1			1			1
T_6	1	1									0
T_7			1								0
T_8				1							1
T_9					1	1					0
T_{10}							1				0
T_{11}								1	1	1	1
M^1				1	1			1	1	1	1
M^0	1	1	1		1	1	1		1		0
$\overline{M}^0$	0	0	0	1	0	0	0	1	0	1	1
F	0	0	0	1	0	0	0	1	0	1	1

The fault detection table processing for obtainment F gives result, represented in four bottom rows of the matrix M. Last FDT row fixes the fact of existence faults in a circuit, which represented in vector or set-theory form $F = (0001000101) = \{F_4, F_8, F_{10}\}$.

To transform the obtained solution to DNF form FDT structure and a fault set, fixed in last table row, are used. The synthesis of disjunctive form gives the following result:

$$F = (F_4 \vee F_{10})(F_8)(F_4)(F_4 \vee F_{10}) =$$
$$= F_4F_8F_4F_4 \vee F_{10}F_8F_4F_4 \vee F_4F_8F_4F_{10} \vee F_{10}F_8F_4F_{10} =$$
$$= F_4F_8 \vee F_{10}F_8F_4 \vee F_4F_8F_{10} \vee F_{10}F_8F_4 = F_4F_8.$$

It is interested that due to writing faults in the form of DNF terms, covering all "1" ORV coordinates; the possibility to remove the fault $F_{10} \in F$ from a fault list appeared. The same result has obtained before at consideration of algebra-logical method of fault diagnosis.

The advantage of the vector-logical method is analysis efficiency of the fault detection table; computational complexity of the method is multiplicative dependence from fault quantity and test power: $Q = n \times m$. The method has to be used when "1" coordinates in the fault detection table prevail. The disadvantage of the method is impossibility of representation all fault combinations, which form terms for covering of "1" ORV coordinates.

Example 2. Carry out vector-logical diagnosis of circuit lines faults (Fig. 1) subject to the circuit structure.

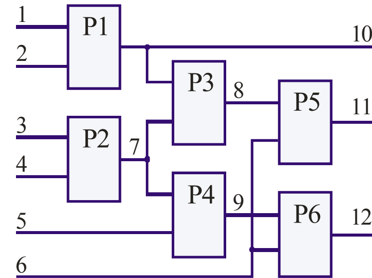

Fig. 1. An instance of a circuit for diagnosis

The fault detection table (first 5 rows) and the output response vector V correspond to the circuit structure.

M^* =

T_i / F_j	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}	F_{11}	F_{12}	Y_{10}	Y_{11}	Y_{12}	V
T_1	1	1		1	1	1	1		1	1	1	1	1	0	0	1
T_2		1	1		1			1	1	1	1	1	0	1		1
T_3		1					1		1	1	1	1	0	0	0	0
T_4									1	1	1	1	0	0	0	0
T_5	1	1	1	1			1	1		1	1	1	0	0	1	1
$\vec{Y}_{10}$	1	1								1						
$\vec{Y}_{11}$	1	1	1	1		1	1	1			1					
$\vec{Y}_{12}$			1	1	1	1	1		1			1				
M^1	1	1	1	1	1	1	1	1	1	1	1	1				
M^0		1					1		1	1	1	1				
$\overline{M}^0$	1		1	1	1	1		1								
F	1		1	1	1	1		1								
$M^1(\vec{Y})$	1	1	1	1			1	1	1	1	1	1				
$F(\vec{Y})$	1		1	1				1								

Use of the vector-logical method, based on the formula of obtainment M^*, enables to get the result ignored the circuit structure:

$$F = (1011110100\ 00) = \{F_1, F_3, F_4, F_5, F_6, F_8\}.$$

The synthesis of disjunctive form by FDT M^*, masked obtained faults $F = \{F_1, F_3, F_4, F_5, F_6, F_8\}$, gives solution:

$$F = (F_1 \vee F_4 \vee F_5 \vee F_6)(F_3 \vee F_5 \vee F_8)(F_1 \vee F_3 \vee F_4 \vee F_8) =$$
$$= (F_1 \vee F_4 \vee F_5 \vee F_6)(F_1F_3 \vee F_1F_5 \vee F_1F_8 \vee F_3F_3 \vee F_3F_5 \vee F_3F_8 \vee$$
$$\vee F_4F_3 \vee F_4F_5 \vee F_4F_8 \vee F_3F_8 \vee F_5F_8 \vee F_8F_8) =$$
$$= F_1F_1F_3 \vee F_1F_1F_5 \vee F_1F_1F_8 \vee F_1F_3F_3 \vee F_1F_3F_5 \vee F_1F_3F_8 \vee$$
$$\vee F_1F_4F_3 \vee F_1F_4F_5 \vee F_1F_4F_8 \vee F_1F_3F_8 \vee F_1F_5F_8 \vee F_1F_8F_8 \vee$$
$$\vee F_1F_3F_4 \vee F_1F_4F_5 \vee F_1F_4F_8 \vee F_3F_3F_4 \vee F_3F_4F_5 \vee F_3F_4F_8 \vee$$
$$\vee F_3F_4F_4 \vee F_4F_4F_5 \vee F_4F_4F_8 \vee F_3F_4F_8 \vee F_4F_5F_8 \vee F_4F_8F_8 \vee$$
$$\vee F_1F_3F_5 \vee F_1F_5F_5 \vee F_1F_5F_8 \vee F_3F_3F_5 \vee F_3F_5F_5 \vee F_3F_5F_8 \vee$$
$$\vee F_3F_4F_5 \vee F_4F_5F_5 \vee F_4F_5F_8 \vee F_3F_5F_8 \vee F_5F_5F_8 \vee F_5F_8F_8 \vee$$
$$\vee F_1F_3F_6 \vee F_1F_5F_6 \vee F_1F_6F_8 \vee F_3F_3F_6 \vee F_3F_5F_6 \vee F_3F_6F_8 \vee$$
$$\vee F_3F_4F_6 \vee F_4F_5F_6 \vee F_4F_6F_8 \vee F_3F_6F_8 \vee F_5F_6F_8 \vee F_6F_8F_8 =$$
$$= F_1F_3 \vee F_1F_5 \vee F_1F_8 \vee F_3F_4 \vee F_3F_5 \vee F_3F_6 \vee F_4F_5 \vee F_4F_8 \vee F_5F_8 \vee F_6F_8.$$

In a case of additional use the circuit structure (Fig. 1) in the form of rows Y_{10}, Y_{11}, Y_{12} of the table M^* that is put on FDT the result can not be worse. Computation of the vector $M^1(\vec{Y})$ in M^* is realized by application the mask of the reachability vectors $\{\vec{Y}_{10}, \vec{Y}_{11}, \vec{Y}_{12}\}$, which correspond to the faulty circuit outputs on test patterns:

$$M^1(\vec{Y}) = [\vec{Y}_{10} \wedge M_1(Y_{10})] \vee [(\vec{Y}_{11}) \wedge M_2(Y_{11})] \vee$$
$$\vee [(\vec{Y}_{12}) \wedge M_5(Y_{12})].$$

Replacement of the specified vectors of the fault detection table to the expression to obtain F results in:

$$M^1(\vec{Y}) = [1100000001\ 00] \vee [0110000100\ 10] \vee$$
$$\vee [0011001010\ 01] = [1111001111\ 11] =$$
$$= \{F_1, F_2, F_3, F_4, F_7, F_8, F_9, F_{10}, F_{12}\}.$$

Subsequent calculations, related to vector operations $F(\vec{Y}) = M^1(\vec{Y}) \wedge \overline{M}^0$ at FDT, form the final solution:

$$F(\vec{Y}) = (1111001111\ \ 11) \wedge (1011110100\ \ 00) =$$
$$= (1011000100\ \ 00) = \{F_1, F_3, F_4, F_8\}.$$

Last vector (111100111111) makes a mask to form disjunctive normal form that has the following terms:

$$F(\vec{Y}) = (F_1 \vee F_4)(F_3 \vee F_8)(F_1 \vee F_3 \vee F_4 \vee F_8) =$$
$$= (F_1 \vee F_4)(F_3 \vee F_8) = F_1F_3 \vee F_1F_8 \vee F_3F_4 \vee F_4F_8.$$

In general case taking into account the circuit structure in the form of the reachability matrix enables to get more exact diagnosis due to removal the faults, which can not influence on faulty outputs.

The proposed vector-logical diagnosis method gives the mathematical apparatus to a developer of SoC, by which the diagnosis of faulty components can be realized on conditions that there is preformed fault detection table. At that set-theory solutions can be represented by all possible fault combinations in the form of DNF terms. The method is effective if a number of “1” in FDT greater then 10-20%. Availability of additional information in the form of reachability matrix for all external outputs enables to reduce essentially (by 40-60%) the power of faults under test or term quantity, which determine all possible fault combinations, forming the output response vector.

3. Software implementation of the fault detection method

The software «Defect Analyzer» is intended for simulation of digital systems-on-chip testing and diagnosis by using the fault detection table. «Defect Analyzer» is application that is based on operating system Windows XP; it is developed by C++ language and programming environment Borland C++ Builder 2006, and includes 659 statements.

The algebra-logical diagnosis method for circuit structure, consecutive and parallel methods of test point choice, where the interactive probing is carried out, are realized in the application. As input data the covering table is used; it is made in the process of circuit testing. The table represents input signal levels, as well as detect faults in a circuit on current test pattern; value of the vector V indicates that (Fig. 2).

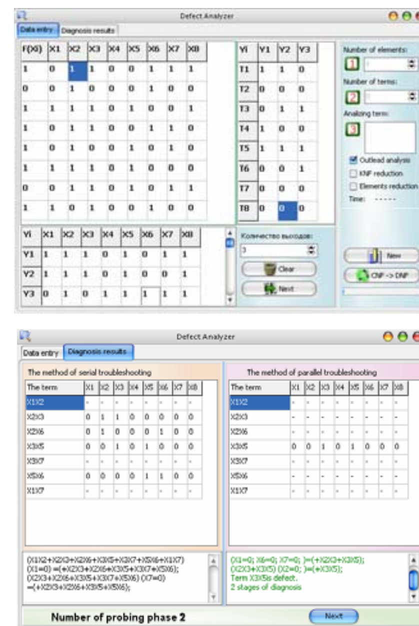

Fig. 2. Interfaces of the diagnosis system

Data level, which can be processed by the application, is limited by quantity of terms of no simplified DNF. A number of table rows (terms) should not be greater then 32766. A number of DNF terms depend on initial data and it can be calculated by formula:

$$N = \prod_{\forall i(V_i=1)}^{i=\overline{1,n}} (N_i) ,$$

where Ni is quantity of elements "1" in a test pattern.

At diagnosis the input patterns for which value of the vector V is equal to 1 is considered.

The main time of diagnosis is consumed on transformation CNF to DNF and its reduction. The computational complexity of transformations depends on experiment results and circuit (FDT) size:

$$Q = \prod_{i=1}^{n} (N_i!) + \frac{n!}{2(n-2)!} nm ,$$

where n is a number of test patterns; m is quantity of elements, which are used in an experiment; Ni is a number of "1" elements in i-th input pattern.

4. Conclusion

The vector-logical method of digital systems-on-chip diagnosis is proposed; it uses preliminarily made fault detection table. Set-theory solutions are represented by all possible fault combinations in the form of DNF terms. The method operates effectively when numbers of "1" in the fault detection table greater then 10-20%. Availability of additional information in the form of reachability matrix for all external outputs enables to reduce essentially (by 40-60%) the power of precautionary faults or numbers of terms, specified all possible fault combinations, which forms the output response vector.

Practical importance of the method is high efficiency, based on processing the fault detection table, masked by the output response vector. Additional use of circuit structure enables to raise essentially the diagnosis resolution due to removal of faults, which don't influence on forming of incorrect output responses. Solution representation in the form of DNF enables to evaluate a complete combination set, as well as to choose minimal of them, in which a fault exists undoubtedly.

Charge for the method advantages is necessity of the fault detection table making, which will have inadmissible size for circuits, including more then million gates. In this case it is necessary to introduce the hierarchy for model extension, bur with reduction of diagnosis resolution.

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