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7th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)

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The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
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CONTENTS

System in Package. Diagnosis and Embedded Repair

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Abstract

Problems of System in Package (SiP), as new constructive generation, modules testing are considered. The method of digital system diagnosis based on the disjunctive normal form, which is represented by fault coverage matrix of test sequences are proposed. The method is focused on embedded service functionality, presented as F –IP modules. Methods for embedded functionality repair are adapted.

1. Problems of embedded SiP components testing

New Technology System in Package actively gaining market of microelectronics. This technology provides a more complete functional and small board size. Such system in the package contains 2 or more crystals, which are combined with passive components, filters and other components.

As a rule, highly derived product used in a specific device for solving pre-defined tasks. Using SiP has significant advantages over other technologies, such as: increasing the productivity of digital systems, miniaturization of the volume, product weight reducing, reducing delay of signals propagation, power and cost of confirmed device.

But, like any other technology, the development of SiP has negative characteristics, among which are: the hardware complexity of digital systems in a package, which has had billions of valves and hundreds of millions of transistors on a single crystal, the high cost of design, low output suitable products SiP , the technological complexity of recovery, the limited market-design problem of heat from hot components are added to the problem and the developers of devices, such as: testing of wafers, substrates, functional modules. problems of silicon crystals joining in the digital electronic system, mechanical protection of internally silicon crystals, assembly, heat dissipation have not been decided (Fig.1).

By the above-mentioned problems of testing, test of logic should be added.

The memory diagnosis and repair problem is related to the tendency to continuous reduction of chip area, which is allocated to original and standardize logic, and simultaneous growth of embedded memory. Figure shows increasing of the memory specific weight on a chip, which will reach 94% by 2014 year. It will provide not only fast response of carrying out of functions, but also flexibility that is appropriate to software in relation to design error correction [1].

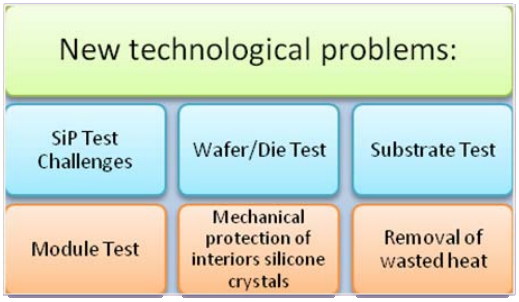

Figure1. The main problem of SiP technology using

To ensure quality and reliability of infrastructure, it is necessary to create service modules I-IP, which includes the technology of testing, diagnosis, and SiP modules recovery in real time.

The research purpose: improvement of digital system quality through the methods development of service for integrated diagnostics and repair IP-modules functionality based on surplus land.

Tasks to solve are: Adaptation of algebra-logical method for embedded diagnosis, based on coverage matrix using; adaptation of vector-logical method for memory repair; working out of digital crystal logic blocks matrix model in the form of functional cells, containing malfunctions; working out of a method for faulty logic blocks of digital system covering by repair cells using matrix rows and columns detour; the practical results of research.

2. Algebra-logical method of defects diagnosis

The structure of service I-IP modules for defects diagnosing in the functional blocks F-IP is presented in figure 2.

The general role is assigned to the boundary scan technology that is implemented into a chip now has to simplify solution of practically all problems of SoC and SiP Functional Intellectual Property Infrastructure [2].

The access controller to internal lines and boundary scan register ports uses a cell or the register stage. In aggregate the number of such cells providing in this case monitoring, should be equal to quantity of observable lines problem of the project which are necessary for an exact diagnosis.

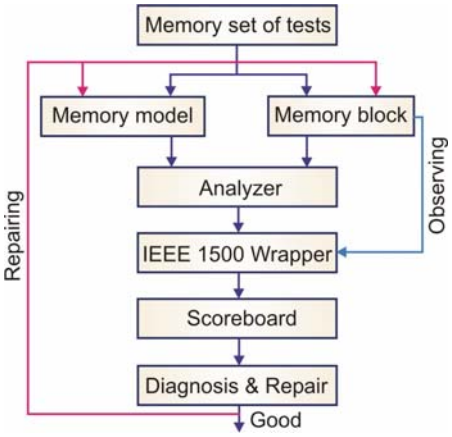

Figure 2. Model of F-IP diagnosing process

IEEE 1500 Wrapper is a multiprobe intended for an establishment of the exact diagnosis. Scoreboard analysis results of diagnosis for subsequent SoC and SiP components repair.

The Analyser module analyzes output reactions of model (Memory Model) and the real device (Memory Block) to the input test vectors arriving from the tests generator. Discrepancy of reactions forms individual co-ordinates of a vector experimental check $V(T) = (V_1, V_2, ,..., V_i, ,..., V_n)$ for each input pattern (VEC). IEEE 1500 Wrapper is a multiprobe intended for an establishment of the exact diagnosis. Scoreboard analysis results of diagnosis for subsequent SoC and SiP components repair.

Coordinate value of the vector V is result of XOR operation execution at generalized model and real output responses.

Solution of the diagnosis problem can be obtained by means of the Boolean algebra and the fault detection table (FDT) M that is the Cartesian product of test T on a set of given faults A in the aggregate with the vector of experimental check, where solving of the covering problem gives maximal exact result in the form of BTA and every term is possible variant of faults existence in a device.

The diagnosis model is represented by the components:

$$A =< T, F, M, V >,$$

$$T = (T_1, T_2, ..., T_i, ..., T_n);\ F = (F_1, F_2, ..., F_j, ..., F_m);$$

$$M = \left|M_{ij}\right|, i = \overline{1,n};\ j = \overline{1,m};\ V = (V_1, V_2, ..., V_i, ..., V_n);$$

$$V_i = R(T_i) \oplus R^*(T_i);\ \{V_i, T_i, M_{ij}, F_j\} \in \{0,1\}.$$

The diagnosing problem decision is reduced to the analysis of the fault table, received as a result of faults modeling, by the subsequent logic product of disjunctions (COF) recording:

$$F = \bigwedge_{\forall V_i=1}^{i=\overline{1,n}} \left(\bigvee_{\forall M_{ij}=1}^{j=\overline{1,m}} F_j \right).$$

The conjunctive normal form (CNF), received of FT, is transformed to a disjunctive normal form (DNF) by means of equivalent transformations (logic multiplication, minimization and absorption)[3]:

$$F = \bigwedge_{\forall V_i=1}^{i=\overline{1,n}} \left(\bigvee_{\forall M_{ij}=1}^{j=\overline{1,m}} F_j \right) = \left| \begin{bmatrix} a \vee ab = b \\ a \vee a = a \end{bmatrix} \right| = \bigvee_{i=1}^{2^m} \left(\bigwedge_{j=1}^{m} k_j F_j \right), k_j = \{0,1\}.$$

The last feature forms the diagnosis of some defects combination subset that need to be clarified further through the use of additional sensing points of the Interior through the boundary scan register.

It also has been adapted vector-logical method for the F-IP diagnosis, the advantage of which is the technological analysis of FT.

Computational complexity of this method is multiplicative dependence on the number of defects and test capacity: $Q = n \times m$. The method should be used with FT, which contain a lot of coordinates with value «1», when algebra-logical method has high Quine estimation value.

3. Example of diagnosis algebra-logical method

Algebra-logical method can be formally considered by an example of the following fault detection table M_1 and it can be represented by five algorithm items:

$M_1 =$

T_i / F_j	F_1	F_2	F_3	F_4	F_5	F_6	V
T_1	1			1			1
T_2		1			1		1
T_3			1	1		1	1
T_4	1		1				1
T_5		1			1	1	0

1. Detection of all rows, which correspond to zero of the experimental validation vector for nulling of all 1-coordinates of found rows. In this case it is the row T_5.

2. Detection of all columns, which have zero values of rows, coordinates with zero state of the vector V. Nulling of unit values of found columns. In this case it is: F_2, F_5, F_6.

3. Removal the rows and the columns, which have only zero coordinate values (found in items 1 and 2), from the fault detection table.

$M_1 =$

T_i / F_j	F_1	F_2	F_3	F_4	F_5	F_6	V
T_1	1			1			1
T_2		0			0		1
T_3			1	1		0	1
T_4	1		1				1
T_5		0			0	0	0

$=$

T_i / F_j	F_1	F_3	F_4	V
T_1	1		1	1
T_3		1	1	1
T_4	1	1		1

4. Making CNF by unit values of VEC:

$$F = (F_1 \vee F_4) \wedge (F_3 \vee F_4) \wedge (F_1 \vee F_3) =$$

$$= (F_1F_3 \vee F_3F_4 \vee F_1F_4 \vee F_4F_4) \wedge (F_1 \vee F_3) =$$

$$= F_1F_1F_3 \vee F_1F_3F_4 \vee F_1F_1F_4 \vee F_1F_4F_4 \vee F_1F_3F_3 \vee$$

$$\vee F_3F_3F_4 \vee F_1F_3F_4 \vee F_3F_4F_4 = F_1F_3 \vee F_1F_3F_4 \vee$$

$$\vee F_1F_4 \vee F_3F_4 \vee F_1F_3F_4 \vee F_3F_4 = F_1F_3 \vee F_1F_4 \vee F_3F_4.$$

5. Transformation CNF to DNF with subsequent minimization of the function. It brings to gaining of sought-for result in the fault combination form:

$$F = F_1F_3 \vee F_1F_4 \vee F_3F_4.$$

4. Software implementation of the fault detection method

The software «Defect Analyzer» is intended for simulation of digital systems testing and diagnosis by using the fault detection table.

The algebra-logical diagnosis method for circuit structure, consecutive and parallel methods of test point choice, where the interactive probing is carried out, are realized in the application. As input data the covering table is used; it is made in the progress of circuit testing (fig. 3).

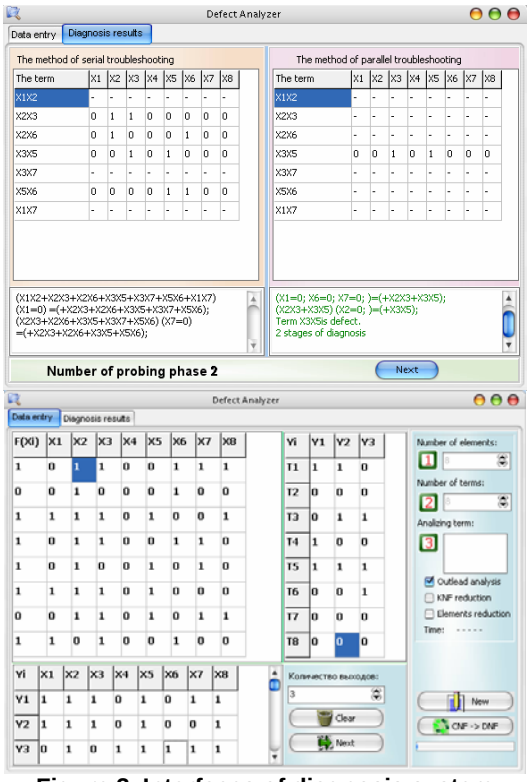

Figure 3. Interfaces of diagnosis system

To simplify the original table cover, the program can use the information on the zero elements of the test sets and the signal values at the circuit structure outputs for each test set, as well as pre preliminary CNF simplification.

After performance of necessary transformations the program gives out following data: status of the faults table at each stage of sounding in control points; value of the defects combination at each stage of sounding in control points; quantity of necessary stages of sounding for result reception at use of consecutive and parallel choice of control points.

The volume of data which are processed by the program is limited by quantity of terms of no simplified DNF.

$$N = \prod_{\forall i(V_i=1)}^{i=\overline{1,n}} (N_i),$$

where Ni – quantity of elements «1» in test pattern.

The basic time expenses of the program fall to transformation of CNF to DNF and its simplification. Computing complexity of transformations depends on data of experiment and is calculated under the formula:

$$k = \prod_{i=1}^{n}((N_i!)) + \frac{n!}{2(n-2)!}nm,$$

N - maximum quantity of PDNF;

Q - computing complexity of transformation of CNF to DNF and its simplifications;

n - quantity of test sets;

m - quantity of the elements participating in experiment;

Ni - quantity of individual elements in the test set number *i*.

5. Method of logic blocks matrix detour for defective FPGA components covering by repair cells

Topology of crystal is represented by a matrix of cells $M = |M_{ij}| i = \overline{1,p};\ j = \overline{1,q}$, scaled on horizontal and vertical integers figures $(p \times q)$ [4-6]. Each cell M_{ij} has n^2 logic blocks. The matrix has any number of defects equal k; in each cell can be no more than n^2 logic blocks.

Example of a matrix of cells with defects are presented in Fig. 4, where the dimension of the cell n is 3, and the dimension of the matrix at the scale of the number of cells in rows and columns is equal to 5.

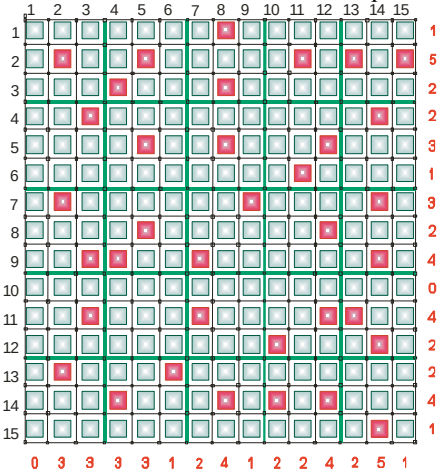

Figure 4. The matrix of blocks in the FPGA-scale cell

The method of circumventing a matrix of logical blocks for FPGA components repair, leading to quasioptimal cover all the defective blocks by minimal number of repair cells, represented by the following paragraphs:

1. Definition of all defective blocks co-ordinates of matrix M that define crystal topology;

2. Construction of binary matrixes, that cover defective blocks by detour of cells on rows and columns:

$$M_r = \left|M_{ij}^r\right|, i = \overline{1, p/n}; j = \overline{1, q};$$

$$M_c = \left|M_{ij}^c\right|, i = \overline{1, p}; j = \overline{1, q/n}.$$

Here, every n coordinate rows (columns) are replaced by one with the value in it, determined $f^r(f^c)$ by OR function from n coordinates.

$$M_{ij}^c = f^r(f^c) = \begin{cases} 0 \leftarrow (000); \\ 1 \leftarrow (1XX) \vee (X1X) \vee (XX1), X = \{0,1\}. \end{cases}$$

For example:

$$M = \left|M_{ij}\right| = \begin{bmatrix} 0&0&0&0&1&1 \\ 0&0&0&0&0&1 \\ 0&1&1&0&1&0 \\ 1&0&0&0&0&1 \\ 0&0&0&0&1&0 \\ 0&1&0&1&0&1 \end{bmatrix} \xrightarrow{f^r} M_r = \left|M_{ij}^r\right| = \begin{bmatrix} 0&1&1&0&1&1 \\ 1&1&0&1&1&1 \end{bmatrix}$$

Here each column is compressed in the two coordinates on the rules of logical operator Or, since the cell parameter n, hereafter, is 3. Similarly, the procedure for obtaining a matrix of columns gives the result of bypass:

$$\left|M_{ij}\right| = \begin{bmatrix} 0&0&0&0&1&1 \\ 0&0&0&0&0&1 \\ 0&1&1&0&1&0 \\ 1&0&0&0&0&1 \\ 0&0&0&0&1&0 \\ 0&1&0&1&0&1 \end{bmatrix} \xrightarrow{f^c} \left|M_{ij}^c\right| = \begin{bmatrix} 0&1 \\ 0&1 \\ 1&1 \\ 1&1 \\ 0&1 \\ 1&1 \end{bmatrix}$$

3. Criteria definition of defective blocks covering quality;

4. Detour of matrix cells on rows (columns);

5. Definition of covering quality of the received decision variant:

$$Q_{cr} = \frac{1}{N}\sum_{i=1}^{n} F_i$$

6. Covering of defective blocks by reserve cells;

6. Strategies for criteria calculating

Method 1. Quality cover defective units are calculated by using the binary matrix based on counting the number of single coordinates given by the actual skeleton unit matrix. Criterion progressive coverage of defective blocks presented the following expression:

$$Q_r = \sum_{i=1}^{p/n}\left[\frac{1}{H_i^r - L_i^r + 1}\sum_{j=1}^{q} M_{ij}^r\right]$$

$H_i^r(L_i^r)$ - maximum (minimum) index of row j, behind which there are no co-ordinates with value "1".

$H_i^r - L_i^r + 1$ - range of variation in the row of the matrix M, which gives the sum of individual coordinates of the row.

Further, given the assessment of all lines are added as a criterion for the effectiveness of line-by-line defective blocks coverage.

Similarly, the criterion is computed by column:

$$Q_c = \sum_{j=1}^{q/n}\left[\frac{1}{H_j^c - L_j^c + 1}\sum_{i=1}^{p} M_{ij}^c\right]$$

Step 1. The counter of zero co-ordinates and the counter of repair cells number nulling: j=0, Q=0.

Step2. Consecutive scanning of vector $j = j+1 \leftarrow M_{ij}^r = 0$ cells to first cell with «1» value $M_{ij}^r = 1 \rightarrow (Q = Q+1, j = j+n-1)$. It is necessary to increase number of repair cells Q on 1;

Step3. If the condition $j \geq q$ is true - end of row processing, otherwise – transition to step 2.

The described procedure is applied to all rows of the modified matrix $\left|M_{ij}^r\right|$ ($\left|M_{ij}^c\right|$) and as a result counter Q contains the minimum number of repair cells to cover all defective blocks.

Similarly, the strategy is executed bypass cell matrix by column.

Method 2. The following method of criteria calculation allows defining more precisely a detour direction of the modified matrix by reserve cells with the minimum expenses. The proposed method has a higher value of computational complexity as compared to the previous one.

The proposed method is based on the idea that the interval between the next cells of the modified matrix longer, the more repair cells must be used to cover all faults.

Step 1. The counter of zero co-ordinates, the counter of repair cells number nulling: j=0, Q=0, parameter K=0 and criteria value for the current column.

Step 2. Consecutive scanning of vector $j = j+1 \leftarrow M_{ij}^r = 0$ cells to first cell with «1» value $M_{ij}^r = 1 \rightarrow (Q = Q+1, j = j+n-1)$.

Step 3. Consecutive detour of cells on a column (row). If expression $M_{ij}^c = 0$ is true – K=K+1, otherwise Q=Q+K.

Step 4. If the condition $j \geq q$ is true - end of row processing, otherwise – transition to step 3.

The described procedure is applied to all rows of the modified matrix $\left|M_{ij}^r\right|$ ($\left|M_{ij}^c\right|$). Similarly, the strategy is executed detour cell matrix by columns.

The decision which is characterized by the least value of criterion is preferable.

The described procedure is applied to all rows of the modified matrix and as a result counter Q contains the minimum number of repair cells to cover all defective blocks. Similarly, the strategy is executed bypass cell matrix by columns.

7. Software implementation for FPGA components repair

Software «aGalls» destination is modeling for FPGA functionality repair using method of logic blocks matrix detour for defective components covering by repair cells

As initial data in the program are: the primary matrix, which define position of defective FPGA components; dimension of one covering cell; quantity of horizontal cells dimension n^2; quantity of vertical cells dimension n^2 (Fig. 5);

Also, you can fill in a matrix of random values, which may be useful to determine the effectiveness of the use of quality criteria covering a large number of tests.

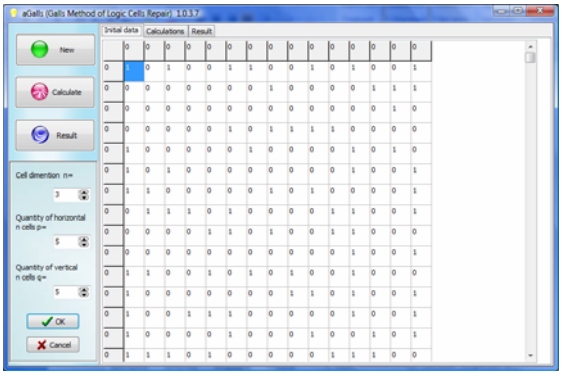

Figure 5. Program interface

The next phase of software allows to build modified matrix to detour the rows and columns, calculates the values of quality criteria cover both the proposed methods, and on the basis of the data suggests the direction of matrix detour for each method (Fig. 6).

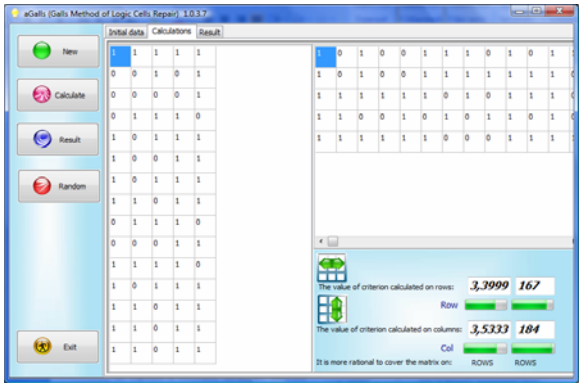

Figure 6. Quality criteria covering calculation

In the third stage software displays the contents of the modified matrix after logic blocks detour on rows and columns. Then it calculates real necessary quantity of repair cells for detour in both directions.

It allows to look at possible variants of problem decision for working capacity FPGA restoration by logic blocks detour and estimate the quality criteria.

Criteria reliability of covering has been estimated after carrying out of 200 experiments with a matrix by dimension 24x24; cells 3x3. The number of defective cells was accidental. When using the criteria based on the calculation of the length of vector with «1», the best solution was identified in 69% of experiments, as in case calculation of quality criteria based on the assessment cover the distance between next cells - in 75% of cases.

8. Conclusion

Suggested methods of diagnosis: algebra-logical and vector-logical offers in the design and testing of digital systems in the crystals mathematical apparatus, which is capable to carry out the diagnosis of defective components, if there exist a pre-built faults table.

The method of logic blocks matrix detour is intended for restoration of components FPGA working capacity by decision reception in a kind quasi-optimal covering of all defective blocks by the minimum number of repair cells. Choice one of two strategies for rows and columns detour of logic blocks matrix on the basis of structurization criteria is offered.

Scientific novelty. A new matrix method for the diagnosis of defects in digital system, which is characterized by normal disjunctive form анв faults table, which makes it possible to obtain a complete and minimal combinations of multiple faults.

Practical significance - attractiveness of the proposed method for the market of electronic technology, which allows to determine the minimum number of repair cells for recovery of digital products, incorporated in the crystal of SoC / SiP.

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