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CONTENTS

SUM IP Core Generator – Means for Verification of Models-Formulas for Series Summation in RKHS

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Abstract

Program system SUM IP Core Generator – means for verification of models – formulas of series summation in Reproducing Kernel Hilbert Space (RKHS) which allows to carry out input of the description of the model-formula with the help of the GUI-interface is offered; to model models – formulas with the help of software products Mathematica, Sinplify, Modelsim, Riviera, Active HDL; to generate initial files IP-core in languages of the description of equipment VHDL, Verilog, System C; to generate scripts – files for modelling, synthesis, implementation, time modelling; to synthesize tests, parameters, conditions for verification on basis Testbench; to carry out post-synthesis modelling for revealing mistakes in codes.

1. Introduction

The program system SUM IP Core Generator is proposed. Its structure is represented on Fig. 1.

The Purpose of this system is essential reduction of time for data preparation by use of the user-friendly GUI-interface with a view of the subsequent modelling for definition of adequacy and accuracy of models-formulas, and also automatic generation of the HDL-code considered in quality IP Core.

Solved problems (see fig. 1):

1. Input of the description of the model-formula with the help of the GUI-interface.
2. Modelling models-formulas with the help of software products Mathematica, Sinplify, Modelsim, Riviera, Active HDL [2,3,8].
3. Generation of initial files IP-core in languages of the description of equipment VHDL, Verilog, System C [1,5,7].
4. Generation of scripts-files for modelling, synthesis, implementation, time modelling [4,6,8].
5. Synthesis of tests, parameters, conditions for verification on the basis of generating Testbench [1,7].
6. Post-synthesis modelling for revealing mistakes in codes [3,8].

2. SUM IP Core Generator

SUM IP Core Generator represents software of automated generation IP Core. The system allows to generate the complex, tested, verified and optimized functional modules (IP Core), described on languages Mathematica, VHDL, Verilog, SystemC [2,8] which can be used repeatedly at designing various devices for reduction of time of its development. SUM IP Core Generator realizes universal models-formulas for summation of series and it can be used for generation IP Core, realizing the following functions: a sine, co-sine, Bessel, harmonious, analytical [4].

The actuality of creation such IP Core is defined by growth of manufacturing techniques of chips that gives modern developers of more and more opportunities at designing complex digital and radio-electronic devices. Use IP Core allows: it is essential to reduce time of an output of an end-product for the market; to minimize risk of designing, due to inclusion of already organized IP-modules; to reduce time of verification of all system as a whole; to predict functionality and productivity of the created project. Thus, application SUM IP Core Generator is focused on essential reduction (15-20 %) time and financial expenses at verification and modelling of formulas of models.

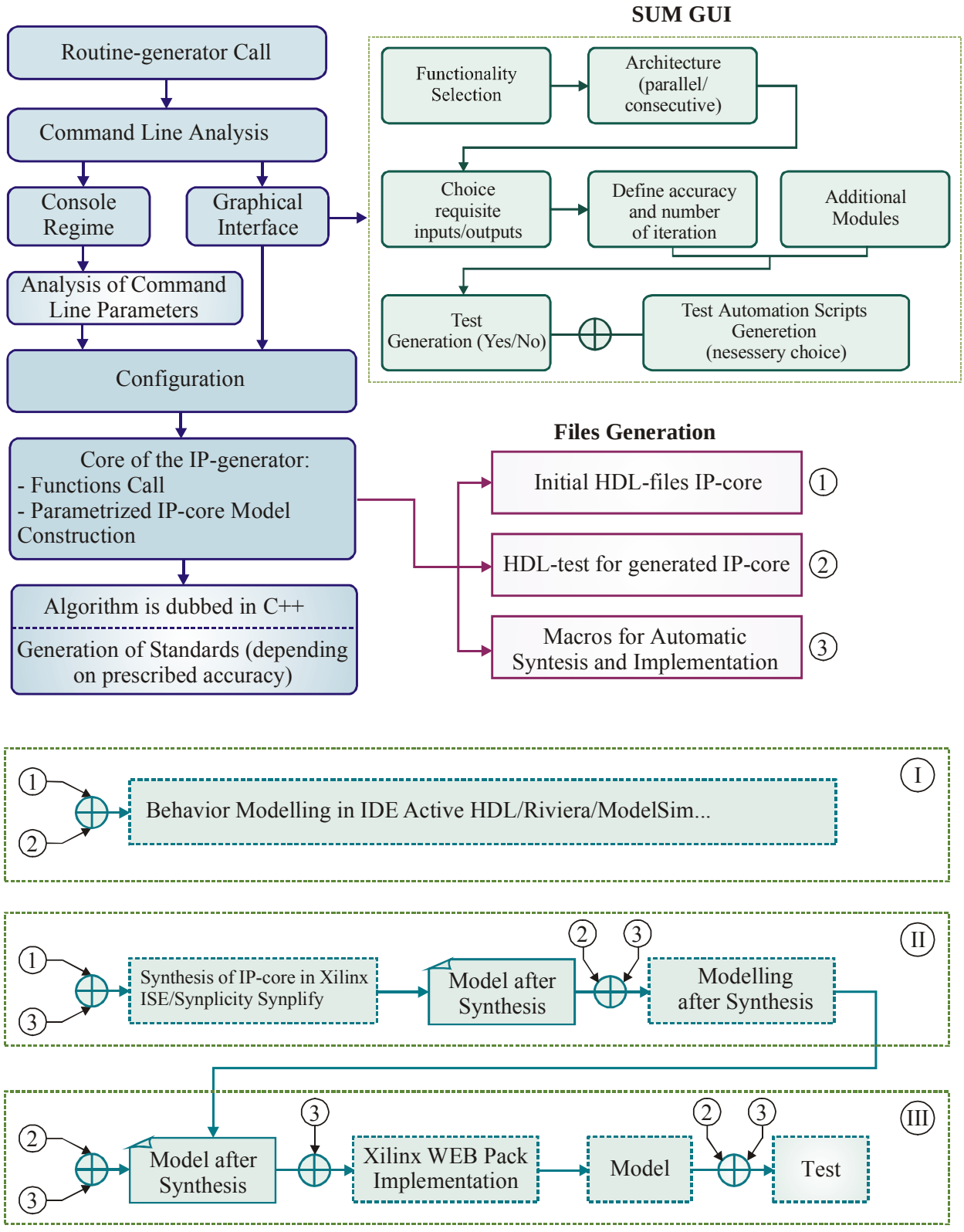

Figure 1. Testing and verification system for models-formulas

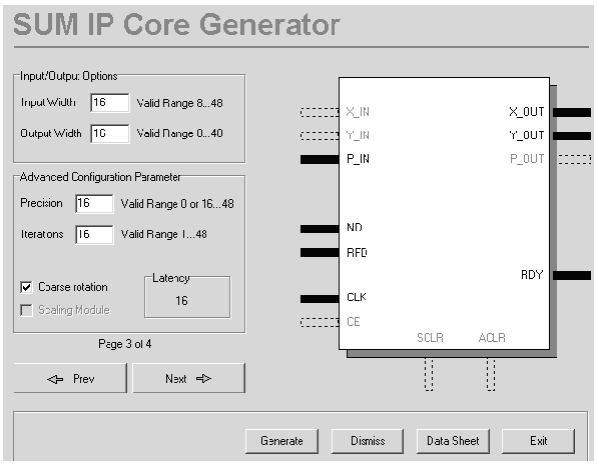

Figure 2. User interface for parameter assignment

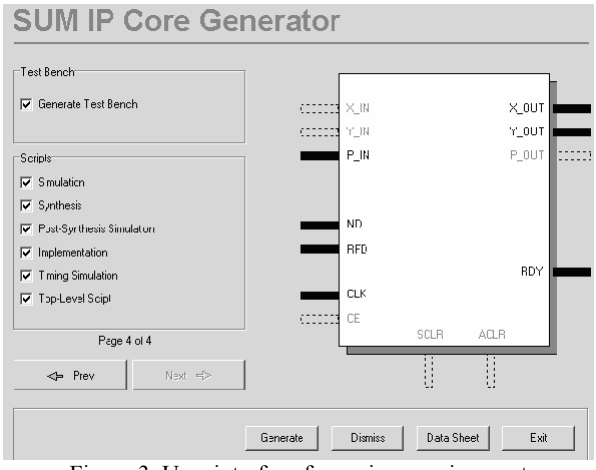

Figure 3. User interface for regimes assignment of verification

SUM IP Core Generator allows to generate automatically Test Bench for the chosen architectural and functional configuration. All modes of verification and testing of models-formulas are submitted on fig. 3. Examples of application of the formula of calculation of triple series are resulted in the table. Time of construction for surfaces at calculation by the direct and truncated formulas decreases for 4 order.

The basic idea having the practical importance, consists in the following: 1) the interesting formulas decisions having a market demand, should be made out on standard languages of programming, such as VHDL, Verilog; 2) the standard products focused on the analysis of mathematical models communicate through languages of the description of the equipment with simulators of known firms of the world. In this case the question is product Riviera of 2005.08 (firms Aldec) which has a wide spectrum own functionalities, but can work also in pair with Mathematica through connection with Simulink. Thus, with a view of input, verification and the analysis of complex mathematical models it is used GUI as the convenient interface for generation of HDL-codes of complex mathematical models which further will be claimed in the market of electronic technologies in quality IP Cores.

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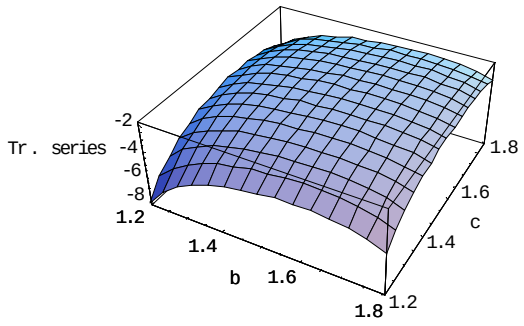
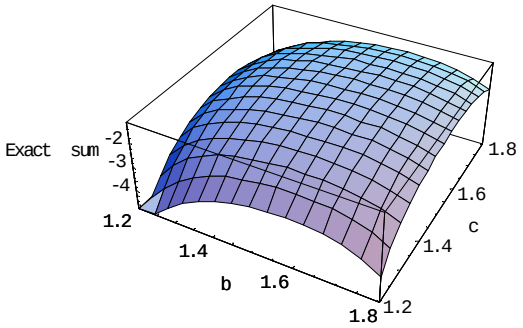
3. Conclusion

For verification of scientific results as models-formulas of the exact sums of series program system SUM IP Core Generator which allows to carry out input of the description of the model-formula with the help of the GUI-interface is developed; to modelling models-formulas with the help of software products Mathematica, Sinplify, Modelsim, Riviera, Active HDL; to generate initial files IP-core in languages VHDL, Verilog, System C; to generate scripts-files for modelling, synthesis, implementation, time modelling; to synthesize tests, parameters, conditions for verification on basis Testbench; to carry out post-synthesis modelling for revealing mistakes in codes.

Practical result of application SUM IP Core Generator is essential, on 20-30 %, downturn time both material inputs on testing and verification of the models-formulas focused on its implementation in crystals by use IP Core, received with the help of offered software product.

The visual system of automatic generation SUM IP Core Generator has the simple user interface and the detailed documentation. It is intended for automation design verification works of hardware-engineers. Methods of exact series summation are actual in the market of radio electronics and there is a necessity for system, which gives convenient and optimum realization of models -formulas, and also ways of their verification and testing.

$$\sum_{k=0}^{\infty}\frac{\varepsilon_k(-1)^k}{a^2-k^2}\sum_{m=0}^{\infty}\frac{\varepsilon_m(-1)^m}{b^2-m^2}\sum_{n=0}^{\infty}\frac{\varepsilon_n(-1)^n}{c^2-n^2}J_k(x)J_m(x)J_n(x)=\frac{\pi^3 J_a(x)J_b(x)J_c(x)}{abc\sin\pi a\sin\pi b\sin\pi c}$$

Formulas	$\sum_{k=0}^{\infty}\frac{\varepsilon_k(-1)^k}{1{,}5^2-k^2}\sum_{m=0}^{\infty}\frac{\varepsilon_m(-1)^m}{b^2-m^2}\sum_{n=0}^{\infty}\frac{\varepsilon_n(-1)^n}{c^2-n^2}J_k(2{,}5)J_m(2{,}5)J_n(2{,}5)$, $1{,}2<b<1{,}8,\ 1{,}2<c<1{,}8$	$\frac{\pi^3 J_{1,5}(2{,}5)J_b(2{,}5)J_c(2{,}5)}{1{,}5bc\sin 1{,}5\pi\sin\pi b\sin\pi c}$
Graphs		
Timing	{748. Second, - SurfaceGraphics -}	{0.031 Second, - SurfaceGraphics -}

Error (Abs)

2.15873	1.60142	1.32214	1.16819	1.0959	1.10488	1.25254
1.60142	1.18132	0.972774	0.859237	0.807497	0.817373	0.932855
1.32214	0.972774	0.800076	0.706594	0.664594	0.67397	0.771572
1.16819	0.859237	0.706594	0.624024	0.586989	0.595401	0.681874
1.0959	0.807497	0.664594	0.586989	0.551841	0.559042	0.638888
1.10488	0.817373	0.67397	0.595401	0.559042	0.564729	0.64232
1.25254	0.932855	0.771572	0.681874	0.638888	0.64232	0.724711

Error (Rel)

26.3601	28.1701	29.09	29.2025	28.5646	27.2202	25.2148
28.1701	29.9357	30.833	30.9427	30.3204	29.0091	27.053
29.09	30.833	31.7188	31.8271	31.2128	29.9182	27.9871
29.2025	30.9427	31.8271	31.9353	31.3219	30.0294	28.1014
28.5646	30.3204	31.2128	31.3219	30.7031	29.3989	27.4535
27.2202	29.0091	29.9182	30.0294	29.3989	28.0702	26.0882
25.2148	27.053	27.9871	28.1014	27.4535	26.0882	24.0516

The result of system work is IP Core, optimum, parameterized and ready for the further use in complex systems.

Parameters of realization: 1. OS: Windows XP, Windows 2000, Windows 98.2. The environment of development: Borland C ++ Builder. 3. Technology: VCL. 4. The size of a package of installation: ~ 3 Mb. 5. Speed of performance: ~1 sec. 6. Technology of development of software product: descending designing - from the general - to particular. 7. Testing: configurations are successfully generated, modeled Active HDL 6.1, synthesized Synplify Pro 7.1, Mathematica. 8. Requirements: 16 Mb RAM, 200 MHz CPU. 9. Number of lines of a code: 10000.10) Number of program modules: 15.

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