KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012)

Copyright © 2012 by the Institute of Electrical and Electronics Engineers, Inc.

Technically Co-Sponsored by

Kharkov, Ukraine, September 14 – 17, 2012

IEEE EAST-WEST DESIGN AND TEST SYMPOSIUM 2012 COMMITTEE

General Chairs
V. Hahanov – Ukraine
Y. Zorian – USA

General Vice-Chairs
R. Ubar - Estonia
P. Prinetto - Italy

Program Chairs
S. Shoukourian – Armenia
D. Speranskiy – Russia

Program Vice-Chairs
Z. Navabi – Iran
M. Renovell – France

Publicity Chair's
G. Markosyan - Armenia
S. Mosin - Russia

Public Relation Chair
V. Djigan - Russia

Program Committee
E. J. Aas - Norway
J. Abraham - USA
M. Adamski - Poland
A.E.Mohamed Mohamed - Egypt
A . Barkalov - Poland
R. Bazylevych - Ukraine
A. Chaterjee - USA
V. Djigan - Russia
A. Drozd - Ukraine
E. Evdokimov - Ukraine
E. Gramatova - Slovakia
A. Ivanov - Canada
M. Karavay - Russia
V. Kharchenko - Ukraine
K. Kuchukjan - Armenia
W. Kuzmicz - Poland
A. Matrosova - Russia
V. Melikyan - Armenia
L. Miklea - Romania
O. Novak - Czech Republic
Z. Peng - Sweden
A. Petrenko - Ukraine
J. Raik - Estonia
A. Romankevich - Ukraine
A. Ryjov - Russia
R. Seinauskas - Lithuania
S. Sharshunov - Russia
A. Singh - USA
J. Skobtsov - Ukraine
V. Tverdokhlebov - Russia
V. Vardanian - Armenia
V. Yarmolik - Byelorussia

Steering Committee
M. Bondarenko - Ukraine
V. Hahanov - Ukraine
R. Ubar - Estonia
Y. Zorian - USA

Organizing Committee
S. Chumachenko - Ukraine
E. Litvinova – Ukraine
V. Kharchenko – Ukraine

EWDTS 2012 CONTACT INFORMATION

Prof. Vladimir Hahanov
Design Automation Department
Kharkov National University of Radio Electronics,
14 Lenin ave,
Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26
E-mail: hahanov@kture.kharkov.ua
Web: www.ewdtest.com/conf/

10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

Kharkov, Ukraine, September 14-17, 2012

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Trades Committee of Kharkov National University of Radioelectronics and Trades Committee of Students, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University.

CONTENTS

An Efficient Fault Diagnosis and Localization Algorithm for Successive-Approximation Analog to Digital Converters
Melkumyan T., Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y. **15**

Application of Defect Injection Flow for Fault Validation in Memories
Amirkhanyan K., Davtyan A., Harutyunyan G., Melkumyan T., Shoukourian S., Vardanian V., Zorian Y. **19**

SSBDDs and Double Topology for Multiple Fault Reasoning
Raimund Ubar, Sergei Kostin, Jaan Raik **23**

Self Compensating Low Noise Low Power PLL design
Vazgen Melikyan, Armen Durgaryan, Ararat Khachatryan, Manukyan Hayk, Eduard Musaelyan **29**

Optimization Considerations in QCA Designs
Zahra NajafiHaghi, Marzieh Mohammadi, Behjat Forouzandeh, Zainalabedin Navabi **33**

Implementation of Address-Based Data Sorting on Different FPGA Platforms
Dmitri Mihhailov, Alexander Sudnitson, Valery Sklyarov, Iouliia Skliarova **38**

Comparison of Model-Based Error Localization Algorithms for C Designs
Urmas Repinski, Jaan Raik **42**

Synthesis of Clock Trees for Sampled-Data Analog IC Blocks
Bilgiday Yuce, Seyrani Korkmaz, Vahap Baris Esen, Fatih Temizkan, Cihan Tunc, Gokhan Guner, I. Faik Baskaya, Iskender Agi, Gunhan Dundar, H. Fatih Ugurdag **46**

Experiences on the road from EDA Developer to Designer to Educator
H. Fatih Ugurdag **50**

Multi-Beam Constant Modulus Adaptive Arrays in Real-Valued Arithmetic
Victor I. Djigan **54**

Simulation of Total Dose Influence on Analog-Digital SOI/SOS CMOS Circuits with EKV-RAD macromodel
Petrosyants K. O., Kharitonov I. A., Sambursky L. M., Bogatyrev V. N., Povarnitcyna Z. M., Drozdenko E. S. **60**

Models for Embedded Repairing Logic Blocks
Hahanov V.I., Litvinova E.I., Frolov A., Tiecoura Yves **66**

Real-time Interconnection Network for Single-Chip Many-Core Computers
Harald Richter **72**

Invariant-Oriented Verification of HDL-Based Safety Critical Systems
Kharchenko V., Konorev B., Sklyar V., Reva L. **76**

An Improved Scheme for Pre-computed Patterns in Core-based SoC Architecture
Elahe Sadredini, Qolamreza Rahimi, Paniz Foroutan, Mahmood Fathy, Zainalabedin Navabi **80**

Synthesis of Moore FSM with transformation of system in CPLD
Aleksander Barkalov, Larysa Titarenko, and Sławomir Chmielewski **85**

A WSN Approach to Unmanned Aerial Surveillance of Traffic Anomalies:
Some Challenges and Potential Solutions
David Afolabi, Ka Lok Man, Hai-Ning Liang, Eng Gee Lim, Zhun Shen, Chi-Un Lei,
Tomas Krilavičius, Yue Yang, Lixin Cheng, Vladimir Hahanov, and Igor Yemelyanov **91**

Synthesis of Qubit Models for Logic Circuits
Wajeb Gharibi, Zaychenko S.A., Dahiri Farid, Hahanova Yu.V., Guz O.A.,
Ngene Christopher Umerah, Adiele Stanley **95**

Theory of Optimal Nonlinear Filtering in Infocommunication's Problems
Victor V. Panteleev **102**

Verification of Specifications in the Language L with respect to Temporal
Properties Expressible by GR(1) Formulas
Anatoly Chebotarev **110**

Properties of code with summation for logical circuit test organization
Anton Blyudov, Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov **114**

Loop Nests Parallelization for Digital System Synthesis
Alexander Chemeris, Julia Gorunova, Dmiry Lazorenko **118**

Decreasing the Power Consumption of Content-Addressable Memory
in the Dataflow Parallel Computing System
Levchenko N.N., Okunev A.S., Yakhontov D.E., Zmejev D.N. **122**

WebALLTED: Interdisciplinary Simulator Based on Grid Services
Zgurovsky M., Petrenko A., Ladogubets V., Finogenov O., Bulakh B. **126**

Malfunctions Modeling of Converters and Homogeneous-chain Distributed Structure Devices
Artur Gulin, Zhanna Sukhinets **130**

On structure of quasi optimal algorithm of analogue circuit designing
Zemliak A., Michua A., Markina T. **134**

A Neuro-Fuzzy Edge Based Spectrum Sensing Processor for Cognitive Radios
Mohammadreza Baharani, Mohammad Aliasgari, Mohammadreza {Najafi, Jamali},
Hamid Noori **138**

Qubit Model for Solving the Coverage Problem
Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas,
Eshetie Abebech Mandefro **142**

PDF testability of the circuits derived by special covering ROBDDs with gates
Matrosova A., Nikolaeva E., Kudin D., Singh V. **146**

Compositional Microprogram Control Unit with Operational Automaton of Transitions
Alexander Barkalov, Roman Babakov, Larisa Titarenko **151**

Observability Calculation of State Variable Oriented to Robust PDFs and LOC or LOS Techniques
Matrosova A., Ostanin S., Melnikov A., Singh V. **155**

Low-Voltage Low-Power 2.5 GHz Linear Voltage Controlled Ring Oscillator
Hayk H Dingchyan **161**

High Speed IC Output Buffer with Reduced Power Consumption
Karine Movsisyan **165**

Engineering-Maintenance Methods of the Calculation Service Area Fixed BWA-paths
Sergey I. Myshlyakov, Victor V. Panteleev **170**

Analyses of two run march tests with address decimation for BIST procedure
Ireneusz Mrozek, Svetlana V. Yarmolik **176**

Design of Area Efficient Second Order Low Pass Analog Filter
Andranik Hovhannisyan **180**

Power Consumption Analysis of Content-Addressable Memories
Levchenko N.N., Okunev A.S., Yakhontov D.E. **183**

IC Physical Design Optimization Due to Effects of Device Physical Geometries
Avag Sargsyan **187**

System-on-Chip FPGA-Based GNSS Receiver
Alexander Fridman, Serguey Semenov **190**

Testware and Automatic Test Pattern Generation for Logic Circuits
Victor Zviagin **196**

Artificial Neural Network for Software Quality Evaluation Based on the Metric Analysis
Oksana Pomorova, Tetyana Hovorushchenko **200**

Self-Compensation of Influence of Parasitic Gate-Drain Capacitances of
CMOS Transistors in Analog Microcircuitry
Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov **204**

Hash-based Detection of OFDM Watermarking Symbol for Radiotelephone Identification
Aleksandr V. Shishkin, Aleksandr A. Lyashko **208**

A Novel Wideband Circular Ring DGS Antenna Design for Wireless Communications
Rakesh Sharma, Abhishek Kandwal, Sunil Kumar Khah **211**

Universal technique of the analysis of round-off noise in digital filters with
arbitrary structure described by topological matrixes
Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev **215**

Hardware Reduction for Compositional Microprogram Control Unit Dedicated for CPLD Systems
Barkalov A., Titarenko L., Smolinski L. **219**

Conservative Finite-difference Scheme for the Problem of Laser Pulse Propagation
in a Medium with Third-order Dispersion
Vyacheslav A. Trofimov, Anton D. Denisov **225**

A Four Bit Low Power 165MSPS Flash-SAR ADC for Sigma-Delta ADC Applications
Hasan Molaei, Khosrow Hajsadeghi **229**

Matrix Implementation of Moore FSM with Nonstandard Presentation of State Codes
Titarenko L., Hebda O. **233**

Alowpower1.2GS/s4-bitflashADCin0.18mCMOS
Mohammad Chahardori, Mohammad Sharifkhani, Sirous Sadughi **237**

Symmetrical Differential Stages on CMOS Transistors with Circuits ofSelf-Compensation and Cancellation
Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov **241**

Lower Bound of Error in AOA Based Passive Source Localization Using Single Moving Platform
Hejazi F., Norouzi Y., Nayebi M.M. **245**

A Design for Testability Technique for Quantum Reversible Circuits
Joyati Mondal, Debesh K. Das, Dipak K. Kole, Hafizur Rahaman **249**

A Flexible Design for Optimization of Hardware Architecture in Distributed Arithmetic based FIR Filters
Fazel Sharifi, Saba Amanollahi, Mohammad Amin Taherkhani, Omid Hashemipour **253**

Models for Quality Analysis of Computer Structures
Murad Ali Abbas, Chumachenko S.V., Hahanova A.V., Gorobets A.A., Priymak A. **258**

Expanding Wireless Bandwidth in a Power-Efficient Way:
Developing a Viable mm-Wave Radio Technology
Daniel Foty, Bruce Smith, Saurabh Sinha, Michael Schröter **264**

Sampling Theorem for Finite Duration Signal in Limited Frequency Band
Gamlet S. Khanyan **270**

SiGe HBT Performance Modeling after Proton Radiation Exposure
Konstantin Petrosyants, Maxim Kozhukhov **274**

Classical Models of Test used in Advanced Electronics Quality Assurance
Surendra Batukdeo **278**

The Use of Natural Resources for Increasing a Checkability of the Digital Components in Safety-Critical Systems
Drozd A., Kharchenko V., Antoshchuk S., Drozd J., Lobachev M., Sulima J. **283**

New version of Automated Electro-Thermal Analysis in Mentor Graphics PCB Design System
Petrosyants K.O., Kozynko P.A., Kharitonov I.A., Sidorov A.V., Chichkanov Y. N. **289**

An Approach to Testing of Planar Integrated Antennas in Frequency Range of 5–7 GHz
Aleksandr Timoshenko, Ksenia Lomovskaya, Victor Barinov, Andrey Tikhomirov **293**

Optimal project solution decision making in telecommunication systems using multicriteria optimization methods
Valery Bezruk, Alexander Bukhanko **298**

Software implementation and debugging of forward error correction codes
Alexey Smirnov, Danila Migalin, Ilya Muravyev, Leonid Pertsev **303**

Architecture of Built-In Self-Test and Recovery Memory Chips
Andrienko V.A., Moamar Diaa, Ryabtsev V.G., Utkina T.Yu. **307**

The methods of exclusion of variables in symbolic time models of linear periodically time-variable circuit
Yuriy Shapovalov, Dariya Smal **311**

Two-Component Encoding of Approximating Picture Pixels in Telecommunication Facilities
Barannik V., Dodukh A., Safronov R. **315**

Development of parameterized cell using Cadence Virtuoso
Vadim Borisov **319**

Simulation Methods of Diffusion Alloying Process by Means of Taurus TSUPREM-4 Programme
Lagunovich N.L., Borzdov V.M. **321**

Control and Diagnosis by Complexity Indicators of System Functioning Process
Tverdokhlebov V.A. **323**

Features of the Transfer of Information with Different Reliability in a Single Channel
Alexander Bakhtin, Leonid Pertsev, Olga Timofeeva **327**

Construction of Signals with Controlled Peak-Factor
Koshevyy V. M., Dolzhenko D.O. **330**

The Effective Method of Space Filtering of Noise in Rayleigh Communication Channel with the Adaptive Antenna
Maistrenko G. V., Rybalko A. M., Shokalo V. M., Strelnitskiy A. A. **333**

A New Structure for Interconnect Offline Testing
Somayeh Sadeghi-Kohan, Shahrzad Keshavarz, Farzaneh Zokaee, Farimah Farahmandi, Zainalabedin Navabi **336**

Researching of Mathematical Models Based on Optimal Control Approaches for Congestion Control in Telecommunication Network
Lemeshko A.V., Semenyaka M.V. **341**

Higher Order Propagation Modes Error and Its Compensation
Zaichenko O. B., Klyuchnyk I. I., Martynenko L. G. **345**

Strategy of analyzing most common algorithms for path finding in discrete labyrinth using software statistic data collector
Krasnov Evgeniy, Dmitry Bagaev **349**

Method of Implementation of Technology of Orders Based Transparent Parallelizing for Solving Computationally Complex Problems on Cluster
Vitaliy D. Pavlenko, Viktor V. Burdejnyj, Sergey V. Pavlenko **353**

Scheduling Tests for 3D SoCs with Temperature Constraints
Indira Rawat, Gupta M.K., Virendra Singh **356**

Automated application mapping into Network-on-Chip topologies
Bykov S. O. **360**

MIMO Radar with Phase-coded waveforms
Amirsadegh Roshanzamir, Bastani M. H. **363**

BBN-based Approach For Assessment of Smart Grid And Nuclear Power Plant Interaction
Eugene Brezhnev, Vyacheslav Kharchenko **367**

Design, Test and Fault Detection in QCA 4-to-1 Multiplexer
Zahra NajafiHaghi, Behjat Forouzandeh **374**

The Evaluation of Statistical Characteristics of the Retransmission Meter Signal Frequency and Initial Phase on the Basis of VHDL-model
Dmitry A. Velychko, Iegor I. Vdovychenko **378**

A Research of Heuristic Optimization Approaches to the Test Set Compaction Procedure Based On a Decomposition Tree for Combinational Circuits
Valentina Andreeva, Kirill A. Sorudeykin **382**

Power Reduction of 7T Dual-Vt SRAM Cell Using Forward Body Biasing
Sahba Sabetghadam Jahromi, Raziyeh Bounik **388**

VLSI: An Investigation into Electromagnetic Signatures (EMS) for Non-Invasive Testing and Signal-integrity Verification
Kadim HJ, Coulibaly L. M. **392**

Secure Data over GSM based on Algebraic Codebooks
Kazemi R., Nashtaali D., Boloursaz M., Behnia F. **397**

Simulation of Telecommunication Channel Using Volterra Model
Vitaliy D. Pavlenko, Viktor O. Speranskyy **401**

Extracting Complete Set of Equations to Analyze VHDL-AMS Descriptions
Arezoo Kamran, Vahid Janfaza, and Zainalabedin Navabi **405**

A Data Modem for GSM Adaptive Multi Rate Voice Channel
Boloursaz M., Hadavi A. H., Kazemi R., Behnia F. **409**

Trends and prospects of development of techniques for extracting acoustic sounding information of the atmospheric boundary layer
Klyuchnik I., Panchenko A., Umyarov R. **413**

Decision-Making in Robotics and Adaptive Tasks
Tsymbal A.M., Bronnikov A.I. **417**

Design of Nonvolatile Memory Based on Magnetic Tunnel Junction for Special Electronic Systems
Aleksandr Kostrov, Vladislav Nelayev, Viktor Stempitsky, Anatoly Belous, Arkady Turtsevich **421**

Improving the Dependability of a Water Supply System via a Multi-Agent based CPS
Teodora Sanislav, Liviu Miclea, Paolo Prinetto **425**

Cyber Security Lifecycle and Assessment Technique for FPGA-based I&C Systems
Illiashenko Oleg, Kharchenko Vyacheslav, Kovalenko Andriy **432**

FPGA Technologies in Medical Equipment: Electrical Impedance Tomography
Perepelitsyn Artem, Shulga Dmitry **437**

A Trend-based Design Space Exploration of Multi-core Systems Using Regression Modeling
Fazeleh Hajari Taheri, Omid Fatemi **441**

Synchronous Rectifiers Enable High Efficiency for Buck-Boost Converter
Yurii Shynkarenko and Igor Klyuchnyk **445**

Test Data Compression Strategy While Using Hybrid-BIST methodology
Elmira Karimi, Mohammad Hashem Haghbayan and Mahmood Tabandeh **449**

Self-Adaptive Mobile Wireless Hotspot Zones
Yanovsky M., Kharchenko V., Gorbenko A. **454**

The Systolic Compositions of Two-dimensional and Multidimensional Lattice Filters for Space-Time Signal Processing
David I. Lekhovytskiy, Andrii V. Semeniaka, and Dmytro S. Rachkov **458**

Power Efficient Implementation of Homogenous Multi-Core Processors
Aram Poghosyan **462**

Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices
Vladimir Hahanov, Karyna Mostova, Oleksandr Paschenko **465**

Improved Scaling-Free CORDIC algorithm
Leonid Moroz, Taras Mykytiv, Martyn Herasym **470**

Coding Tangible Component of Transforms to Provide Accessibility and Integrity of Video Data
Barannik V.V., Hahanova A.V., Krivonos V.N. **475**

Review of the botnet detection techniques
Oleg Savenko, Sergiy Lysenko, Kryshchuk Andrii **479**

MEMS Intellect Multiprobes Contacting Devices for Electrical Checking-up of Multilayers Commutative Boards and BGA/CSP Electronic Components
Nevliudov I.Sh., Palagin V.A., Razumov-Frizjuk E.A., Zharikova I.V. **483**

Internet of Things: A Practical Implementation based on a Wireless Sensor Network Approach
Michele Mercaldi, Andrea D'Oria, Davide Murru, Hai-Ning Liang, Ka Lok Man, Eng Gee Lim, Vladimir Hahanov, Mischenko Alexander **486**

Investigation of EM Wave Propagation of the Wireless Capsule in Human Body
Eng Gee Lim, Zhao Wang, Jin Hui Chen, Tammam Tillo, Ka Lok Man **490**

Using pyroelectric detectors in the design of temperature measuring devices
Bondarenko A.Yu, Klyuchnik I.I. **494**

Transaction Level Model of Embedded Processor for Vector-Logical Analysis
Irina V. Hahanova, Volodymyr Obrizan, Alexander Adamov, Dmitry Shcherbin **497**

Embedded Intelligent Control Systems on the Basis of Elementary Fuzzy-Logic Cells
Dontsova A., Vassiliev A.E. **502**

Interconnection Analysis of the Integral Reliability Characteristics of the Monoergative Computer System and User's Competency
Krivoulya G., Shkil A., Kucherenko D. **505**

System approach to determination of ADC parameters
Knyshev Ivan **511**

Methodological Aspects of Complex Ecological Estimation of Man-Caused Territory State and Mathematical Modelling of Processes in a Environment System
Kozulia T. V., Sharonova N. V. , Emelianova D. I., Kozulia M.M. **514**

Method for “Failure on Demand” Latent Faults Diagnosis of NPP Safety Control Systems
Gerasymenko K.E. **519**

Informational Saturation of Noise Signals
Kolodiy Z. A., Kolodiy A.Z. **523**

The Positional Structural-Weight Coding of the Binary View of Transformants
Barannik V., Krasnoruckiy A., Hahanova A. **525**

Synchronization of a Fuzzy Automata
Speranskiy Dmitriy **529**

Models for SoC Infrastructure of Radio Frequency Identification with Code-Division Multiple
Filippenko I.V., Hahanova I.V., Filippenko I.O, Maksimov M., Chugurov I. **535**

Factorization of Rhythmograms Parametric Spectra on the Base
of Multiplicative Linear Prediction Models
Nataliia V. Kudriavtseva, Iryna O. Fil **538**

Logi-Thermal Analysis of Digital Circuits Using Mixed-Signal Simulator Questa ADMS
Petrosyants K.O., Rjabov N.I. **541**

Method of Hybrid Regression Analysis in the Calibration Experiments
Ordinartseva N. P. **545**

Keynotes speeches and Invited Reports **548**

AUTHORS INDEX **554**

Qubit Model for Solving the Coverage Problem

Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas, Eshetie Abebech Mandefro

Computer Engineering Faculty, Kharkov National University of Radioelectronics, Kharkov, Ukraine, hahanov@kture.kharkov.ua

Abstract

Qubit (quantum) structures of data and computational processes for significantly improving performance when solving problems of discrete optimization and fault-tolerant design are proposed. We describe a hardware-focused models for parallel (one cycle) calculating the power set (the set of all subsets) on the universe of n primitives for solving coverage problems, minimization of Boolean functions, data compression, analysis and synthesis of digital systems through the implementation of the processor structure in the form of the Hasse diagram. A prototype of quantum device, implemented by programmable logic, is described.

1. Introduction

A quantum computer is designed for fault-tolerant design and solving optimization problems by way of the brute-force method through the use of set theory. Considering the discreteness and multiple-valuedness of the alphabets for description of information processes, the parallelism, inherent in the quantum computing, is particularly actual when developing effective and intelligent engines for data retrieval in cyberspace or Internet [5], tools for synthesis of fault-tolerant digital primitives and systems [4], designing and testing digital systems-on-chips [5-7], tools for solving problems of discrete optimization [3]. It does not cover the physical basis of quantum computing, originally planted in the works of scientists, focused on the use of non-deterministic quantum interactions within the atom [8-9].

2. Qubit–processor of optimal coverage (quantum processor)

Qubit (quantum) structures of data and computational processes are proposed to significantly improve performance, when solving discrete optimization problems. We describe hardware-focused models for parallel (one cycle) calculating the power set (the set of all subsets) in the universe of n primitives for solving problems of coverage, minimization of Boolean functions, data compression, analysis and synthesis of digital systems through the implementation of the processor structure in the form of the Hasse diagram.

The aim of creating the qubit-processor is significant reduction the time, when solving optimization problems by way of parallel computing vector logical operations on the set of all subsets of the primitive components through increasing the memory for storing intermediate data.

The problems are the following: 1) Definition of data structures to determine the power set, when solving the coverage problem of the columns of the matrix

$$M = \left|M_{ij}\right|, i = \overline{1,m}; j = \overline{1,n}$$

by unit values of rows. In particular, when m=n=8, it is necessary to perform a logical operation in parallel by 256 variants of all possible combinations of the vectors (matrix rows), which constitute the power set. 2) The instruction set of the processor must include the following operations (and, or, xor) on vectors (words) of the dimension m. 3) Development of a qubit processor architecture for parallel computing $2^n - 1$ combinations, focused on the optimal solving the NP-complete coverage problem. 4) Implementation of a qubit processor prototype, based on programmable PLD logic, and verification (validation) of hardware solution on the examples of minimizing Boolean functions. 5) Reduction of other practical problems of discrete optimization to a form of coverage problem for subsequent solving on the qubit-processor.

As an example, we propose to solve the problem of searching the optimal unit coverage of all the columns by minimal number of rows of the matrix M, represented below:

M	1	2	3	4	5	6	7	8
a	1	.	.	.	.	1	.	.
b	.	.	1	.	.	.	1	.
c	1	.	.	.	1	.	1	.
d	.	1	.	1	.	.	.	1
e	.	1	.	.	1	.	.	.
f	1	.	1	.	.	1	1	.
g	.	1	.	1	.	.	.	1
h	.	.	1	.	1	.	.	.

To do this, it is necessary to make search of all 255 combinations: from eight of one row, two, three, four, five, six, seven and eight. The minimum number of primitives (rows), forming the coverage, is the optimal solution. There can be several such decisions. The Hasse diagram is a compromise proposal with respect to time and memory. This is a strategy for addressing the coverage problem, when the previously obtained result is used to create a more complex superposition. Therefore, for each coverage table, containing n primitives (rows), it is necessary to generate their own multiprocessor structure in the form of the Hasse diagram, which then must be used to solve almost parallel NP-complete problem. For instance, for four rows of the coverage table the Hasse diagram – multiprocessor structure – will have the form, shown in Fig. 1.

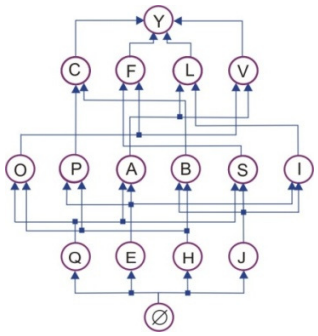

Fig. 1. Quantum structure of computational processes

The optimal solutions for the coverage problem of the matrix M, which generates 255 possible combinations, are presented by rows in the form of DNF: $C = fgh \vee efg \vee cdf$. Control automaton of the computing process for the quantum structure by means of bottom-up analysis of graph nodes is based on the following sequential steps:

1. Storing information about the primitives in the registers (the matrix) of the first level $L_i^1 = P_i$ with subsequent analysis of the coverage quality of each primitive in a binary format (1 – there is a coverage, 0 – there is not a coverage). If one of the primitive provides the coverage $\bigwedge_{j=1}^{m} L_{ij}^1 = 1$, analysis of the Hasse structure ends. Otherwise, go to the next level $(r = r + 1)$ of the graph:

$$L_i^1 = P_i \rightarrow \bigwedge_{j=1}^{m} L_{ij}^1 = \begin{cases} 0 \rightarrow n = n + 1; \\ 1 \rightarrow \text{end}. \end{cases}$$

2. Initiating instruction for processing the next (second) level. Consistent executing the vector (matrix) operations (or $L_i^r = L_{ij}^{r-1} \bigwedge_{j=1}^{m} L_{tj}^{r-1}$, and $\bigwedge_{j=1}^{m} L_{ij}^r = 1$) to analyze the coverability of combinations of primitive elements of r-level. Here $t = \overline{1,m}, i = \overline{1,m}, r = \overline{1,n}$, n – the number of layers or rows in a coverage table; m – the number of columns in it. If on the considered level there exist a combination, determining a complete coverage and forming estimation equal to 1, the processing of all subsequent processor levels is not performed. Otherwise, go to analysis of the next processor level:

$$L_i^r = L_{ij}^{r-1} \bigwedge_{j=1}^{m} L_{tj}^{r-1} \rightarrow \bigwedge_{j=1}^{m} L_{ij}^r = \begin{cases} 0 \rightarrow r = r + 1; \\ 1 \rightarrow \text{end}. \end{cases}$$

To search an optimal coverage always enough two elements of the low level; this means that all operational nodes have two register (matrix) inputs, which significantly reduces the hardware expenses. The number of time cycles for processing the processor structure in the worst case is n. An algorithm for searching the optimal coverage through top-down analysis of the graph nodes can be created. In this case, if complete coverage is found in one of the layers it is necessary one more descent by the structure to make sure that there is not complete coverage in bottom layer. If a positive answer to this question the optimal solution is obtained. Otherwise, it is necessary to carry out the descent to such level, where next bottom layer will not contain complete coverage.

The nodes of the processor structure can have more than one binary (unary) register logic operation. Then it is necessary to create a simple instruction decoder to activate, for example, the operations: and, or, xor, not.

Thus, the advantages of Qubit Hasse Processor (QHP) is the ability to use no more than two input circuits for vector logical operations (and, or, xor), and hence substantial reduction the Quine's cost of implementing processor elements (nodes) and memory through the use of sequential computation and slight increase the processing time of all Hasse graph nodes. For each node the criterion of coverage quality is used – presence of all 1's in the coordinates of the result vector. If the quality criterion is satisfied, then all the other calculations cannot be produced, because the Hasse diagram is a strictly hierarchical structure according to the number of combinations in each layer.

This means the best solution is at lower level of the hierarchy. Variants of the same level are equal by implementation (cost), so obtained first quality coverage ($Q = \sum_{i=1}^{n} q_i = n$) is the best solution, suggesting finish all subsequent calculations by the strategy of the Hasse diagram. According to a series-parallel strategy of node analysis, time (cycle) of processing all primitives of QH-processor is determined by the number of hierarchy levels (the number of bits (primitives, rows in the coverage table) in the qubit variable) multiplied by the analysis time of a single node: $T = \log_2 2^n \times t = t \times n$. At that the length m of the coverage table row does not influence on the estimation of performance. Node analysis includes two instructions: logical one (and, or, xor) and calculation of the criterion of coverage quality in the form of a scalar by applying function «and» to all bits of the result vector:

$$m_{ir,j} = M_{i,j} \vee M_{r,j}, (j = \overline{1,n}; \{i \neq r\} = \overline{1,m};);$$

$$m^{s}_{ir} = \wedge m_{ir,j} = \wedge (M_{i,j} \vee M_{r,j})$$

The hardware cost of implementing QH-processor depends on the total number of Hasse graph nodes and the number of bits (digits) in the row of coverage table:

$$H = 2^n \times k \times m,$$

where k – coefficient of hardware implementation (complexity) of a single bit of binary vector logical operation and subsequent instruction for calculating the coverage quality criterion.

Thus, high performance of solving coverage problem is achieved by increasing hardware cost (in $2^n \times k \times m / k \times m \times n = 2^n / n$ times compared to sequential processing of graph nodes), which provides a compromise between a fully parallel structure of computational processes (here hardware cost is determined by the number of primitives in each node $H = k \times m \times n \times 2^n$, increasing hardware will be in 2^n times) and serial calculations of uniprocessor computer (performance of processing Hasse graph is equal to $T = t \times 2^n$, and hardware cost is equal $H^* = k \times m \times n$). Reduction of hardware compared to the parallel graph processing is equal to $Q^H = k \times m \times n \times 2^n / k \times m \times 2^n = n$. Due to significant hardware redundancy reducing the analysis time of graph nodes compared to the serial structure processing has the following estimate:

$$Q^T = \frac{t \times 2^n}{t \times n} = \frac{2^n}{n}.$$

3. Implementation of a cubit processor of optimal coverage

The model of a quantum device is developed by Verilog language. The processor cell consists of two register gates, Fig. 2. Register element "or" performs a logical operation by two vectors, forming the vector result. Register gate "and" performs convolution of all the bits of the vector by the operation "and", forming a single-bit element that identifies the optimal solution of coverage problem.

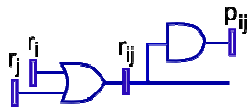

Fig 2. The unit cell of a quantum processor

A fragment of a simplified circuit of a quantum processor is shown in Fig. 3. Forming values for the Hasse diagram nodes of six levels is presented here. Each element of the circuit involves the primitive of coverage quality analysis as function "and".

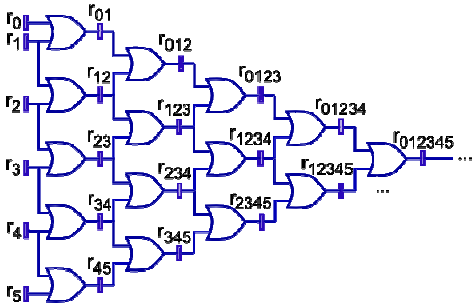

Fig.3. Fragment of the circuit of RTL-level

Implementation of the computing unit is based on FPGA of Xilinx xc3s1600e-4-fg484, the main parameters of which are as follows:

Map-report.
Logic Utilization:
Number of Slice Flip Flops: 2,286 out of 29,504 7%
Number of 4 input LUTs: 2,715 out of 29,504 9%
Logic Distribution:
Number of occupied Slices: 1,514 out of 14,752 10%
Number of Slices containing only related logic: 1,514 out of 1,514 100%
Number of Slices containing unrelated logic: 0 out of 1,514 0%
*See NOTES below for an explanation of the effects of unrelated logic.
Total Number of 4 input LUTs: 2,715 out of 29,504 9%
Number of bonded IOBs: 321 out of 376 85%
Number of BUFGMUXs: 1 out of 24 4%
Timing parameters of project:
Tclk_to_clk = 4.672 ns
Tclk_to_pad_max = 11.552 ns
Period = max{ Tclk_to_clk , Tclk_to_pad_max };
Period = 11.552 ns
Fclk = 86,5 МГц

4. Conclusion

The implementation of a quantum processor based on the Hasse structure allows reducing hardware cost in n times, compared with the parallel implementation, but it reduces the processor speed as well as in n times too. Conclusion: it is necessary to create new data structures to reduce the hardware cost for quantum computing, or more intelligent algorithms for solving coverage problem by using Hasse diagrams.

The scientific novelty lies in first proposed data model and structure of hardware implementation of a quantum computer, which is characterized by the use of Hasse structure, which enables to improve significantly (x100) speed of solving practical problems of discrete optimization.

The practical value is significant increase in speed of solving coverage problems and other problems of discrete optimization by means of increasing the hardware cost for parallel execution of vector logic operations by using Hasse-structure of quantum computing device.

Synthesis of digital Hasse structure on chip based on components (LUT, Slice, CLB) is of particular interest for its industrial use.

10. References

[1] *Keyes R.W.* Challenges for quantum computing with solid-state devices // Computer. Jan. 2005. Vol. 38, Issue 1. P. 65 – 69.

[2] *Glassner A.* Quantum computing. 3. // IEEE Computer Graphics and Applications. Nov/Dec 2001. Vol. 21, Issue 6. P. 72 – 82.

[3] *Marinescu D.C.* The Promise of Quantum Computing and Quantum Information Theory – Quantum Parallelism // Proceedings of the 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS'05). 2005. P. 112-114.

[4] *Mark Gregory Whitney.* Practical Fault Tolerance for Quantum Circuits. PhD Dissertation in Computer Science. Berkeley: University of California. 2009. 206p.

[5] *Hahanov V. I., Litvinova E. I., Chumachenko S. V., Guz O.A.* Logic associative computer. Electronic modeling. 2011. No 1, P. 73-90,

[6] *Hahanov V., Wajeb Gharibi, Litvinova E., Chumachenko S.* Information analysis infrastructure for diagnosis. Information. An international interdisciplinary journal. 2011. Japan. Vol.14. No 7. P. 2419-2433.

[7] *V.I. Hahanov et al.* Digital System-on-Chip Design and Test. Kharkov: Novoye Slovo. 2009. 484 p.

[8] *Stig Stenholm, Kalle-Antti Suominen.* Quantum approach to informatics. Published by John Wiley & Sons, Inc., Hoboken, New Jersey. 2005. 238p.

[9] *Michael A. Nielsen & Isaac L. Chuang.* Quantum Computation and Quantum Information. Published in the United States of America by Cambridge University Press, New York. 2010. 676p.

Camera-ready was prepared in Kharkov National University of Radio Electronics
Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 27.08.2012. Format 60×841/8.
Relative printer's sheets: 49. Circulation: 200 copies.
Published by SPD FL Stepanov V.V.
Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозіуму «Схід-Захід Проектування та Діагностування – 2012»
Макет підготовлено у Харківському національному університеті радіоелектроніки
Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова
Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 27.08.2012. Формат 60×84$^{1}/_{8}$.
Умов. друк. Арк. 49. Тираж: 200 прим.
Видано: СПД ФЛ Степанов В.В.
Вул. Ак. Павлова, 311, Харків, 61168, Україна