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11th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2013)

Rostov-on-Don, Russia, September 27-30, 2013

The main target of the **East-West Design & Test Symposium** (EWDTS) is to exchange experiences between the scientists and technologies of the Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic systems. The symposium aims at attracting scientists especially from countries around the Black Sea, the Baltic states and Central Asia. We cordially invite you to participate and submit your contribution(s) to EWDTS'13 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level TPG
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Test
- Power Issues in Testing
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- Using UML for Embedded System Specification

CAD Session:

- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Rostov-on-Don, Russia, one of the biggest scientific and industrial center. Venue of EWDTS 2013 is Don State Technical University – the biggest dynamically developing centre of science, education and culture.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics http://anpre.org.ua/ in cooperation with Don State Technical University and Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Aldec, Synopsys, DataArt Lab, Tallinn Technical University, Aldec Inc.

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Quantum Technology for Analysis and Testing Computing Systems

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Abstract

A theory of quantum models, methods and algorithms for improving the performance of existing software and hardware tools for analysis and synthesis of digital computing devices by increasing the dimension of the data structures and memory are proposed. The basic concepts, terminology and definitions are introduced, which are necessary for the understanding the theory and practice of quantum computation.

1. Introduction

In recent years quantum computing becomes interesting for analyzing cybernetic space, developing cloud Internet technologies, which is explained by their alternativeness to the existing models of computing processes [1]. Market feasability of quantum methods and qubit models is based on the high parallelism when solving almost all discrete optimization problems, factorization, minimization of Boolean functions, effective compression of data, their compact representation and teleportation, fault-tolerant design through significant increase in hardware costs. But now it is acceptable, because of nano-electronic technologies propose now up to 1 billion gates, located on a chip of the dimension 2x2 sm with the substrate thickness 5 microns. At that modern technologies allow creating a package (sandwich) containing up to 7 dies, which is comparable with the quantity of the human brain neurons [2]. Practically wireless connection of such chips is based on through-silicon vias (TSV) - the technological capability of drilling about 10 thousand through vias in 1 square centimeter of wafer or die. In addition, the emergence of FinFET transistors and 3D-technology based on them for implementation of digital systems provide almost unlimited hardware capabilities to researchers for creating new parallel computing devices [2-7]. So, it is necessary to use hardware-focused models and methods for creating high-speed tools for parallel solving real world problems. Discreteness and multiple-valuedness of the alphabets for describing information processes, the parallelism, inherent in the quantum computing, are particularly important when developing effective and intelligent engines for cyberspace, cloud structures and services of Internet, and tools for synthesis of fault-tolerant digital devices, testing and simulation of digital systems-on-chips, technologies for information and computer security [7-11]. We do not consider the physical basis of quantum computing, originally described in the works of scientists, focused on the use of non-deterministic quantum interactions within the atom. We do not address the physical foundations of quantum mechanics, concerning non-deterministic interactions of atomic particles [1], but we use the concept of information quantum as a joint definition of the power set (the set of all subsets) of states for the discrete cyberspace area that provides the high parallelism level of the proposed quantum models and methods.

2. The quantum method for diagnosing digital systems

Matrix method for quantum diagnosing functional failures and stuck-at faults in software or hardware units is proposed. It is based on qubit data structures comprising diagnostic information, which allows significantly reducing the computational complexity of the simulation and diagnosis due to the introduction of parallel logical operations on the matrix data. The quantum method for fault-free simulating digital units with the possibility of online repair of digital system components is presented. It is characterized by significantly improved performance due to addressed processing procedure of the functional primitives, defined by Q-coverages.

A model of diagnosing object is represented in the form of digital system, which has functional elements connected by communication lines. Among them there are assertion points, needed for verification, testing and diagnosis of faults [2]. Diagnostic information is provided by the following components: 1) the verification test for diagnosing faults of a given class, in this case they considered single stuck-at faults of circuit lines $\{\equiv 0, \equiv 1\}$. 2) Fault detection table [6], rows of which define vectors of faults, checked by each test pattern and assosiated with circuit lines. 3) the reachability matrix, which determines the reachability of each assertion point by using the set of input (previous) lines [8]. 4) Matrix of assertion engine states or output response matrix, which determines the status of each assertion on test patterns by comparing the reference response in given point with the real signal during the execution of diagnostic experiment [2,7].

The base model for diagnosing digital unit, discrete process or phenomenon is represented by the components, which create 4 dimensions in the feature space:

$$\begin{cases} D_b = \langle S, A, F, T \rangle \\ D = \{\langle S, A \rangle, \langle F, T \rangle\}; \end{cases}$$

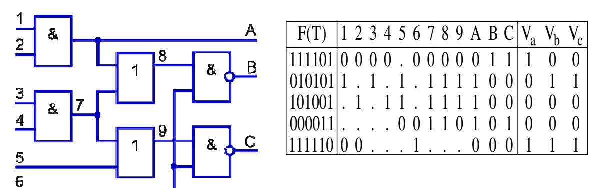
$$\begin{cases} V_b = (|S| \times |A| \times |F| \times |T|); \\ V = (|S| \times |A|) + (|F| \times |T|); \\ V_b >> V; \end{cases}$$

$$\begin{cases} S^* = f(S, A, T); \\ A^* = g(T, A); \\ F^* = h(S, A, F, T); \end{cases}$$

At that the amount of diagnostic information V is formed by the Cartesian product (powers) of four components in the order specified above: 1) the object structure; 2) assertion or monitoring engine; 3) a set of faults or modules, subject to functional failures; 4) test patterns or segments to diagnose faults or a set of these modules. Significantly reduce the amount of diagnostic information can be achieved by reducing the dimension of the feature space by partitioning the base model into two disjoint subsets $\langle S, A \rangle, \langle F, T \rangle$. In this case, the estimate of the diagnostic information is not multiplicative and additive with respect to the power of subsets, derived from partitioning, without reducing the diagnosis depth. Here, the first component of the diagnosis model is presented by reachability matrix, which allows minimizing the mask of possible faults by analyzing the structure of the circuit by comparing the true and real results of simulation of output signals for each test pattern or segment. The number of rows of this matrix is the number of observed outputs or assertions.

In realizing the diagnosis method the binary matrix of structural fault activation is created, which are a mask for a substantial reduction of the set of suspected faults when concurrent analysis of the fault detection table. In this case, the symbols of single stuck-at faults $\{0, 1, X, \varnothing\}$, $X = \{0, 1\}$ in the cells of fault detection table [6] are encoded by the corresponding qubits (10,01,11,00) of the multi-valued Cantor alphabet $A^k = \{0, 1, X, \varnothing\}$, which makes it possible to exclude the set-theoretic procedures from the calculation processes and replaced them by vector logical operations.

A fragment of digital circuit shown in Fig.1 is used for consideration of the method. There are three assertion points A, B, C to monitor the status of all circuit lines under test (during diagnostic experiment) by input five test patterns specified by a fault detection table F(T). The coordinates of the table define faults 0 and 1 detected by the test vectors, as well as the states of coordinates are: $\varnothing$ (.) – lack of detectable faults; and X – detecting constants 0 and 1 on the line simultaneously. The right side of the table is a matrix of assertion engine states as comparison results of the reference and actual responses of the digital device to the test patterns. A value of 1 means negative result (incomparable), 0 - match of the responses.



F(T)	1	2	3	4	5	6	7	8	9	A	B	C	V_a	V_b	V_c
111101	0	0	0	0	.	0	0	0	0	0	1	1	1	0	0
010101	1	.	1	.	1	.	1	1	1	1	0	0	0	1	1
101001	.	1	.	1	1	.	1	1	1	1	0	0	0	0	0
000011	.	.	.	.	0	0	1	1	0	1	0	1	0	0	0
111110	0	0	.	.	.	1	.	.	.	0	0	0	1	1	1

Fig. 1. A fragment of the digital circuit and fault detection table

The circuit structure is not taken into account in a fault detection table to enhance the diagnosis depth, based on calculating the actual state matrix of assertion engine, which together with the reachability matrix creates a structure mask, minimizing the set of suspected faults. For the fragment of a digital circuit shown in Fig. 1, the reachability matrix is as follows:

$S = \lvert S_{ij} \rvert$	1	2	3	4	5	6	7	8	9	A	B	C
1	1	1	.	.	.	.	.	.	.	1	.	.
2	1	1	1	1	.	1	1	1	.	.	1	.
3	.	.	1	1	1	1	1	.	1	.	.	1

Here assertion outputs A, B, C are monitors of the technical condition of the diagnosing object. Each of

them can have two states: $A_{ij} = \{0,1\}, A_{ij} = T_i \oplus U_j$, forming a mask of possible faults by using the following expression: $S(T_i) = \triangleleft = (\underset{A_j=1}{\vee} S_j) \wedge (\overline{\underset{A_j=0}{\vee} S_j})$. Each test-vector (segment) activates its own structure, so the mask of possible faults is functionally dependent on the structure, assertions (states of observed outputs) and test patterns: $S = f(S, A, T_i)$. Assuming that in the matrix $S = |S_{ij}|$ the output states are equal to (A,B,C) = (011), where the value 1 identifies the appearance of a fault in the unit, the mask of possible faults will be the following:

$$S = (S_2 \vee S_3) \wedge (\overline{S_1}) =$$
$$(111101110010 \vee 001111101001) \wedge (\overline{110000000100}) =$$
$$= (111111111011) \wedge (001111111011) = (001111111011).$$

The resulting mask is applied to the first row of fault detection table that defines a set of suspected faults, which form output response (A, B, C) = (011) of the device assertion on the first test-vector:

Test \ Faults	1	2	3	4	5	6	7	8	9	A	B	C
T1	0	0	0	0	.	0	0	0	0	0	1	1
S1	0	0	1	1	1	1	1	1	1	0	1	1
T1(S1)	.	.	0	0	.	.	0	0	0	.	1	1

Under the proposed procedure for obtaining a mask of one line building a matrix of structural faults activation S (T) is performed based on the use of output response table defining the states of assertion engine during test execution:

$S = \|S_{ij}\|$	1	2	3	4	5	6	7	8	9	A	B	C
1	1	1	.	.	.	.	.	.	.	1	.	.
2	1	1	1	1	.	1	1	1	.	.	1	.
3	.	.	1	1	1	1	1	.	1	.	.	1

$\xrightarrow{\triangleleft}$

T \ A	A	B	C	A(T)
T1	1	0	0	1
T2	0	1	1	1
T3	0	0	0	0
T4	0	0	0	0
T5	1	1	1	1

=

S(T)	1	2	3	4	5	6	7	8	9	A	B	C
T1	1	1	0	0	0	0	0	0	0	1	0	0
T2	0	0	1	1	1	1	1	1	1	0	1	1
T3	0	0	0	0	0	0	0	0	0	0	0	0
T4	0	0	0	0	0	0	0	0	0	0	0	0
T5	1	1	1	1	1	1	1	1	1	1	1	1

To form data structures suitable for computer processing, it is necessary to translate the symbols of a fault detection table faults in the two-digit code in accordance with the rules of $\triangleright$-coding: $\triangleright = \{0 = 10, 1 = 01, X = 11, \varnothing = 00\}$ the application of which to the fault detection table F (T) gives the following result:

F(T)	1	2	3	4	5	6	7	8	9	A	B	C
T1	0	0	0	0	.	0	0	0	0	0	1	1
T2	1	.	1	.	1	.	1	1	1	1	0	0
T3	.	1	.	1	1	.	1	1	1	1	0	0
T4	.	.	.	.	0	0	1	1	0	1	0	1
T5	0	0	.	.	.	1	.	.	.	0	0	0

$\xrightarrow{\triangleright}$

F(T)	1	2	3	4	5	6	7	8	9	A	B	C
T1	10	10	10	10	00	10	10	10	10	10	01	01
T2	01	00	01	00	01	00	01	01	01	01	10	10
T3	00	01	00	01	01	00	01	01	01	01	10	10
T4	00	00	00	00	10	10	01	01	10	01	10	01
T5	10	10	00	00	00	01	00	00	00	10	10	10

After obtaining the structural matrix, intended to mask the real faults in fault detection table it is necessary to perform #-superposition of two matrices: $F(T) = S(T) \# F(T)$, which is reduced to performing #-operation on the coordinates of the same name $F_{ij} = \overline{F}_j \leftarrow (F_j = 00) \vee (S_{ij} = 0)$ that means modification of coordinate codes in the table F (T) when the predetermined conditions fulfilled. Otherwise, the operation is reduced to the inversion of the matrix cells of fault codes, masked by zero signals of the structural activation matrix, as well as all zero codes of fault detection table. The truth table of #-operation in the symbol and coded form is shown below:

$\# = S_{ij} \setminus F_{ij}$	∅	1	0	X
0	X	0	1	∅
1	X	1	0	X

$\# = S_{ij} \setminus F_{ij}$	00	01	10	11
0	11	10	01	00
1	11	01	10	11

The truth table is changed with respect to inversion of the state 00 in 11 in the presence of "1" value of the fault activation signal, because such code (00) indicates the presence of the empty set of detectable faults in a circuit line, which is impossible. But the code 00 blocks all the calculations of the conjunction on the column, making the result in 00. The inversion of the code makes it possible not mask really faults of any signs when logical multiplying. It is assumed that it is impossible to check circuit faults of different signs on the same line by a test-vector.

Performing the superposition procedure of the structural matrix with coded fault detection table in accordance with the #-operation gives the following result:

S(T)	1	2	3	4	5	6	7	8	9	A	B	C
T1	1	1	0	0	0	0	0	0	0	1	0	0
T2	0	0	1	1	1	1	1	1	1	0	1	1
T3	0	0	0	0	0	0	0	0	0	0	0	0
T4	0	0	0	0	0	0	0	0	0	0	0	0
T5	1	1	1	1	1	1	1	1	1	1	1	1

$\xrightarrow{\#}$

$\xrightarrow{\#}$

F(T)	1	2	3	4	5	6	7	8	9	A	B	C
T1	10	10	10	10	00	10	10	10	10	10	01	01
T2	01	00	01	00	01	00	01	01	01	01	10	10
T3	00	01	00	01	01	00	01	01	01	01	10	10
T4	00	00	00	00	10	10	01	01	10	01	10	01
T5	10	10	00	00	00	01	00	00	00	10	10	10

=

F(T)	1	2	3	4	5	6	7	8	9	A	B	C
$\wedge$	10	10	01	01	11	01	01	01	01	10	10	10
	10	11	01	11	01	11	01	01	01	10	10	10
	11	10	11	10	10	11	10	10	10	10	01	01
	11	11	11	11	01	01	10	10	01	10	01	10
	10	10	11	11	11	01	11	11	11	10	10	10
F(C) =	10	10	01	00	00	01	00	00	00	10	00	00
F =	0	0	1	.	.	1	.	.	.	0	.	.

In the final stage of diagnosis a single vector operation of logical multiplication for all the rows of the modified encoded truth table F(T) is performed:

$$F(T_i) = (\underset{A_j=1}{\vee} F_j) \wedge (\overline{\underset{A_j=0}{\vee} F_j}) = (\underset{A_j=1}{\wedge} F_j) \wedge (\overline{\underset{A_j=0}{\vee} F_j}) =$$

$$= (\underset{A_j=1}{\wedge} F_j) \wedge (\underset{A_j=0}{\wedge} \bar{F}_j) = (\overset{n}{\underset{j=1}{\wedge}} F_j).$$

This makes it possible exactly detect all the faults presented in the diagnosing object, which are shown in two lower rows of the above encoded fault detection table F(T): $F = \{1^0, 2^0, 3^1, 6^1, A^0\}$.

The theoretical proof of the matrix diagnosis of single and multiple faults is presented below in the form of two theorems.

Theorem 1: Single stuck-at faults of a digital circuit, defined by qubits (two digit vectors) on the test patterns of multi-valued fault detection table, are determined by using vector and-operation, masked in rows by output response vector A(T) for all assertion points:

$$F(T_i) = (\underset{A_j=1}{\vee} F_j) \wedge (\overline{\underset{A_j=0}{\vee} F_j}) =$$

$$= (\underset{A_j=1}{\wedge} F_j) \wedge (\underset{A_j=0}{\wedge} \bar{F}_j) = (\overset{n}{\underset{j=1}{\wedge}} F_j).$$

The expression is true, because: 1) The second multiplier is pure mathematics - the negation of the disjunction is the conjunction of negations, which means the multiplication of table codes by their preliminary negation. 2) The first multiplier is focused on detection the consistent faults, so it is replaced by $\underset{A_j=1}{\wedge} F_j$. Indeed, in one line or a variable two detected faults of opposite sign cannot be present simultaneously. Therefore, in the basic formula the fault disjunction $\underset{A_j=1}{\vee} F_j$ is largely focused on detecting multiple faults, but not associated with a single line. Multiplicity of discrepant faults on one line, as well as the inversion of the empty fault set, theoretically creates conditions for smooth multiplying other cells of a column in order to form in each line result in the form of a fault of one sign or an empty fault set.

Theorem 2: Multiple stuck-at faults of digital circuit, defined by qubits on test patterns of multi-valued fault detection table, are defined by using vector or-and-operations, masked in rows by an output response vector A (T) for all assertion points:

$$F(T_i) = (\underset{A_j=1}{\vee} F_j) \wedge (\overline{\underset{A_j=0}{\vee} F_j}) = (\underset{A_j=1}{\vee} F_j) \wedge (\underset{A_j=0}{\wedge} \bar{F}_j).$$

The expression is true because: 1) The second multiplier is pure mathematics - the negation of the disjunction is the conjunction of negations, which means the multiplication of table codes by their preliminary negation. 2) The first multiplier is focused on detection the multiple faults in the assumption that two detectable faults of opposite sign may be present simultaneously on a line or variable. This formula is more focused on detection of multiple faults in blocks of digital systems not connected with a single line. Multiplicity of faults in a digital system theoretically creates conditions for logical addition of other column cells to form result in the form of fault set, forming a predetermined output response vector; detectable by a test faults, which do not affect on appearance of incorrect responses on outputs, must be subtracted from them.

Detecting multiple faults based on Hasse multiprocessor, which is focused on solving the coverage problem by complete enumeration of events, ensuring exact coverage of output response vector by columns of fault detection table is interesting:

$$F(T_i) = (\underset{j}{\vee} F_j) \oplus A = 0.$$

This solution is a combination of columns, involved in vector operations of logic addition (OR), which provides the equality to output response vector. Because the operation is time-consuming, then it should be used Hasse multiprocessor, focused on calculating the power set in almost parallel mode.

To sum up, it should be noted that a model for diagnosing digital devices contains transducers, focused to implementation of the following steps (Fig. 2):

1. Preprocessing. Generating the initial diagnostic information in the form of diagnostic test, fault detection table and reachability matrix of a digital system.

2. Testing real unit, based on the use of industrial simulator to compare the actual responses and reference values on the observed assertion lines, which

enables to form a matrix of output responses or output response vector in binary alphabet.

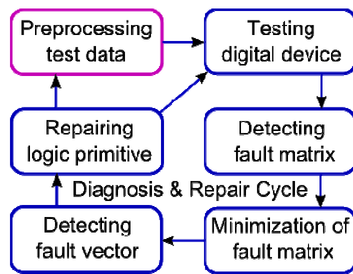


Fig. 2. Diagnosis and repair cycle

3. Calculating the activity matrix of the graph structure for each input test pattern, which is equal to the dimension of fault detection table by using the output response matrix and reachability matrix, which allows significantly reducing the area of suspected faults

4. Modification of the content of the fault detection table by means of their masking by an activity matrix of graph structure in order to detect only those faults, which really form an output response matrix in the diagnostic process.

5. Executing the procedure of logical multiplication of the fault detection table rows to obtain the vector of suspected faults.

6. Repairing digital unit by means of readdressing the faulty logic components to their analogues from spares and repeating the diagnosis process.

3. Conclusion

A theory and implementation of quantum models, methods and algorithms to improve the performance of existing software and hardware tools for analysis and synthesis of digital computing devices by increasing the dimension of the data structures and memory are proposed.

A matrix method for quantum diagnosing functional failures and stuck-at faults in software or hardware units is described; it is focused on the qubit structures of diagnostic information that allows significantly reducing the computational complexity of simulation and diagnosis through the introduction of parallel logic operations on matrix data.

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