

KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2013)

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Rostov-on-Don, Russia, September 27 – 30, 2013

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11th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2013)

Rostov-on-Don, Russia, September 27-30, 2013

The main target of the **East-West Design & Test Symposium** (EWDTS) is to exchange experiences between the scientists and technologies of the Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic systems. The symposium aims at attracting scientists especially from countries around the Black Sea, the Baltic states and Central Asia. We cordially invite you to participate and submit your contribution(s) to EWDTS'13 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level TPG
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Test
- Power Issues in Testing
- Real Time Embedded Systems

- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- Using UML for Embedded System Specification

CAD Session:

- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Rostov-on-Don, Russia, one of the biggest scientific and industrial center. Venue of EWDTS 2013 is Don State Technical University – the biggest dynamically developing centre of science, education and culture.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics <http://anpre.org.ua/> in cooperation with Don State Technical University and Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Aldec, Synopsys, DataArt Lab, Tallinn Technical University, Aldec Inc.



CONTENTS

| | |
|---|-----------|
| Impact of Process Variations on Read Failures in SRAMs Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y. | 15 |
| Noise Effect Estimation and Reduction in High-Speed Voltage Controlled Oscillators Vazgen Melikyan, Abraham Balabanyan, Armen Durgaryan | 19 |
| A Probabilistic Approach for Counterexample Generation to Aid Design Debugging Payman Behnam, Hossein Sabaghian-Bidgoli, Bijan Alizadeh, Kamyar Mohajerani, Zainalabedin Navabi | 23 |
| Hybrid History-Based Test Overlapping to Reduce Test Application Time Vahid Janfaza, Payman Behnam, Mohammadreza Najafi, Bahjat Forouzandeh | 28 |
| A Mathematical Model for Estimating Acceptable Ratio of Test Patterns Vahid Janfaza, Paniz Foroutan, M. H. Haghbayan, Zain Navabi | 32 |
| Session based Core Test Scheduling for Minimizing the Testing Time of 3D SOC Surajit Roy, Payel Ghosh, Hafizur Rahaman, Chandan Giri | 36 |
| Functional Fault Model Definition for Bus Testing Elmira Karimi, Mohamad Hashem Haghbayan, Adele Maleki, Mahmoud Tabandeh | 40 |
| Evolution of von Neumann's Paradigm: Dependable and Green Computing Kharchenko V., Gorbenko A. | 46 |
| Quantum Technology for Analysis and Testing Computing Systems Wajeb Gharibi, Hahanov V.I., Anders Carlsson, Hahanova I.V., Filippenko I.V. | 52 |
| Diversity Assessment of Multi-Version NPP I&C Systems: NUREG7007 and CLB-BASED Techniques Kharchenko V., Duzhyi V., Sklyar V., Volkoviy A. | 57 |
| Features of Design, Implementation, and Characterization of On-Chip Antennas for Microwave Frequencies Aleksandr Timoshenko, Ksenia Lomovskaya, Mikhail Suslov | 62 |
| Design and Optimization of a Planar UWB Antenna Eng Gee Lim, Zhao Wang, Gerry Juans, Ka Lok Man, Nan Zhang, Vladimir Hahanov, Eugenia Litvinova, Svetlana Chumachenko, Mishchenko Alexander, Dementiev Sergey | 67 |
| Cloud Traffic Control System Hahanov V.I., Guz O.A., Ziarmant A.N., Ngene Christopher Umerah, Arefjev A. | 72 |
| Cloud Infrastructure for Car Service Litvinova E.I., Englesy I.P., Miz V.A., Shcherbin D. | 77 |

| | |
|--|------------|
| Quantum Computing Approach for Shortest Route Finding Volodymyr Hahanov, Volodymyr Miz | 85 |
| Quantum Modeling and Repairing Digital Systems Baghdadi Ammar Awni Abbas, Hahanov V.I., Palanichamy Manikandan, Litvinova E.I., Dementiev S. | 88 |
| Quantum Models for Description of Digital Systems Hahanov V.I., Hahanova I.V., Litvinova E.I., Priymak A., Elena Fomina, Maksimov M., Tiecoura Yves, Malek Jehad Mohammad Jararweh | 94 |
| A Concept of Computing Based on Resources Development Analysis Drozd J., Drozd A., Zashcholkin K., Antonyuk V., Kuznetsov N., Kalinichenko V. | 102 |
| Blind Least Mean Square Criterion Algorithms for Communication Adaptive Arrays Victor I. Djigan | 108 |
| Estimation of structural complexity of IIR digital filters Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich | 113 |
| ASICPlacementAnalyzer: Software Tool for Data Analysis and Visualization of ASIC Placement Victor M. Kureichik, Maria V. Lisyak | 118 |
| Robust Watermarking System for Audio Identification Aleksandr V. Shishkin | 122 |
| Adaptive Artificial Boundary Conditions for Schrödinger Equation Taking into Account the First Order Dispersion of Laser Pulse and Diffraction of Laser Beam Vyacheslav A. Trofimov, Anton D. Denisov | 125 |
| Research of Methods to Create Informational Composition With the View of CAD of Intellectual Training Devices Knowledge-Based Signals of Cerebral Cortex Lavlinskiy V.V., Bibikov D.V., Burov R.B., Tabakov Y.G., Zolnikov K.V., Achkasov V.N. | 129 |
| Development of Upgraded Version of Finite Element Package ACELAN Arcady Soloviev, Pavel Oganesyan, Darya Krivorotova | 133 |
| Statistical Characteristics of Envelope Outliers Duration of non-Gaussian Information Processes Artyushenko V. M., Volovach V. I. | 137 |
| Optimizing Test Time for Core-Based 3-D Integrated Circuits by a Technique of Bi-partitioning Manjari Pradhan, Chandan Giri, Hafizur Rahamany, Debesh K. Das | 141 |
| Basic Concept of Linear Synthesis of Multi-Valued Digital Structures in Linear Spaces Chernov N.I., Yugai V.Ya., Prokopenko N.N., Butyrlagin N.V. | 146 |

| | |
|--|------------|
| Boundary Problem for Nonlinear Elliptic Equations on Video Card Hasmik A. Osipyan | 150 |
| The High-Frequency Correction Circuit for Resistive Voltage Dividers with Capacitive Load Prokopenko N.N., Budyakov P.S., Butyrlagin N.V. | 154 |
| Simulation Features of Diffusion Doping Process by Means of Software Package of Synopsys Company Lagunovich N.L., Borzdov V.M., Turtsevich A.S. | 158 |
| Synthesis Circuit Correction for Speed Sensors of Physical Quantities and Current-Voltage Converters with Parasitic Capacitance Prokopenko N.N., Gaiduk A.R., Budyakov P.S., Butyrlagin N.V. | 161 |
| Microwave Selective RC Amplifiers with Control Parameters Prokopenko N.N., Krutchinsky S.G., Budyakov P.S. | 165 |
| Using Java Optimized Processor as an Intellectual Property core beside a RISC Processor in FPGA Mohammad Erfan Khazaee, Shima Hoseinzadeh | 169 |
| The automated testing system for optimizing and parallelizing program transformations Alymova E., Golozubov A., Morylev R., Pitinov A., Steinberg R. | 175 |
| Methodology to Design-For-Testability Automation for Mixed-Signal Integrated Circuits Sergey Mosin | 178 |
| Static Analysis of HDL Descriptions: Extracting Models for Verification Alexander Kamkin, Sergey Smolov, Igor Melnichenko | 184 |
| Fault-Injection Testing: FIT-Ability, Optimal Procedure and Tool for FPGA-Based Systems SIL Certification Kharchenko V., Sklyar V., Odarushchenko O., Ivasuyk A. | 188 |
| Query Optimization Based on Time Scheduling Approach Wajeb Gharibi, Ayman Mousa | 193 |
| Analysis of Error-Detection Possibilities of CED Circuits Based on Hamming and Berger Codes Valery Sapozhnikov, Vladimir Sapozhnikov, Dmitry Efanov, Anton Blyudov | 200 |
| Low-Power Design of Combinational CMOS Networks Dmitry Cheremisinov, Liudmila Cheremisinova | 208 |
| IGBT on SOI. Technology and Construction Investigation Ivan Lovshenko, Vladislav Nelayev, Sergey Shvedov, Vitaly Solodukha, Arkady Turtsevich | 212 |
| Generating Pipeline Integrated Circuits Using C2HDL Converter Denis Dubrov, Alexander Roshal | 216 |

| | |
|--|------------|
| Data-Flow Multiprocessor with Deterministic Architecture Novatsky A. A., Glushko Je. V., Chemeris A.A., Pugachov O.S. | 220 |
| An Approach to Estimate the Error of Oscillator Time-Domain Analysis Vadim N. Biryukov, Alexandr M. Pilipenko | 223 |
| Sampling Theorem Applied to Data Interpolation Problem Gamlet S. Khanyan | 227 |
| A Few Test Generation Algorithms for web Applications from Imitational Model Anahit Asatryan | 231 |
| Design Automation Tool to Generate EDIF and VHDL Descriptions of Circuit by Extraction of FPGA Configuration Cheremisinov D.I. | 235 |
| Object-Oriented Approach to Software Implementation of Virtual Laboratory Workshop Gubsky D.S., Zemlyakov V.V., Mamay I.V., Sinyavsky G.P. | 239 |
| Schematic Design of HF and UHF Op-Amp for SiGe Technology Sergei G. Krutchinsky, Evgeniy A. Zhebrun, Victor A. Svizev | 243 |
| Improvement of Common-Mode Rejection Ratio in Symmetrical Differential Stages with Dynamic Load Sergei G. Krutchinsky, G.A. Svizev, Alexey E. Titov | 247 |
| Adaptation of the FPGA to Logic Failures Tyurin S.F., Grekov A.V., Gromov O.A. | 251 |
| Testable Combinational Circuit Design Based on Free ZDD-implementation of Irredundant SOP of Boolean Function Ostanin S. | 257 |
| On the Problem of Selection of Code with Summation for Combinational Circuit Test Organization Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov, Anton Blyudov | 261 |
| A 6-bit CMOS Inverter Based Pseudo-Flash ADC with Low Power Consumption Morozov D.V., Pilipko M.M., Piatak I.M. | 267 |
| Method of free C++ code migration between SoC level tests and stand-alone IP-Core UVM environments Fedor Putrya | 271 |
| A List Decoding Algorithm for Practical Reed-Solomon codes Sergey Egorov | 275 |
| On Stability of Optimization Process for Analog Circuits Markina T., Zemliak A. | 279 |

| | |
|--|------------|
| Analysis of Converters with Heterogeneous Three-Pole Chain Structure Zhanna Sukhinets, Artur Gulin | 283 |
| The Modeling of Electromagnetic Fields Intensity in Urban Development Condition Anishin M.M., Zargano G. F., Zemlyakov V.V., Hondu A.A. | 287 |
| Estimation of Radio Wave Frequency Shift and Phase Incursion on the Basis of FPGA in the Retransmission Meter Vdovychenko I.I., Velychko D.A. | 291 |
| Delay Testable Sequential Circuit Designs Matrosova A., Mitrofanov E., Singh V. | 293 |
| Supervision in Airborne Systems with Antenna Array Klochko V.K., Nguyen Tr.T. | 297 |
| Self-timed Functionally Complete Tolerant Element with Different Supply Voltage Kamenskih A.N., Tyurin S.F. | 300 |
| SPICE Model Parameters Extraction Taking into Account the Ionizing Radiation Effects Konstantin Petrosyants, Maxim Kozhukhov | 304 |
| Analysis and Simulation of Temperature-Current Rise in Modern PCB Traces Petrosyants K.O., Kortunov A.V., Kharitonov I. A., Popov A.A., Gomanilova N.B., Rjabov N.N. | 308 |
| Coupled TCAD-SPICE Simulation of Parasitic BJT Effect on SOI CMOS SRAM SEU Petrosyants K.O., Kharitonov I.A., Popov D.A. | 312 |
| Digital Converter of Frequency Deviation Based on Three Frequency Generator Shakurskiy M.V., Shakurskiy V.K., Ivanov V.V. | 316 |
| Comparative Analysis of Coding Effectiveness in Telecommunication Systems with ARQ Anfalov K. V., Volovach V. I. | 320 |
| Multiagent Bionic Algorithm for Optimization of Circuitry Solutions Andrey Bereza, Andrey Strogenko, Luis Blanco | 324 |
| Nonlinear Filtering of Pseudonoise Signals Using High-Order Markov Chain Model Dmitriy Prozorov, Anton Chistyakov | 328 |
| Representation of Solutions in Genetic Placement Algorithms Zaporozhets D.U., Zaruba D.V., Kureichik V.V. | 332 |
| Digital Adaptive System of Linearization Power Amplifier Natalya V. Gudkova, Vladimir M. Chuykov, Ksenya V. Besklubova | 336 |
| A Parallel Shrinking Algorithm for Connected Component Labeling of Text Image Sergey S. Zavalishin, Yury S. Bekhtin | 340 |

| | |
|---|------------|
| Automated Measurement of Digital Video Cameras Exposure Time Budilov V.N., Volovach V.I., Shakurskiy M.V., Eliseeva S.V. | 344 |
| Hybrid Pareto-Evolutionary Algorithm for Solving Mathematical Models of High Dimensional Electronic Circuits (HPEA) Vadim Beglyarov, Andrey Bereza, Luis Blanco | 348 |
| Finite State Machine Synthesis for Evolutionary Hardware Andrey Bereza, Maksim Lyashov, Luis Blanco | 352 |
| Increasing Efficiency of Information Transmission with Interference Influence by the Use of Multi-parameter Adaptation Nechaev Y.B., Kashenko G.A., Plaksenko O.A. | 356 |
| Analysis of Ferromagnetic Structures Fast-Acting Under the Influence of External Magnetic Fields of Various Intensity Alexander Shein, Gennady Sinyavsky, Larissa Cherkesova, George Shalamov | 360 |
| Modeling Using Multivariate Hybrid Regression Analysis Method Danilov A. A., Ordinartseva N. P. | 365 |
| Analog Input Section of the Ultrafast ADCs Prokopenko N.N., Serebryakov A.I., Butyrlagin N.V., Pakhomov I.V. | 368 |
| A Recursive Least Squares Solution to AOA Based Passive Source Localization Hejazi F., Azimi K., Nayebi M.M. | 371 |
| Identification Discrete Fractional Order Linear Dynamic Systems with Errors-in-Variables Ivanov D.V. | 374 |
| Self-Calibration Method for Capacitor Mismatch Elimination Vazgen Melikyan, Harutyun Stepanyan, Ani Aleksanyan, Ani Harutyunyan, Armen Durgaryan | 378 |
| Whitespace Calculation in 3D IC Ara Gevorgyan | 382 |
| Low-Voltage Compatible Linear Voltage Ramp Generator for Zero-Crossing-Based Integrators Melikyan Vazgen Sh., Dingchyan Hayk H., Sahakyan Arthur S., Vardan Grigoryants P., Safaryan Karo H. | 386 |
| High Accuracy Equalization Method for Receiver Active Equalizer Melikyan Vazgen Sh., Sahakyan Arthur S., Safaryan Karo H., Dingchyan Hayk H. | 390 |
| Implementation of Parallel Dataflow Computational Model on Cluster Supercomputers Levchenko N.N., Okunev A.S., Klimov Ark.V., Zmejov D.N. | 394 |

| | |
|--|------------|
| Semiconductor Electronic Parts Testing Efficiency Martynov Oleg, Ogurtsov Alexander, Sashov Alexander | 397 |
| An Approach to Accelerated Life Tests of Electronic Components Koulibaba Andrey, Krasnov Mikhail, Prischepova Svetlana | 401 |
| Next Generation Visual Programming Technology Velbitskiy I.V. | 404 |
| Efficient Calculation of Cyclic Convolution by Means of Fast Fourier Transform in a Finite Field Amerbaev V.M., Solovyev R. A., Stempkovskiy A.L., Telpukhov D.V. | 411 |
| High-level Test Program Generation Strategies for Processors Shima Hoseinzadeh, Mohammad Hashem Haghbayan | 415 |
| Fault Tolerance of the Distributed Structure of Object Controllers for Automation of Transport Sergey Rodzin, Lada Rodzina | 419 |
| Effective planning of calculations on the PDCS "Buran" Architecture Levchenko N.N., Okunev A.S., Zmejeyev D.N., Klimov A.V. | 423 |
| Ways to Ensure the Stability of Circuits to Single Events in the Design of Radiation-Resistant Circuits Smerek V.A., Utkin D.M., Zolnikov V.K. | 426 |
| Smart Road Infrastructure Artur Ziarmand | 430 |
| Testing of Transport System Management Strategy Sergey Lupin, Than Shein, Kyaw Kyaw Lin, Anastasia Davydova | 435 |
| The Bioinspired Algorithm of Electronic Computing Equipment (ECE) Schemes Elements Placement Kureichik V.V., Kureichik VI.VI. | 439 |
| The Hardware Architecture and Device for Accurate Time Signal Processing Jiř í Dost´al, Vladim´ir Smotlacha | 443 |
| Management Methods of Computational Processes in the PDCS "Buran" Levchenko N.N., Okunev A.S., Zmejeyev D.N., Klimov A.V. | 446 |
| Service-Oriented Computing (SOC) in a Cloud Computing Environment Petrenko A.I. | 449 |
| The Methodology of Two-Stage Masking Images in Information and Telecommunications Systems Barannik V. V., Vlasov A. V., Shiryayev A. V. | 453 |

| | |
|--|------------|
| Perforated with Technology of Description Massives Differential Representation in the Delivery Compressed Images Systems Kulitsa O.S., Lekakh A.A., Akimov R.I. | 457 |
| Method of Coding Bitmap Transformant to Improve Image Compression while Maintaining a Predetermined Quality Image to be Transmitted in Infocommunication Real Time Systems Krasnorutskiy A.A., Hahanova A.V., Demedetskiy A.O. | 461 |
| Method Structure Coding of Aperture Elements for Image in Infocommunication Systems Barannik V.V., Dodukh A.N., Krivonos V.N. | 465 |
| Domain-Driven Design the Database Structure in Terms of Metamodel of Object System Pavel P. Oleynik | 469 |
| An Approach to the Fuzzy Logic Modeling of Digital Devices Dmitriy Speranskiy | 473 |
| Reconfiguration of FPGAs Using Genetic Algorithms Gorodilov A. Yu., Tyurin S. F. | 477 |
| Algorithm for Automated Custom Network-on-Chip Topologies Design Bykov S. O. | 481 |
| Choice of Variants of Radio-Frequency Identification Systems on Set of Quality Parameters Bagdasaryan A.S., Kashenko A.G., Kashenko G.A., Semenov R.V. | 484 |
| Green logic FPGA Tyurin Sergey, Kharchenko Vyacheslav, Prokhorov Andrey | 489 |
| Restoration missing values of discrete signal during the calibration ADC with build-in interpolation Koroleva Ksenia, Gritsutenko Stanislav | 492 |
| Keynotes Speeches and Invited Reports | 496 |
| AUTHORS INDEX | 501 |

Quantum Models for Description of Digital Systems

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Abstract

Quantum models for description of digital systems and results of studies concerning the models and methods of quantum diagnosis of digital systems, qubit fault simulation and analysis of fault-free behavior are presented.

1. Introduction

Quantum calculators are effectively used for fault-tolerant design and solving optimization problems by way of the brute-force method through the use of set theory [1-7]. A set of elements in the traditional computer is orderly, because each bit, byte or other component has its own address. Therefore, the set-theoretical operations are reduced to exhaustive search of addresses of primitive elements. Address order of data structures useful for applications where model components can be strictly ranked, which makes it possible to carry out their analysis in a single pass (a single iteration). If there is not order in the structure, for example, the set of all subsets, the classical model of memory and computational processes disimprove the analysis time of primitive association equal by the rank, or processing of associative groups is ineffective.

What can be offered for unordered data instead of the strict order? Processor, where the unit cell is the image or pattern of the universe of n primitives, which generates $Q = 2^n$ all possible states of a cell as a power set or the set of all subsets. Direct solution about creating such cell is based on unitary positional coding states of primitives that form the set of all subsets and in the limit the universe of primitives by superposition of last ones [8]. History of the issue of the necessity for developing quantum computing on the background of the technological revolution in nano-electronics fit in a few of clear theses:

1) Quantum Computer was created the experts in the field of quantum mechanics and electronics, who introduced the idea of creating a non-numeric analog-based computer.

2) The introduced notion of a qubit [9-11] corresponds to the power set of primitives, which is the ideal nonnumeric form of object component description for analysis, synthesis and optimization of discrete objects.

3) The forms of qubit representation are the following: 1. The universe of primitive symbols, which generate the set of all subsets (power set). 2. Binary vectors, where the power set is a combination of unit values of primitives. 3. Hasse diagram, which forms the power set of all possible solutions on the graph. 4. Full transition graph, which determines the set of all subsets of transitions in the form of arcs. 5. The geometric representation in a plane for a qubit in the form of points and segments corresponding to the Boolean (power set).

4) In practice, more than 90% of all IT-industry problems associated with information retrieval in cyberspace, pattern recognition and decision-making are related to the field of discrete mathematics, where it is difficult to find a place of numerical arithmetic.

5) It is necessary to create associative logic brain-like parallel (quantum) processors, which effectively use Boolean (qubit) primitives or elements (sets) to solve problems of discrete mathematics.

6) Set-theoretic operations have to be replaced the isomorphic logical instructions (and, or, not, xor) for the subsequent creating a new system of parallel qubit programming to solve logic and optimization problems, based on qubit data structures.

7) Another solution for organization computing is associated with topological representation of the qubit, where the elements are the geometric shapes [6].

8) Nonnumeric problems, focused to the use of quantum processor are the following: minimization of forms of Boolean functions, when describing complex systems; searching paths in the graph; testing and diagnosis of digital systems; combinatorial studies of processes and phenomena; intelligent data searching, pattern recognition and decision making; discretization of fuzzy models and methods, when creating the intelligence; digital data processing and the developing efficient codec for DSP-devices.

2. Quantum models for description of digital systems

Information quantum is a spatio-temporal frame of vector description of the functionality in the form of a qubit, specifying the power set of states on the set of variables.

Qubit is a vector or:

1) The vector form of unitary coding of primitive universe to represent power set, which allows using logic operations instead of set-theoretic ones to significantly speed up the processes of synthesis and analysis of discrete systems.

2) The vector form of compact definition of digital system functionalities and their components in the form of address ordered values of input variables for status column of the truth table.

Qubit synonymous are: Q-coverage, vector truth table, implicit truth table, implicitly addressed status vector of functionality, vector or tuple of implicitly addressed functionality states, vector form of a cubic coverage. Qubit is a functional abstraction, and quantum is a component of the system.

Information quantum of the system is a structural primitive, which is invariant to the implementing technologies of the functionality (hardware, software). Moreover, the quantum synthesis of digital systems is no longer tied to the mandatory existence of an inverter that provides functionally complete basis. The quantum format $Q = (X, Q, Y)$ includes interface, input and output variables, as well as qubit-vector Q , defining the functionality $Y = Q(X)$, dimension of which is determined by the power function of the number of

input lines $k = 2^n$. The modeling procedure on the quantum of the functionality is reduced to writing the qubit bit status in the output variable Y , the address of which is generated by concatenation of the states of the

input variables: $Y = Q(X) = Q(X_1 * X_2 * \dots * X_j * \dots * X_k)$. For modeling digital systems, where components are interrelated quantum-primitives, based on the vector of equipotential lines M , the procedure for processing quantum is defined by the expression: $M(Y) = Q[M(X)] = Q[M(X_1 * X_2 * \dots * X_j * \dots * X_k)]$.

Given the through numbering of the quantum primitives the universal procedure for modeling current i -quantum will have the following format: $M(Y_i) = Q_i[M(X_i)] = Q_i[M(X_{i1} * X_{i2} * \dots * X_{ij} * \dots * X_{ik})]$.

In this case, the algorithm for analyzing digital system is greatly simplified; the speed of interpretive simulation is increased in 2^n times due to increase of

memory volume for describing the functionality of the circuit structure.

Synthesis of a quantum of digital system is reduced to superposition of the quanta of its functionalities. For example, for the three quanta-primitives, which compose a circuit, the operation of superposition forms a quantum of whole functionality, where the dimension of the qubit-vector will be greater than the sum of the qubits of original primitives:

$$\begin{array}{|c|c|c|c|c|} \hline a & & & & \\ \hline b & 0 & 0 & 0 & 1 \\ \hline c & & & & \\ \hline d & 1 & 1 & 1 & 0 \\ \hline e & & & & \\ \hline \end{array} \begin{array}{|c|c|c|c|c|} \hline c & & & & \\ \hline f & 1 & 1 & 1 & 0 \\ \hline g & & & & \\ \hline \end{array} = \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline a & & & & & & & & & & & & & & \\ \hline b & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ \hline d & & & & & & & & & & & & & & \\ \hline e & & & & & & & & & & & & & & \\ \hline \end{array} g$$

But at the same modeling procedure will be represented by only one qubit reference to read the contents from the cell instead of three ones, when the system consists of three qubits. Qubit representation of the functional elements makes it possible to introduce new circuit design symbols associated with the decimal number of the quantum vector defining functionality.

If a system of logic elements has $n=2$ inputs, then the number of possible functions is equal to $k = 2^{2^n}$, where the types or numbers of functional are shown in the bottom line of the table below:

| | | | | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 01 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| 10 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| f = | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

Moreover, on the basis of a set of qubits of the first level, defining functions of two variables, we can enter a qubit for unitary encoding two-input functions that allows creating a structure for simultaneous defining and analyzing all the states of the discrete system, where the input variables are the functionals of the first level:

| | | | | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 01 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Q = | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

| | | | | | | | | | | | | | | | | |
|-----|----|---|---|---|---|---|---|---|----|----|----|----|---|----|---|---|
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 01 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Q = | 11 | 3 | 5 | 8 | 1 | 2 | 0 | 7 | 12 | 13 | 14 | 15 | 6 | 10 | 9 | 4 |

This table four vectors-primitives of input variables (00,01,10,11) are shown, which form $k = 2^{2^2} = 2^4$

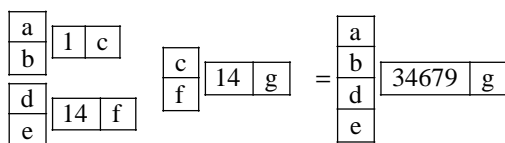
complete set of all possible functions, which are treated as primitives of second level. Then the vectors - primitive of output variables (16 columns from 0000

up to 1111), form already $k = 2^{2^4} = 2^{16}$ functional primitives, which are part of a more complex discrete system; they can be analyzed in parallel! Further it is possible to extrapolate creating a more complex system of qubits, where the vector $Q=0111110000001100$ represented in bottom line will be considered as one of $k = 2^{2^{16}}$ primitives of the third hierarchy level. In each hierarchy level of qubits the number or Boolean (power set) of states depends exponentially on the

number of primitives-vectors $k = 2^{2^n}$. If the vector Q has all unit values $Q=1111111111111111$, it simultaneously determines the space that contains 16 symbols of two-stroke alphabet, which correspond to the Boolean (power set) on the universe of four primitives.

The main innovative idea of quantum computation compared to the von Neumann machine is to move from computational procedures of the byte-operand, defining in the discrete space a single solution (point) to the quantum parallel processes of the qubit-operand, at the same time forming the power set of solutions. In this thesis the future of high-performance computers for parallel non-digit analysis and synthesis of structures and services for discrete cyberspace are formulated. Otherwise, computational complexity of the procedure for processing a set of n elements in a quantum processor and a single element in von Neumann machine are equal due to respective n-fold increase in the hardware complexity of the quantum structure.

Three-element circuit, presented above by quanta or vectors, can be represented by circuit, where corresponding decimal numbers will be featured instead of the vectors:



When processing this form of functional quanta it is necessary to expand the decimal code to binary vector and calculate the address of a cell, the contents of which will determine the state of the output variable, in this case – g.

A somewhat different circuitry, not based directly on the transistors can be presented in the form of graph structures, where each node (arc) is identified with the functional transformation, which is given by the

quantum vector. The arc (node) defines the relationship between the functional quanta, as well as input and output variables. The implementation of such structures is based on the memory cells (FPGA LUTs), which are capable to store information in the form of a vector, where each bit or digit has a unique address, identified with the input word. However, the software implementation of the structures is competitive in EDA market in speed due to addressed implementation of modeling processes for the functional quanta. In addition, hardware support for EDA systems in the form of Hardware Embedded Simulator (HES, Aldec) acquires a new motivation for system-level design of digital products, when software and hardware solutions have the same quantum format. Three generic graph forms of digital functionality, which use the quantum vectors to define the behavior of logical primitives, are shown in Fig. 1. The right form is interesting by its register implementation that can be used to formalize the descriptions of both software and hardware models of gate, registry and system levels. Now this presentation is unusual and difficult for perceiving by a person, but it is technological and easily “understood” by computer to automatically create efficient software systems for analyzing and synthesizing computing structures and cyberspace services.

A one-dimensional quantum is a vector describing the functionality. It can be associated with the output (internal) line of the unit, which is formed by the quantum in simulation process. The register implementation of a combination unit can be represented by the modeling vector M; the functionality with arcs is associated with non-input lines going from the input variables, the states of which form an address of a quantum bit. The functionality forms the states of non-input line under study. Otherwise, if the functionality is described by single output primitives, each of them can be identified by number or coordinate of non-input line associated with the element. If the functionality is multi-output, the qubit is represented by a matrix with the number of rows equal to the number of outputs. The preference of such primitive lies in the parallelism of concurrent computing the states of several outputs in one access to the matrix at the current address! This fact is an important argument in favor of synthesis of generalized qubits for fragments of a digital unit or whole circuit for their parallel processing in a single time frame.

The ideal data structure, where the quanta of functionalities and numbers of input variables are associated with non-input lines of the unit, is the following structured table:

| | | | | | | | | | | | | |
|---|---|---|---|---|----|----|----|----|----|----|----|---|
| L | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |
| M | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | |
| X | . | . | . | . | 13 | 34 | A7 | 75 | 12 | 86 | 96 | |
| Q | . | . | . | . | 1 | 0 | 0 | 0 | 0 | 1 | 1 | |
| | . | . | . | . | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| | . | . | . | . | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| | . | . | . | . | 0 | 1 | 1 | 1 | 1 | 0 | 0 | |

It shows external variables of a digital circuit, how many quantum primitives available in the structure, and which inputs are associated with each quantum-vector. The advantage of the table is absence of the vector of output numbers for each primitive, but it is still a need to have numbers of input variables for generating addresses, processing of which is time-consuming. Model for analyzing the circuit structure is simplified to calculating two addresses when forming the modeling vector $M_i = Q_i[M(X_i)]$ by eliminating the complex address of the primitive output when writing output states in the coordinates of the vector M.

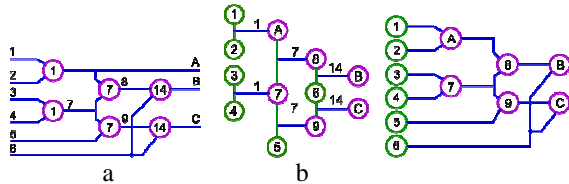


Fig. 1. Graph forms of quantum functionalities

The structure contains 12 lines (arcs), associated with the quantum functionalities (1 = 0001, 7=0111, 14=1110). It is similar to the traditional structural-functional model of a combinational circuit. Graph b looks like Sharshunov's register transfer model, which is reversed first structure. Here, blue horizontal arcs are identified with functionalities, and nodes – with the groups of input lines for functionalities, combined in register variables by green vertical arcs. States of these lines form a binary vector used as an address for calculating quantum state (logic element or more complicated functional one). The variables used in forming an address for a quantum of the functionality can be combined into a single node, with showing all the identifiers of lines, which form vector-address. The register graph of combinational circuit quanta is the ranked by levels of input signal formation, enabling conditions for concurrent handling of the elements of the same level and performability of Seidel iterations, which improve the performance of algorithms for fault-free simulating digital systems. Thus, the quantum-register graph of a digital circuit is discontinuous (by galvanic connections) flexible system of interconnected addressed primitives for creating functional structure of any complexity, especially on PLD, where all combinational primitives are implemented by memory elements (LUTs), which provides high operation performance and online

repairing the logic modules. The discontinuous quantum-register graph of Fig. 1 can be represented as quantum matrix $\mu = |\mu_{ij}|, i = \overline{1, p}; j = \overline{1, q}$ for parallel-to-serial processing logic primitives:

| | | | |
|------------|--|---|--|
| μ_{ij} | 1 | 2 | 3 |
| 1 | $\begin{matrix} 1 \\ 2 \end{matrix} \begin{matrix} 1 \\ 1 \end{matrix} \begin{matrix} A \\ A \end{matrix}$ | $\begin{matrix} A \\ 7 \end{matrix} \begin{matrix} 7 \\ 8 \end{matrix}$ | $\begin{matrix} 8 \\ 6 \end{matrix} \begin{matrix} 14 \\ B \end{matrix}$ |
| 2 | $\begin{matrix} 3 \\ 4 \end{matrix} \begin{matrix} 1 \\ 7 \end{matrix}$ | $\begin{matrix} 7 \\ 5 \end{matrix} \begin{matrix} 7 \\ 9 \end{matrix}$ | $\begin{matrix} 6 \\ 9 \end{matrix} \begin{matrix} 14 \\ C \end{matrix}$ |
| 3 | $\begin{matrix} X \\ X \end{matrix} \begin{matrix} 1 \\ X \end{matrix}$ | $\begin{matrix} X \\ X \end{matrix} \begin{matrix} 7 \\ X \end{matrix}$ | $\begin{matrix} X \\ X \end{matrix} \begin{matrix} 14 \\ X \end{matrix}$ |

which shows the interaction of quanta at three operation levels in accordance with the format (X–Q–Y) inputs-quant-output for each primitive: [(1,2–1–A), (3,4–1–7)], [(A,7–7–8), (7,5–7–9)], [(8,6–14–B), (6,9–14–C)]. To provide the correctness of the functionality, it is necessary to generate all input variables till a given moment. Therefore quantum-register graph is split into operation levels, where all primitives within a single level can be processed in parallel, and the levels – in succession. Quantum matrix due to its regular structure is focused on solving the following problems: 1) Repair of logical primitives in the operation due to readdressing faulty elements on spare primitives (line 3), just as is done in the memory matrix; 2) Index addressing each quantum of the matrix $\mu_{ij} \in \mu, \mu_{ij} = (X_{ij}, Q_{ij}, Y_{ij})$ for rapid repair of failed primitives (in the example we can replace three faulty primitives, one of each layer); 3) Providing high performance of combinational unit prototype based on quantum primitives implemented in PLD LUTs due to parallel processing of quantum primitives of a single layer; 4) Developing a matrix quantum multiprocessor, focused on synthesis of hardware prototypes of combinational units of large dimension to significantly speed up testing and verification of digital systems on chips like Aldec Hardware Embedded Simulator (HES); 5) Developing methods of analysis and synthesis of combinational circuits, focused to matrix realizing quantum structures of logic elements by means of their implementation in PLD memory elements; 6) Developing a code generator for implementing the quantum matrix of combinational circuit in the structure of PLD circuit primitives; 7) Designing a control automaton for functional processing and repairing the quantum matrix of combinational unit implemented in PLD structure.

The process model of control automaton functioning involves three items:

1. The initiation of the next input action for combinational unit.

2. Selection of the next layer (matrix column) with the number i for parallel processing quantum primitives Q to form output states at the address of an input word represented by the vector $M(X_{ij})$, where X_{ij} is vector of numbers of input variables for the quantum primitive Q_{ij} , M is modeling vector for all lines of combinational unit: $M(Y_{ij}) = Q_{ij}[M(X_{ij})]$, $j = \overline{1, q}$.

3. Incrementing the index column $i=i+1$ and going to the item 2 for processing the next layer of quantum primitives. After the analysis of all the columns of the matrix $i=P$ incrementing index of the next input pattern $t=t+1$ is performed, and subsequent going to the item 1. When reaching a finite number of input patterns $t=n_{max}$ the loop for processing test of the quantum matrix ends.

Thus, the basis of a process model for functioning of the combinational circuit represented in the form of the quantum matrix is the simplest and the only function of the read (write) of the binary information from the LUTs (memory elements) of PLD structure:

$M(Y) = Q[M(X)]$, which provide generating an arbitrarily complex computing products and/or processes.

Moreover, all of the computational processes in computer systems and networks in cyberspace, in the limit can be reduced to two operations read and write! Otherwise, all the technological and circuit constructs, on which hardware and software products are implemented, not be considered to synthesize new information services, which use only read-write operations as the basic procedures of the quanta, which are invariant to technology and constructs for the synthesis and analysis of objects, processes and phenomena in cyberspace. There is a new paradigm of the quantum computer based on a pair of operations "read" and "write" – Quantum–Read–Write Computer or QRW–Computer, which can be implemented on anything that is capable of storing 0 and 1 in a quantum to perform two mentioned actions. The priority of the writing-reading involves, of course, the ability of any carrier (quantum) to store information; otherwise there is nothing to apply these elementary functions. Any logic functions are implemented by writing and reading bits of the quantum-vector $Q = (q_1, q_2, \dots, q_i, \dots, q_n), q_i \in \{0,1\}$. But it becomes quite redundant theorem of Post that forms conditions in the form of mathematical functional basis of logic functions, necessary and/or sufficient complete to create any computing system, since the quantum vector

is a universal deterministic compact form of existence a simple or an arbitrarily complex functionality of (information) cyber-space. Write and read are technologically one procedure (transaction) of wired (wireless) connection when one component is a source of signal, and the second one is receiver. With respect to the first information carrier the transaction is regarded as reading, and to the second - writing. This pair can only exist together. Therefore, writing is impossible without reading and vice versa. Cyclical transaction $M \xleftarrow{Y_i} Q_i \xleftarrow{X_i} M$, (Fig. 2) represented by Read–Write operations $M(Y_i) = Q_i[M(X_i)]$ in QRW–structure (Fig. 2b), is determined by using the vector of component interconnections M that forms a soft (address focused) automaton model, the main component of which is quantum as part of a computer system:

$$\begin{cases} A = \langle M, Q, f, g, X, Y \rangle, \\ M(t+1) = f[X(t), Q(t), M(t)]; \\ Y(t) = g[X(t), Q(t), M(t)]; \\ M(Y_i) = Q_i[M(X_i)]. \end{cases}$$

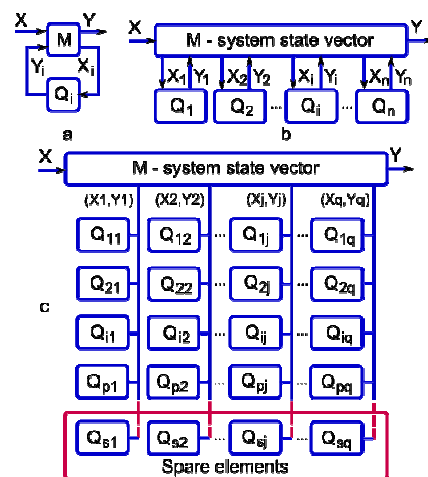


Fig. 2. Matrix structure of quantum primitives

These expressions corresponds to the classic definition of a Moore automaton, but the equality $M(Y_i) = Q_i[M(X_i)]$ defines the main procedure for analyzing addressable quantum components (vectors) of a digital system to form addressable coordinates of the state vector M . The last one is address computational responses of device primitives on input patterns obtained by concatenating the coordinates of the vector M , the addresses of which correspond to the number of input variables of the primitive. An automaton has an input register variable X , the vector of output signals Y , which being a subset of the variables of the vector M , can be excluded from

consideration. The address register variables Y_i, X_i of each primitive make it possible to form the state of the vector M by analysis (simulation) of the structure of quantum primitives Q .

Here (Fig. 2) the model of digital unit includes a modeling or system status vector that combines together and structure all the quantum primitives to achieve the functionalities described by specifications. At that the cycle of processing each element is the interaction between a pair $M-Q$ (Fig. 2), which implement the universal functionality $M(Y_i) = Q_i[M(X_i)]$ by means of two transactions writing-reading $M \leftarrow \overset{Y_i}{Q_i} \leftarrow \overset{X_i}{M}$. Processing all quantum elements on the input pattern X allows producing the vector M (System State Vector – SSV), which has, in addition to the internal variables, and output ones Y (Fig. 2b), necessary to control other components of computer structure. Speed of analysis (read-write) of vector (linear) structure of $n = p \times q$ primitives has the estimate: $\gamma = (R + W) \times n$. Strictly sequential processing ranked by numbers outputs, quantum primitives can be improved in the direction of performance.

To do this it is necessary to create a two-dimensional structure - the matrix of elements, ranked by levels of concurrency processing the groups of primitives, combined in columns (Fig. 2c). Performance of such structure, compared with linear one, is decreased in q -times that is becoming comparable to the combinational circuit, based on hard

$$\gamma = \frac{1}{q} (R + W) \times p$$

galvanic connections. But the main advantage of the matrix of soft component connections is the presence of the spare line in bottom for online repairing, which provides testability for any project, based on the combinational logic, due to the readdressing of any faulty quantum primitive on spare element. When synthesizing a two-dimensional structure it is desirable to set the primitives of the same type in one column that allows reducing hardware costs of spare elements.

An example of analysis of digital circuit on a test pattern is proposed below; the modeling vector and the quantum structure are as follows:

$$M = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & A & B & C \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

| Q_{ij} | 1 | | | 2 | | | 3 | | |
|----------|---|----------|--|---|----------|--|---|----------|--|
| 1 | 1 | 0001 A | | A | 0111 8 | | 8 | 1110 B | |
| | 2 | 0001 7 | | 7 | 0111 9 | | 6 | 1110 C | |
| 2 | 3 | 0001 7 | | 7 | 0111 9 | | 6 | 1110 C | |
| | 4 | 0001 7 | | 5 | 0111 9 | | 9 | 1110 C | |

The analysis of the digital structure is to fill the modeling vector for all coordinates: 1) Entry of input variables of the binary set 000111 into the modeling vector M for six coordinates. 2) Processing the primitive Q_{11} that has the input variables 1 and 2, and the output, marked by the symbol A . This address 00 is formed by concatenating the contents of the cells 1 and 2 of the vector M . Applying this address to the quantum-vector 0111 we can specify the content of the zero cell that is equal to zero; it is written in the vector M by the address A of the output variable of the quantum. 3) Repeating the analysis procedure described in item 2 to all quantum primitives, which enables fully define the coordinates of the modeling vector 000111001010 by the binary signals. The hardware implementation of the quantum structure of the digital devices, based on the use of memory elements, is shown in Fig. 3.

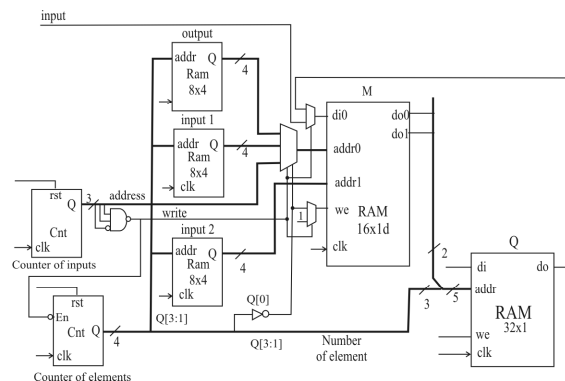


Fig. 3. Hardware realization of quantum structure of combinational circuit

The structure of the circuit contains the following variables and functional elements: input is designed for serial entering input values of vector; rst – general reset of the system (in this case for counters); clk – sync input; counter of inputs – counter for filling the input coordinates of the vector; counter of element – counter of processed primitive number, which provides two cycles for reading the input set of two coordinates of the vector; $Q[3:1]$ – bus for number of processed primitive; $Q[0]$ – variable for mode of reading input value from the vector M or writing the result to. Memory: Ram 8x4 output – stores the number of primitive output lines; Ram 8x4 input 1 and Ram 8x4 input 2 – store the numbers of primitive input lines. Ram 16x1d – dual-port memory for storing the modeling vector, where $addr0$ – address of the input 1 when the value 00 appears on control inputs of the multiplexer, address of writing result when the value 01 appears on control inputs of the multiplexer, address for initializing input data when the value 1X appears

on control inputs of the multiplexer; addr1 – address of input 2 for processed primitive; di0 – memory data input when processing primitive (MUX=1) or external input when initializing input data (MUX=0); we – permission of writing in the vector ; do0 – output, corresponding to the input addr0; do1 – output, corresponding to the input addr1. RAM 32x1 is designed for storing quantum-vectors defined functionalities of combinational circuit: di – data input that can be used to initialize (write) the structure of quanta; addr – [4:0]; addr[4:2] – element number, addr[1:0] – input set for a primitive.

The complexity of hardware implementation of the combinational circuit is 150 gates, which include 20 LUTs of Xilinx Spartan 3E element system. The speed of the operation or generation of the modeling vector is 180 ns.

Introduction of triadic QRW-structure for describing computational processes allows making more general conclusions: 1) The world has a duality of material and information integrity, and therefore deterministic reproducibility of objects, processes and phenomena. 2) Any material object is capable to store information, therefore, it can be used for reading and writing, so – for creating computer (management) system, even if it is specific. 3) Human is a biological computer with given program for functioning (life) of all his organs in time. 4) As any program, code (genome) of human functioning can be read and written, so - it can be adjusted. 4) Any objects in the world have their own programs of existence in time - information genomes. 5) Processes and phenomena in the world also have their own development programs, but the higher level of the hierarchy. 6) The universe also has its own genome – the information development program. 7) Of course, any program can be read, written, and then adjusted - this is an optimistic note of the information model of objects, processes and phenomena of the material world! Decoding the program, as well as disassembling the binary code is difficult, but possible. To do this, it is necessary to define a place - the code carrier and the encryption method for each object, process or phenomenon of nature. It can be assumed that the genome of the biological object is shaped like a multivalued quantum-vector

$$Q = (q_1, q_2, \dots, q_i, \dots, q_n), q_i \in \{a_1, a_2, \dots, a_j, \dots, a_k\}$$

The last one can be transformed into a binary matrix, where each symbol of the alphabet for describing quantum bits can be decompressed into a binary vector or code column. The multi-valuedness of the functionality is quite common in nature, convenient for perception by the human eye, but for the computer the

symbols of any alphabet until transformed into binary vectors.

3. Conclusion

Thus, the quantum structure of combination devices provides an opportunity to make the following transition: from the software simulation of digital systems for the hardware emulation of structures and processes, which are invariant with respect to implementation technologies. An analogue and prototype is Dr. Stanley Hyduke's hardware accelerator of simulation processes PRUS (Aldec Inc.), focused on reducing the time of the design and verification of digital systems on chips. But it is proposed to use processor for soft (address based) hardware simulating quantum structures for direct functional purpose as a computing product! This maintains the high speed operation of the device, supplemented by an opportunity of repairing in real time that is important for critical system.

The spatial parallelism of existing computers and point simultaneous multiple-valuedness are two ways of intelligent cyberspace development. Technological Singularity (Vernor Vinge <http://vingesingularity.blogspot.com/2008/05/dr-vernor-vinges-singularity-sponsored.html>) is the explosion in the understanding of the universe laws – it is almost vertical line in a short period of time in the development of humanity and cyberspace, thanks to the achievements of nano-, bio-technologies and cyber intelligence. Here it is assumed built-in human-computer integration, as well as the definition of intelligence as follows: second - self-training, and first of all, self-improvement of computers and cyberspace, when computers are capable to reproduce more sophisticated models and processes. One of the main conditions for achieving given point of human development is the creation of a fundamentally new computer (computational process), is invariant with respect to any point in space or a substance that can be structured and used in place of silicon. Otherwise, the computer can be based on anything that can have at least two controlled and monitorable states in time and/or space. Register or memory, as the basis for storing data and performing computational procedures, is a set of physical points or triggers, to which parallel operation distributed in space can be applied. At that increase in performance of digital devices today is realized only due to the expansion of space computational structure. Question - is it possible to combine the mentioned points of the space to a single one to perform parallel operations on a set of data, concentrated in one material point? Probably, just so the question is raised by practical scientists, who

anticipated the emergence of a quantum computer paradigm. There is no doubt that the future of the computer industry should be associated with multi-valuedness of physical space point as a primitive of data structures, which must be able to represent (store) the power set of states as the operand for the implementation of computational procedures. But here there is only one solution that deserves attention. Everything that is physically stable over time can have only one state at any given time, including digital discrete automata, devices and systems. The solution is clear – the dualism of wave and particle at the entire spectrum of electromagnetic radiation has the required properties of the spatial points: 1) each point of the space can be associated each time with a set of waves or particles (quanta) of known and unknown ranges to humanity; 2) This means the possibility of availability of a particle set of corresponding ranges in space point, which form the set of informational states of the point; 3) The instability or indeterminacy in time of processes and phenomena is the key to creating a fundamentally new computers, which can be called as quantum and electromagnetic, given the duality of electrostatics in respect to carrier (particle or wave); 4) At each stage of cyberspace development it is necessary to choose a suitable point in space or substance (gas, liquid, solid, plasma) that can be used to monitor and control its multi-valued states using existing technologies. Science fiction of writer Stanislaw Lem and predictions of scientist V.I. Vernadsky about the possibility of the existence of mind in the liquid (ocean Solaris) or gaseous medium (noosphere) today are close in time to the creation of a global artificial intelligence of cyberspace, which we need to get to 2050; 5) Sampling frequency spectrum at each point in space can serve as a basis for encoding the primitives (binary, multi-valued) or more complex associations, for example, the power set of states. Otherwise, 8-bit register having 256 states can be represented by one point in the space for further processing based on the monitoring and management of the respective quanta or range of frequencies. Projection of the register on the three-dimensional space degenerates to a point, but there is no determinism or monitoring ambiguity of a given point on the time axis. It is easy to imagine a register in the form of the parallelepiped, put vertically. If we look at it from above, we can see only one digit. To see all the bits, we need to throw light on this figure by spectrum of 8 frequencies (quanta). The multi-valuedness of the spectrum is determined by monitoring the frequency spectrum or quanta of different energy levels at a given point; 6) The principal difference which range of frequencies to be used for creating an electromagnetic (electrodynamic, quantum) computer does not exist! The only question

in the convenience of monitoring and control for particles or waves of this spectrum in a point in space or substance there exist. 7) The feasibility of a quantum computer, based on the use of the atomic structure is confirmed by the follows: its compactness, non-determined position of the electron in time and space, the presence of two directions for rotation, change of the orbit at external influence, low energy costs. The drawback is the lack of simple technologies today for monitoring and management of atomic primitives, which are need for creating deterministic computers; 8) If we assume that quanta exist in all ranges of continuous and infinite spectrum, the question is what range of frequencies will be mastered first to create new powerful and simple quantum computer.

4. References:

- [1] *Michael A. Nielsen & Isaac L. Chuang.* Quantum Computation and Quantum Information. Cambridge University Press. 2010. 676p.
- [2] *Hahanov V.I.* Digital System-on-Chip Design and Test. Kharkov: Novoye Slovo, 2009. 484 p.
- [3] *Hahanov V., Wajeb Gharibi, Litvinova E., Chumachenko S.* Information analysis infrastructure for diagnosis // Information an int. interdisciplinary journal. 2011. Japan. Vol.14. 7. .2419-2433.
- [4] *Hahanov V.I., Murad A.A., Litvinova E.I., Guz O.A., Hahanova I.V.* Quantum models for computing processes // Radioelectronics & Informatics. 2011. No 3. P.35-40.
- [5] *Bondarenko M.F., Hahanov V.I., Litvinova E.I.* Logical Associative Multiprocessor Structure. Automation and Remote Control. 2012. No 10. P. 71-92.
- [6] *Hahanov V.I.* Technical diagnosis of digital and microprocessor structures. K.: ICIO. 1995. 242 p.
- [7] *Vladimir Hahanov, Alexander Barkalov and Marian Adamsky.* Infrastructure intellectual property for SoC simulation and diagnosis service. Springer, 2011. . 289-330.
- [8] *Gorbatov V.A.* Fundamentals of Discrete Mathematics. .: Vysshaya Shkola. 1986. 311 p.
- [9] *Hahanov V., Litvinova E., Gharibi W., Murad Ali Abbas.* Qubit models for SoC Synthesis Parallel and cloud computing. USA. 2012. Vol.1. Iss 1. P. 16-20.
- [10] *Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas, Eshetie Abebech, Mandefro.* Qubit Model for solving the coverage problem // Proc. of IEEE East-West Design and Test Symposium. IEEE. USA. Kharkov. 14-17 September 2012. P.142 - 144.
- [11] *Chzen G., Menning E., Metz G.* Fault diagnosis of digital computing systems. .: Mir. 1972. 230 p.

Camera-ready was prepared in Kharkov National University of Radio Electronics
Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 11.09.2013. Format 60×84¹/₈.

Relative printer's sheets: 52. Circulation: 200 copies.

Published by SPD FL Stepanov V.V.

Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозиуму «Схід-Захід Проектування та Діагностування – 2013»
Макет підготовлено у Харківському національному університеті радіоелектроніки

Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова

Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 11.09.2013. Формат 60×84¹/₈.

Умов. друк. Арк. 52. Тираж: 200 прим.

Видано: СПД ФЛ Степанов В.В.

Вул. Ак. Павлова, 311, Харків, 61168, Україна