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11th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2013)

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The main target of the **East-West Design & Test Symposium** (EWDTS) is to exchange experiences between the scientists and technologies of the Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic systems. The symposium aims at attracting scientists especially from countries around the Black Sea, the Baltic states and Central Asia. We cordially invite you to participate and submit your contribution(s) to EWDTS'13 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level TPG
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Test
- Power Issues in Testing
- Real Time Embedded Systems

- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- Using UML for Embedded System Specification

CAD Session:

- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Rostov-on-Don, Russia, one of the biggest scientific and industrial center. Venue of EWDTS 2013 is Don State Technical University – the biggest dynamically developing centre of science, education and culture.

The symposium is organized by Kharkov National University of Radio Electronics and Science Academy of Applied Radio Electronics <http://anpre.org.ua/> in cooperation with Don State Technical University and Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Aldec, Synopsys, DataArt Lab, Tallinn Technical University, Aldec Inc.



CONTENTS

Impact of Process Variations on Read Failures in SRAMs Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.	15
Noise Effect Estimation and Reduction in High-Speed Voltage Controlled Oscillators Vazgen Melikyan, Abraham Balabanyan, Armen Durgaryan	19
A Probabilistic Approach for Counterexample Generation to Aid Design Debugging Payman Behnam, Hossein Sabaghian-Bidgoli, Bijan Alizadeh, Kamyar Mohajerani, Zainalabedin Navabi	23
Hybrid History-Based Test Overlapping to Reduce Test Application Time Vahid Janfaza, Payman Behnam, Mohammadreza Najafi, Bahjat Forouzandeh	28
A Mathematical Model for Estimating Acceptable Ratio of Test Patterns Vahid Janfaza, Paniz Foroutan, M. H. Haghbayan, Zain Navabi	32
Session based Core Test Scheduling for Minimizing the Testing Time of 3D SOC Surajit Roy, Payel Ghosh, Hafizur Rahaman, Chandan Giri	36
Functional Fault Model Definition for Bus Testing Elmira Karimi, Mohamad Hashem Haghbayan, Adele Maleki, Mahmoud Tabandeh	40
Evolution of von Neumann's Paradigm: Dependable and Green Computing Kharchenko V., Gorbenko A.	46
Quantum Technology for Analysis and Testing Computing Systems Wajeb Gharibi, Hahanov V.I., Anders Carlsson, Hahanova I.V., Filippenko I.V.	52
Diversity Assessment of Multi-Version NPP I&C Systems: NUREG7007 and CLB-BASED Techniques Kharchenko V., Duzhyi V., Sklyar V., Volkoviy A.	57
Features of Design, Implementation, and Characterization of On-Chip Antennas for Microwave Frequencies Aleksandr Timoshenko, Ksenia Lomovskaya, Mikhail Suslov	62
Design and Optimization of a Planar UWB Antenna Eng Gee Lim, Zhao Wang, Gerry Juans, Ka Lok Man, Nan Zhang, Vladimir Hahanov, Eugenia Litvinova, Svetlana Chumachenko, Mishchenko Alexander, Dementiev Sergey	67
Cloud Traffic Control System Hahanov V.I., Guz O.A., Ziarmand A.N., Ngene Christopher Umerah, Arefjev A.	72
Cloud Infrastructure for Car Service Litvinova E.I., Englesy I.P., Miz V.A., Shcherbin D.	77

Quantum Computing Approach for Shortest Route Finding Volodymyr Hahanov, Volodymyr Miz	85
Quantum Modeling and Repairing Digital Systems Baghdadi Ammar Awni Abbas, Hahanov V.I., Palanichamy Manikandan, Litvinova E.I., Dementiev S.	88
Quantum Models for Description of Digital Systems Hahanov V.I., Hahanova I.V., Litvinova E.I., Priymak A., Elena Fomina, Maksimov M., Tiecoura Yves, Malek Jehad Mohammad Jararweh	94
A Concept of Computing Based on Resources Development Analysis Drozd J., Drozd A., Zashcholkin K., Antonyuk V., Kuznetsov N., Kalinichenko V.	102
Blind Least Mean Square Criterion Algorithms for Communication Adaptive Arrays Victor I. Djigan	108
Estimation of structural complexity of IIR digital filters Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich	113
ASICPlacementAnalyzer: Software Tool for Data Analysis and Visualization of ASIC Placement Victor M. Kureichik, Maria V. Lisyak	118
Robust Watermarking System for Audio Identification Aleksandr V. Shishkin	122
Adaptive Artificial Boundary Conditions for Schrödinger Equation Taking into Account the First Order Dispersion of Laser Pulse and Diffraction of Laser Beam Vyacheslav A. Trofimov, Anton D. Denisov	125
Research of Methods to Create Informational Composition With the View of CAD of Intellectual Training Devices Knowledge-Based Signals of Cerebral Cortex Lavlinskiy V.V., Bibikov D.V., Burov R.B., Tabakov Y.G., Zolnikov K.V., Achkasov V.N.	129
Development of Upgraded Version of Finite Element Package ACELAN Arcady Soloviev, Pavel Oganesyan, Darya Krivorotova	133
Statistical Characteristics of Envelope Outliers Duration of non-Gaussian Information Processes Artyushenko V. M., Volovach V. I.	137
Optimizing Test Time for Core-Based 3-D Integrated Circuits by a Technique of Bi-partitioning Manjari Pradhan, Chandan Giri, Hafizur Rahamany, Debesh K. Das	141
Basic Concept of Linear Synthesis of Multi-Valued Digital Structures in Linear Spaces Chernov N.I., Yugai V.Ya., Prokopenko N.N., Butyrlagin N.V.	146

Boundary Problem for Nonlinear Elliptic Equations on Video Card Hasmik A. Osipyan	150
The High-Frequency Correction Circuit for Resistive Voltage Dividers with Capacitive Load Prokopenko N.N., Budyakov P.S., Butyrlagin N.V.	154
Simulation Features of Diffusion Doping Process by Means of Software Package of Synopsys Company Lagunovich N.L., Borzdov V.M., Turtsevich A.S.	158
Synthesis Circuit Correction for Speed Sensors of Physical Quantities and Current-Voltage Converters with Parasitic Capacitance Prokopenko N.N., Gaiduk A.R., Budyakov P.S., Butyrlagin N.V.	161
Microwave Selective RC Amplifiers with Control Parameters Prokopenko N.N., Krutchinsky S.G., Budyakov P.S.	165
Using Java Optimized Processor as an Intellectual Property core beside a RISC Processor in FPGA Mohammad Erfan Khazaee, Shima Hoseinzadeh	169
The automated testing system for optimizing and parallelizing program transformations Alymova E., Golozubov A., Morylev R., Pitinov A., Steinberg R.	175
Methodology to Design-For-Testability Automation for Mixed-Signal Integrated Circuits Sergey Mosin	178
Static Analysis of HDL Descriptions: Extracting Models for Verification Alexander Kamkin, Sergey Smolov, Igor Melnichenko	184
Fault-Injection Testing: FIT-Ability, Optimal Procedure and Tool for FPGA-Based Systems SIL Certification Kharchenko V., Sklyar V., Odarushchenko O., Ivasuyk A.	188
Query Optimization Based on Time Scheduling Approach Wajeb Gharibi, Ayman Mousa	193
Analysis of Error-Detection Possibilities of CED Circuits Based on Hamming and Berger Codes Valery Sapozhnikov, Vladimir Sapozhnikov, Dmitry Efanov, Anton Blyudov	200
Low-Power Design of Combinational CMOS Networks Dmitry Cheremisinov, Liudmila Cheremisinova	208
IGBT on SOI. Technology and Construction Investigation Ivan Lovshenko, Vladislav Nelayev, Sergey Shvedov, Vitaly Solodukha, Arkady Turtsevich	212
Generating Pipeline Integrated Circuits Using C2HDL Converter Denis Dubrov, Alexander Roshal	216

Data-Flow Multiprocessor with Deterministic Architecture Novatsky A. A., Glushko Je. V., Chemeris A.A., Pugachov O.S.	220
An Approach to Estimate the Error of Oscillator Time-Domain Analysis Vadim N. Biryukov, Alexandr M. Pilipenko	223
Sampling Theorem Applied to Data Interpolation Problem Gamlet S. Khanyan	227
A Few Test Generation Algorithms for web Applications from Imitational Model Anahit Asatryan	231
Design Automation Tool to Generate EDIF and VHDL Descriptions of Circuit by Extraction of FPGA Configuration Cheremisinov D.I.	235
Object-Oriented Approach to Software Implementation of Virtual Laboratory Workshop Gubsky D.S., Zemlyakov V.V., Mamay I.V., Sinyavsky G.P.	239
Schematic Design of HF and UHF Op-Amp for SiGe Technology Sergei G. Krutchinsky, Evgeniy A. Zhebrun, Victor A. Svizev	243
Improvement of Common-Mode Rejection Ratio in Symmetrical Differential Stages with Dynamic Load Sergei G. Krutchinsky, G.A. Svizev, Alexey E. Titov	247
Adaptation of the FPGA to Logic Failures Tyurin S.F., Grekov A.V., Gromov O.A.	251
Testable Combinational Circuit Design Based on Free ZDD-implementation of Irredundant SOP of Boolean Function Ostanin S.	257
On the Problem of Selection of Code with Summation for Combinational Circuit Test Organization Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov, Anton Blyudov	261
A 6-bit CMOS Inverter Based Pseudo-Flash ADC with Low Power Consumption Morozov D.V., Pilipko M.M., Piatak I.M.	267
Method of free C++ code migration between SoC level tests and stand-alone IP-Core UVM environments Fedor Putrya	271
A List Decoding Algorithm for Practical Reed-Solomon codes Sergey Egorov	275
On Stability of Optimization Process for Analog Circuits Markina T., Zemliak A.	279

Analysis of Converters with Heterogeneous Three-Pole Chain Structure Zhanna Sukhinets, Artur Gulin	283
The Modeling of Electromagnetic Fields Intensity in Urban Development Condition Anishin M.M., Zargano G. F., Zemlyakov V.V., Hondu A.A.	287
Estimation of Radio Wave Frequency Shift and Phase Incursion on the Basis of FPGA in the Retransmission Meter Vdovychenko I.I., Velychko D.A.	291
Delay Testable Sequential Circuit Designs Matrosova A., Mitrofanov E., Singh V.	293
Supervision in Airborne Systems with Antenna Array Klochko V.K., Nguyen Tr.T.	297
Self-timed Functionally Complete Tolerant Element with Different Supply Voltage Kamenskih A.N., Tyurin S.F.	300
SPICE Model Parameters Extraction Taking into Account the Ionizing Radiation Effects Konstantin Petrosyants, Maxim Kozhukhov	304
Analysis and Simulation of Temperature-Current Rise in Modern PCB Traces Petrosyants K.O., Kortunov A.V., Kharitonov I. A., Popov A.A., Gomanilova N.B., Rjabov N.N.	308
Coupled TCAD-SPICE Simulation of Parasitic BJT Effect on SOI CMOS SRAM SEU Petrosyants K.O., Kharitonov I.A., Popov D.A.	312
Digital Converter of Frequency Deviation Based on Three Frequency Generator Shakurskiy M.V., Shakurskiy V.K., Ivanov V.V.	316
Comparative Analysis of Coding Effectiveness in Telecommunication Systems with ARQ Anfalov K. V., Volovach V. I.	320
Multiagent Bionic Algorithm for Optimization of Circuitry Solutions Andrey Bereza, Andrey Strogenko, Luis Blanco	324
Nonlinear Filtering of Pseudonoise Signals Using High-Order Markov Chain Model Dmitriy Prozorov, Anton Chistyakov	328
Representation of Solutions in Genetic Placement Algorithms Zaporozhets D.U., Zaruba D.V., Kureichik V.V.	332
Digital Adaptive System of Linearization Power Amplifier Natalya V. Gudkova, Vladimir M. Chuykov, Ksenya V. Besklubova	336
A Parallel Shrinking Algorithm for Connected Component Labeling of Text Image Sergey S. Zavalishin, Yury S. Bekhtin	340

Automated Measurement of Digital Video Cameras Exposure Time Budilov V.N., Volovach V.I., Shakurskiy M.V., Eliseeva S.V.	344
Hybrid Pareto-Evolutionary Algorithm for Solving Mathematical Models of High Dimensional Electronic Circuits (HPEA) Vadim Beglyarov, Andrey Bereza, Luis Blanco	348
Finite State Machine Synthesis for Evolutionary Hardware Andrey Bereza, Maksim Lyashov, Luis Blanco	352
Increasing Efficiency of Information Transmission with Interference Influence by the Use of Multi-parameter Adaptation Nechaev Y.B., Kashenko G.A., Plaksenko O.A.	356
Analysis of Ferromagnetic Structures Fast-Acting Under the Influence of External Magnetic Fields of Various Intensity Alexander Shein, Gennady Sinyavsky, Larissa Cherkesova, George Shalamov	360
Modeling Using Multivariate Hybrid Regression Analysis Method Danilov A. A., Ordinartseva N. P.	365
Analog Input Section of the Ultrafast ADCs Prokopenko N.N., Serebryakov A.I., Butyrlagin N.V., Pakhomov I.V.	368
A Recursive Least Squares Solution to AOA Based Passive Source Localization Hejazi F., Azimi K., Nayebi M.M.	371
Identification Discrete Fractional Order Linear Dynamic Systems with Errors-in-Variables Ivanov D.V.	374
Self-Calibration Method for Capacitor Mismatch Elimination Vazgen Melikyan, Harutyun Stepanyan, Ani Aleksanyan, Ani Harutyunyan, Armen Durgaryan	378
Whitespace Calculation in 3D IC Ara Gevorgyan	382
Low-Voltage Compatible Linear Voltage Ramp Generator for Zero-Crossing-Based Integrators Melikyan Vazgen Sh., Dingchyan Hayk H., Sahakyan Arthur S., Vardan Grigoryants P., Safaryan Karo H.	386
High Accuracy Equalization Method for Receiver Active Equalizer Melikyan Vazgen Sh., Sahakyan Arthur S., Safaryan Karo H., Dingchyan Hayk H.	390
Implementation of Parallel Dataflow Computational Model on Cluster Supercomputers Levchenko N.N., Okunev A.S., Klimov Ark.V., Zmejov D.N.	394

Semiconductor Electronic Parts Testing Efficiency Martynov Oleg, Ogurtsov Alexander, Sashov Alexander	397
An Approach to Accelerated Life Tests of Electronic Components Koulibaba Andrey, Krasnov Mikhail, Prischepova Svetlana	401
Next Generation Visual Programming Technology Velbitskiy I.V.	404
Efficient Calculation of Cyclic Convolution by Means of Fast Fourier Transform in a Finite Field Amerbaev V.M., Solovyev R. A., Stempkovskiy A.L., Telpukhov D.V.	411
High-level Test Program Generation Strategies for Processors Shima Hoseinzadeh, Mohammad Hashem Haghbayan	415
Fault Tolerance of the Distributed Structure of Object Controllers for Automation of Transport Sergey Rodzin, Lada Rodzina	419
Effective planning of calculations on the PDCS "Buran" Architecture Levchenko N.N., Okunev A.S., Zmejeyev D.N., Klimov A.V.	423
Ways to Ensure the Stability of Circuits to Single Events in the Design of Radiation-Resistant Circuits Smerek V.A., Utkin D.M., Zolnikov V.K.	426
Smart Road Infrastructure Artur Ziarmand	430
Testing of Transport System Management Strategy Sergey Lupin, Than Shein, Kyaw Kyaw Lin, Anastasia Davydova	435
The Bioinspired Algorithm of Electronic Computing Equipment (ECE) Schemes Elements Placement Kureichik V.V., Kureichik VI.VI.	439
The Hardware Architecture and Device for Accurate Time Signal Processing Jiř í Dost' al, Vladim ír Smotlacha	443
Management Methods of Computational Processes in the PDCS "Buran" Levchenko N.N., Okunev A.S., Zmejeyev D.N., Klimov A.V.	446
Service-Oriented Computing (SOC) in a Cloud Computing Environment Petrenko A.I.	449
The Methodology of Two-Stage Masking Images in Information and Telecommunications Systems Barannik V. V., Vlasov A. V., Shiryayev A. V.	453

Perforated with Technology of Description Massives Differential Representation in the Delivery Compressed Images Systems Kulitsa O.S., Lekakh A.A., Akimov R.I.	457
Method of Coding Bitmap Transformant to Improve Image Compression while Maintaining a Predetermined Quality Image to be Transmitted in Infocommunication Real Time Systems Krasnorutskiy A.A., Hahanova A.V., Demedetskiy A.O.	461
Method Structure Coding of Aperture Elements for Image in Infocommunication Systems Barannik V.V., Dodukh A.N., Krivonos V.N.	465
Domain-Driven Design the Database Structure in Terms of Metamodel of Object System Pavel P. Oleynik	469
An Approach to the Fuzzy Logic Modeling of Digital Devices Dmitriy Speranskiy	473
Reconfiguration of FPGAs Using Genetic Algorithms Gorodilov A. Yu., Tyurin S. F.	477
Algorithm for Automated Custom Network-on-Chip Topologies Design Bykov S. O.	481
Choice of Variants of Radio-Frequency Identification Systems on Set of Quality Parameters Bagdasaryan A.S., Kashenko A.G., Kashenko G.A., Semenov R.V.	484
Green logic FPGA Tyurin Sergey, Kharchenko Vyacheslav, Prokhorov Andrey	489
Restoration missing values of discrete signal during the calibration ADC with build-in interpolation Koroleva Ksenia, Gritsutenko Stanislav	492
Keynotes Speeches and Invited Reports	496
AUTHORS INDEX	501

Quantum Modeling and Repairing Digital Systems

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Abstract

The results of studies concerning the models and methods of quantum diagnosis of digital systems, qubit fault simulation and analysis of fault-free behavior, as well as repair of faulty primitives, are presented.

1. Qubit fault models

A fault is defined as each individual discrepancy of a product to specification, but fault model should never lead out the product beyond the functionality limits [1,2,8]. Therefore fault (fault model – failure) is time fixed part of the functionality that is tied to a physical component. The constant line fault is fixed transition 0-0 at two adjacent cycles. It makes no sense to consider it as a further extension to other cycles, because according to the automaton model they are all described by means of two adjacent time frames. By extending this two-frame concept to automaton variables we can introduce the full set of fault transitions: 00, 01, 10, 11. Indeed, if we consider the automatic variables, for instance for the register, it is necessary to generate test patterns for verifying the above transitions. Based on the concept of the fault, it follows that the total number of states of functionality also forms a complete set of faults, with the only difference being that the specific fault is always a complement to test signal that detects a fault [2]:

$$\left\{ \begin{array}{l} F \oplus T \oplus L = \emptyset, \\ T \oplus F = L; \\ T \oplus L = F; \\ F \oplus L = T. \end{array} \right.$$

Here it is shown that the interaction of the functionality test and faults is always convoluted to empty or null space, which allows determining any fault by non-empty interaction between the test and

functionality. But because the test is a derivative of the function, then it follows that a fault (its model) is a derivative of the function or its spatio-temporal frame. In order to such triad interaction was possible it is necessary to lead the models of three components to a single type or view (matrix or table, Boolean equations, structure). One of the variant of replacing the traditional Roth symbols [8], aimed on searching active paths in the circuit, can be vector representation of spatio-temporal frames of a model, test, and fault in Boolean discrete measurement.

Qubit data model carries out “transformation” of the information quantum from the set-theoretic symbol in the logical bit-vector with unitary encoding primitives. This practically means the replacement of set-theoretic operations by vector-logic ones, which has a positive impact on performance, but there is a subjective loss in the visualization of information for a human who is not able to read the letters (texts), presented in the form of binary vectors. Thus, any closed multi-valued set-theoretic alphabet is written by a set of binary vectors, where the transformation is determined by the relation:

$n = \log_2(B = 2^n)$, where B is the Boolean (power set), n – the number of bits or primitives (power of the universe), which form the power set. Otherwise, qubit is a vector-logical equivalent of any closed set-theoretic alphabet. This means that qubit is a vector with the number of bits (at least two) equal to the number of primitive symbols, which is capable to represent the power set of states by means of its binary digits. Single-bit qubit does not make sense, since it has no conformance in the set-theoretic space.

Example of a four-digit qubit is presented below. Suppose we have a two-stroke alphabet for description of automatic variables, which is the power set on the universe of the four primitives:

$B^*(Y) = \{Q=(1000), E=(0100), H=(0010), J=(0001), O=\{Q,H\}=(1010), I=\{E,J\}=(0101), A=\{Q,E\}=(1100), B=\{H,J\}=(0011), S=\{Q,J\}=(1001), P=\{E,H\}=(0110),$

$C=\{E,H,J\}=(1110)$, $F=\{Q,H,J\}=(1011)$, $L=\{Q,E,J\}=(1101)$, $V=\{Q,E,H\}=(1110)$, $Y=\{Q,E,H,J\}=(1111)$, $U=(0000)$.

Operations on the symbols of the set-theoretic alphabet are reduced to logical instructions and, or, not, xor, which form a functionally complete basis according to Post's theorem [3]. For example, the following logical transformations of some set-theoretic operations are presented below:

$$\begin{aligned} Q \cup E &= 1000 \vee 0100 = 1100 = A; \\ S \cap V &= 1001 \wedge 1110 = 1000 = Q; \\ \tilde{B} &= \overline{0011} = 1100 = A; \\ F \Delta P &= 1011 \oplus 0110 = 1101 = Y; \\ H \Delta J &= 0010 \oplus 0001 = 0011 = B; \\ F \Delta Y &= 1011 \oplus 1111 = 0100 = Y; \\ F \Delta F &= 1011 \oplus 1011 = 0000 = U(\emptyset); \end{aligned}$$

The quantum interpretation of the power set of four primitives (binary positional codes: 00, 01, 10, 11) is presented below:

00	0	0	0	0	0	0	0	1	1	1	1	1	1	1
01	0	0	0	0	1	1	1	1	0	0	0	0	1	1
10	0	0	1	1	0	0	1	1	0	0	1	1	0	0
11	0	1	0	1	0	1	0	1	0	1	0	1	0	1

It describes 16 different functions of two variables. At the same time the last table can be represented in the form of codes (vectors) of multi-valued alphabet symbols, which are easy to use to address the problems of synthesis and analysis of Boolean functions:

Q	0	0	0	0	0	0	0	1	1	1	1	1	1	1
E	0	0	0	0	1	1	1	1	0	0	0	0	1	1
H	0	0	1	1	0	0	1	1	0	0	1	1	0	0
J	0	1	0	1	0	1	0	1	0	1	0	1	0	1
\emptyset	J	H	B	E	I	P	C	Q	S	O	F	A	L	V

Thus, a qubit composed of four bits can be used for describing 16 states of the spatio-temporal frame of functionalities; at that it uses vector logic operations to address the problems of synthesis and analysis.

2. Quantum modeling digital systems

For example, to describe a digital circuit shown in Fig. 1 we must have a structure of interconnected elements, and cubic coverage of logic AND-NOT element.

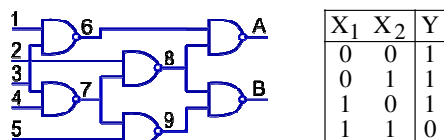


Fig. 1. Fragment of digital circuit

The coverage may be modified taking into account unitary encoding input vectors. As a consequence for any coverage of the functional single input primitive there always exist only two cubes. They show not only all the solutions, but also the inverse of the signals at the outputs, which is interesting from the point of activation of all logical paths in the circuit structure. For example, in the following qubit gate coverage in order to change the state of the output it is necessary to create a pair of consecutive conditions on inputs, where the first three vectors (addresses) have to be in the first cycle, fourth vector that is forming by two input variables - in the second one:

$$\begin{array}{|c|c|} \hline 00 & 1 \\ \hline 01 & 1 \\ \hline 10 & 1 \\ \hline 11 & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline Q & 1 \\ \hline E & 1 \\ \hline H & 1 \\ \hline J & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline V & 1 \\ \hline J & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline 1110 & 1 \\ \hline 0001 & 0 \\ \hline \end{array} \rightarrow \begin{array}{|c|c|c|c|} \hline 1 & 1 & 1 & 0 \\ \hline \end{array}$$

To simulate the fault-free behavior it is sufficient to have only one cube (zero or unit), because the second one is always complement of the first. Consequently, if we are focused, for example, on unit cube that forms 1 on the output we can remove the bit of primitive output state, which reduces the dimension of the cube or primitive model up to the number of element addresses, where bit with address number I identifies the capability of an address, consisting of the values of the input variables, to form unit state of primitive output.

Qubit or quantum coverage of single output primitive is two cubes the dimension of which is equal to the power of two of the number of input variables, where unit coordinate value defines the use of bit address in forming the corresponding (0,1) state of primitive output. Quantum models of primitives require the creation of a new theory of modeling, direct and inverse implication, test synthesis, fault simulation, fault detection. Here, the basic procedures are associated with the manipulation by addresses, implicitly represented in the coordinates of two cubes of quantum (qubit) coverage hereafter named Q-coverage.

$$\begin{array}{|c|c|} \hline 00 & 0 \\ \hline 01 & 0 \\ \hline 10 & 1 \\ \hline 11 & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline Q & 0 \\ \hline E & 0 \\ \hline H & 1 \\ \hline J & 0 \\ \hline \end{array} = \begin{array}{|c|c|} \hline F & 0 \\ \hline H & 1 \\ \hline \end{array} = \begin{array}{|c|c|} \hline 1101 & 0 \\ \hline 0010 & 1 \\ \hline \end{array}$$

Model for analyzing digital system based on the use of qubit data structures and information quanta can be described by four components:

$$\begin{aligned} F &= \langle L, M, X, Q \rangle, \\ L &= (L_1, L_2, \dots, L_j, \dots, L_n); \\ M &= (M_1, M_2, \dots, M_j, \dots, M_n); \end{aligned}$$

$$X = (X_{x+1}, X_{x+2}, \dots, X_{x+i}, \dots, X_{x+n});$$

$$Q = (Q_{x+1}, Q_{x+2}, \dots, Q_{x+i}, \dots, Q_{x+n}).$$

The vector of identifiers for circuit potential lines of digital system, state modeling vector for all circuit lines, ordered set of input variable vectors for each circuit primitive associated to the output numbers, a set of vectors – quantum primitives coverages, strictly associated to the output numbers and the input variables of primitives, n is the number of lines in the circuit, x – the number of input variables are represented here.

An example of qubit model of digital device $F = \langle L, M, X, Q \rangle$ (Fig. 1) is presented below – two variants of circuit description tables for analyzing fault-free behavior (fault free simulation):

L	1	2	3	4	5	6	7	8	9	A	B	L	1	2	3	4	5	6	7	8	9	A	B
Q	1	1	1	1	1	1	M	1	1	1	1	0	0	1	1	1	0	
	1	1	1	1	1	1	X	13	34	27	75	68	89	
	1	1	1	1	1	1	Q	1	1	1	1	1	1	
	0	0	0	0	0	0		1	1	1	1	1	1	
X	13	34	27	75	68	89		1	1	1	1	1	1	
M	1	1	1	1	1	0	0	1	1	1	0		0	0	0	0	0	0	

The method of quantum fault-free simulation is reduced to the definition of address generated by binary states of input variables for each primitive of digital circuit. If the variables create non-binary address, in this case, there is possibility of forming non-binary output state of the primitive, which is defined in the ternary alphabet by symbol X. The output states are formed by consistent modeling, based on simple iterations or Seidel iterations [3,4]. In the second case a preprocessor procedure for ranking lines and circuit primitives is necessary, which considerably reduces the number of passes on the circuit primitives to achieve convergence when the equality of the states of all circuit lines in two adjacent iterations is fixed. In addition, ranking of primitives on the levels of forming outputs allows significantly improving the performance of simulation due to parallel processing functional elements of one level. For example, for the circuit shown in Fig. 1, we can handle concurrently the elements with the numbers 6, 7, and then – 8, 9 and beyond - A, B. In the first case, when simple iterations are used ranking is not required, but cost for simplicity of simulation algorithm is significantly greater number of iterative passes through the circuit primitives to achieve the convergence criterion.

For the synthesis of quasi-optimal data structures of a combinational device it is necessary to use the following rules:

1) To simulate by using Seidel's method, the ranked circuit of a digital device on the structural depth must

have the same type of primitives as possible in each level (layer) of operation.

2) It is desirable to have the same number of primitives at each level that means - synthesis of digital device has to be focused on creation a rectangular or matrix like structure of similar logical elements.

3) Implementation of the combinational primitives provides for using addressable memory elements existing in programmable logic devices (FPGA, CPLD), widely used for prototyping.

4) Providing spare primitives for each level of the combinational device for online repairing - one spare element for each type of component that is used in the level.

5) Hardware cost for implementing high-performance combinational device should be determined by the sum of all the primitives associated to the levels of combinational device, extended by set of spares, one for each layer (assuming the existence of the same primitives in each layer):

$$Q = \sum_{i=1, n}^{\overline{j=1, m}} P_{ij} + n.$$

6) Implementation of the combinational device based on minimizing hardware cost is determined by the sum of all types of primitives, which are invariant to the levels of combinational device and extended by set of spares, one for each type:

$$Q = \sum_{i=1}^m P_i + m.$$

7) Processing the matrix of the combinational elements by using the processor line of primitives, the number of which is equal to the power of maximum level or layer in rectangular structure, which provides the possibility for parallel processing all primitives in each element level in order to improve the performance of the combinational prototype, implemented in the PLD.

3. Repair of combinational units

The few works devoted to repair of logic circuits [5-7] describe the two ideas. The first one provides for reconfiguring the structure of logical components off-line, which provides the possibility of replacing each of the faulty primitives. The second one creates the conditions for replacement of faulty components through the use of spare components and extension of multiplexers for readdressing failed primitives.

Qubit data structures is modified by way of adding a row of primitive types

$$F = \langle L, M, X, P, Q \rangle, P = (P_1, P_2, \dots, P_1, \dots, P_m),$$

used when synthesizing the digital system, if necessary to repair the system during operation by using spare primitives, which like basic elements are implemented on the basis of memory.

Fig. 2 illustrates an example of a circuit structure, composed from addressable and three spare components. Data structures corresponding to the circuit with three additional elements are presented below:

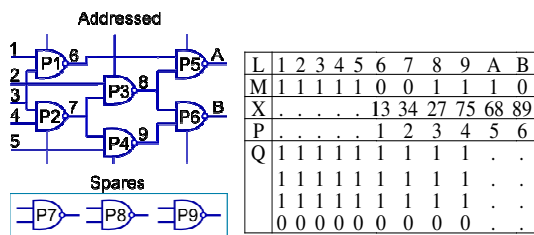


Fig. 2. An example of a circuit structure of addressable and spare elements

The table uses the numbers of structural primitives, which gives the opportunity to replace any failed element by spare by changing the address number in the line of primitives P. Repair elements in this table begin with the number 7.

The following table shows the line of logical elements, as well as the addresses of types for these primitives, marked with numbers:

L	1	2	3	4	5	6	7	8	9	A	B
M	1	1	1	1	1	0	0	1	1	1	0
X	13	34	27	75	68	89
P	1	1	1	1	1	1
Q	1	1	1	1
	1	1	1	1
	1	1	1	1
	0	0	0	0

This data structure is focused on software simulation, and spare primitives begin with the number 2. If it is possible to reprogram the logic in the memory element with the same number of input variables, then the procedure should be performed after fixing the faulty element, where it is known - which element in the structure refused and the type of it. This repair procedure is focused to PLD-implementation of digital systems. If the qubit models of circuits have no spare primitives, the corresponding tables will be as follows:

L	1	2	3	4	5	6	7	8	9	A	B
M	1	1	1	1	1	0	0	1	1	1	0
X	13	34	27	75	68	89
P	1	1	1	1	1	1
Q	1
	1
	1
	0

L	1	2	3	4	5	6	7	8	9	A	B
M	1	1	1	1	1	0	0	1	1	1	0
X	13	34	27	75	68	89
P	1	2	3	4	5	6
Q	1	1	1	1	1
	1	1	1	1	1
	1	1	1	1	1
	0	0	0	0	0

Thus, quantum data structures are focused on compact description of digital product functionality by means of qubit vectors, speedup simulation procedures by using addresses of output states of primitives, and repairing the logic gates due to their implementation in PLD memory elements.

Processing circuit on a chip is reduced to determine the address, compiled from binary bits of the simulation vector, which determines a logical function. Each primitive has processing loop that contains three procedures:

1) Address reading the numbers of input variables from the corresponding column of the matrix X to form the address of the states of the input variable for the simulation vector: $A = X_{ij}, i = 1, n; j = 1, s_p - 1$;

2) Generating the address (binary code) to compute the logic function by concatenating the corresponding states of the input variables in the simulation vector $A = M(X_{ij}) * M(X_{ir})$;

3) Saving the result of executing the logical function (the status of the output) to the corresponding bit of the simulation vector $M(X_{is_p}) = P[M(X_{ij}) * M(X_{ir})]$

The processing of all circuit primitives in this case is strongly consistent that result in considerable slowdown of procedure for forming states of output variables. However, the decrease in performance can be considered as payment for embedded and autonomous repairing the functionality of digital structure, which is one of the stages of functioning SoC infrastructure IP, shown in Fig. 5.

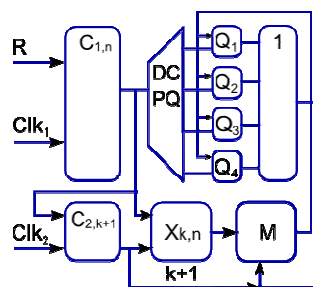


Fig. 5. Operational structure of combinational circuit

Combinational circuit becomes operating unit, where there are operating and control automata. Replaceable components in the operating automaton are primitive types - functional elements or structural primitives.

Operational unit for implementation of element-addressable combinational circuits contains the following components: counter for processing the

current primitive C_1 ; memory for storing the types of primitives, corresponding to the structural elements P ; counter for reading the numbers of input and output variables of the current primitive C_2 ; decoder of primitive types DC ; memory for storing the simulation vector M ; matrix memory for storing the numbers of inputs-outputs of the structural primitives X ; memory line, realizing the functional primitives $P(Q)$; register for generating the input address word for the processed primitive RG ; logic element Or for switching results of processing functional primitives.

Flow-chart of control algorithm for simulating the structure of combinational circuit is shown in Fig. 3 and includes the following items:

1. Initialization (forming) of all components of the circuit structure (numbers and types of elements, connection lines for inputs and outputs of logic gates):

$$P = (P_1, P_2, \dots, P_1, \dots, P_n); \quad Q = (Q_1, Q_2, \dots, Q_j, \dots, Q_m);$$

$$X = [X_{pq}]; p = \overline{1, n}; q = \overline{1, s_p}.$$

2. Initialization of parameter of the processed primitive and the number of input pattern $i=0, t=0$ for its simulating in the binary alphabet $M_r = \{0,1\}$.

3. Incrementing the index of the primitive, the numbers of test and initialization of the input test pattern:

$$i = i + 1, t = t + 1, M(X) = T_t(X), |T_t(X)| = \eta.$$

4. Concatenation (#) of word bits for generating the input stimulus $\#_{j=1}^k M(X_{ij})$ for logic element P_1 (of the

type Q_i); performing the procedure for determining the state of its output and subsequent writing into the correspondent coordinate of the simulation vector $M(X_{k+1})$:

$$M(X_{k+1}) = \{P_i, Q_i\} \#_{j=1}^k M(X_{ij}).$$

5. Iteration of items 3 and 4 in order to obtain the states of the outputs for all the logic elements to satisfy the condition: $i=n$.

6. Iteration of items 2–4 for simulating all input test patterns to the equality: $t=\eta$, where η is length of the test.

7. The end of the simulation of digital device.

The operating and control automata are represented here; they are focused on consistent processing combinational primitives that allow realizing the readdressing procedure for primitives in case of failure of one of them. It is easy to develop similar automata for parallel processing layers of ranged circuit

primitives that maximum approaches the performance of the device to realization in PLD chips.

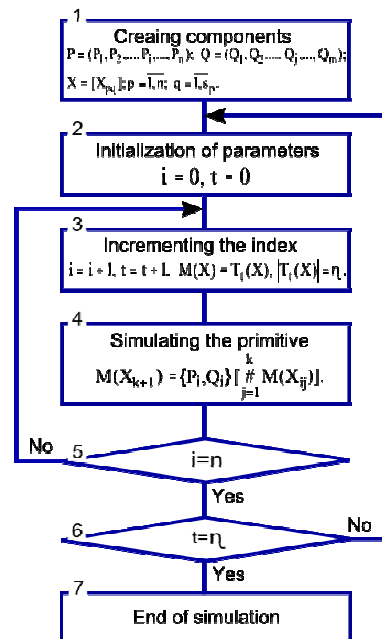


Fig. 3. Flow-chart of control algorithm for simulation

4. Conclusion

A quantum method for fault-free simulation of digital devices with online repairing components of digital systems is presented; it is characterized by significantly better performance due to the address processing functional primitives, defined by qubit coverage.

Case-studies of repairing faulty modules based on the addressable logical primitives are considered.

Directions for future research:

1. Using the or-operation for the analysis of fault detection table in order to detect multiple faults.

2. Research and application of Hasse processor to detect single and/or multiple faults by fault detection table and reduction of the procedure to searching for optimal coverage.

3. Modeling fault-free behavior of the sequential circuits based on qubit data structures of digital devices.

4. Synthesis of qubit models of functional primitives and digital systems, based on the use of quantum primitives, as well as the decomposition (analysis) of functionality quanta on qubit primitive models.

5. Simulation of transition faults of automaton variables by modifying the deductive algorithm.

6. Development of encoders and decoders for DSP-processors based on the use of qubit data structures, which allow increasing the performance of coding tools and compactness of data representation.

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