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NEW FEATURES OF DEDUCTIVE FAULT SIMULATION

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This paper describes the Fast Backtraced Deductive-Parallel Fault Simulation method. This method is oriented on processing large digital devices that are described in RTL or gate level format. Also in article are described data structures and algorithms for implementation of the method in the automated design for test (DFT) systems.

1. Introduction

The work is conditioned by importance of dramatic improve of test generation speed for complex digital devices implemented in ASICs. Well known automatic test generation and fault simulation systems from such vendors as Cadence, Mentor Graphics, Synopsis, Logic Vision, are oriented on processing of whole logic blocks (chips). But maximum size of such logic blocks is about hundred of thousands of equivalent gates and the processing time is several hours and more. It is not acceptable for today multi-million gates digital designs.

Therefore, it is needed to develop new approach to the problem, that allows to speed-up digital system analysis and test generation. To solve this problem the new technology has been used, and the fast fault simulation method have been developed.

Unit under test is a digital system, which can be implemented in ASIC. The system is described on HDL. *Objectives* are to develop high performance stuck-at-fault simulation method for evaluation of quality of generated tests for digital systems. Method should satisfy designers of multi-million gates devices.

Research problems: 1. Create general deductive-parallel analysis model of digital circuit. 2. To develop internal model and data structures for digital device analysis. 3. Develop algorithms for structure-functional analysis of digital systems. In term of this task should be defined the set of reconverging fan-outs (RF) and tree-like structures (TS). 4 To develop fault simulation method. It should differently process RF and TS. 5. Simulation process. The model of the circuit is reconfigured during the fault analysis and backtracing to reduce the time of quality estimation of tests.

The methods of fault analysis speed-up [1-3], deductive model of faults propagation [4, 5], parallel method of processing of lists of faults [4, 6], backtracing algorithm [7] are forming the base of BDP method (Backtraced Deductive-Parallel).

2. General model of deductive-parallel fault analysis

The model of deductive-parallel synchronous faults analysis of discrete objects allows discovering all faults that can be detected by test-vector during only one iteration of processing the circuit. Such model is based on solving the following equation [3, 4]:

$$L = T \oplus F, \qquad (1)$$

Where,

$F = (F_{m+1}, F_{m+2}, ..., F_i, ...F_n)(i = \overline{m+1, n})$ – is a set of functions that describe fault-free behaviour of the device; m – number of inputs;

$Y_i = F_i(X_{i1}, ..., X_{ij}, ..., X_{in_i})$ – output line, which is defined by function F_i on test-vector T_t. Here X_{ij} – is the j-variable of element i.

Test $T = (T_1, T_2, ..., T_t, ..., T_k)$ is a set of binary vectors, which are determined on the set of input, output and internal lines during fault-free simulation.

$$T = [T_{ti}] = \begin{bmatrix} T_{11}, T_{12}, ..., T_{1i}, ..., T_{1n} \\ ....\ ....\ ....\ ... \\ T_{t1}, T_{t2}, ..., T_{ti}, ..., T_{tn} \\ ....\ ....\ ....\ ... \\ T_{k1}, T_{k2}, ..., T_{ki}, ..., T_{kn} \end{bmatrix}, \qquad (2)$$

The internal and output coordinates of matrix are defined by function

$T_{ti} = Y_i = F_i(X_{i1}, ..., X_{ij}, ..., X_{in_i})$ on test-vector T_t; $L = (L_1, L_2, ..., L_t, ..., L_k)$ is a set of deductive functions (DF) or models, defined according to Eq. (1), where

$$L_t = (L_{t1}, L_{t2}, ..., L_{ti}, ..., L_{tn});$$

$$L_{ti} = T_t \oplus F_i \quad (3)$$

- is a deductive function of parallel fault simulation on test T_t. This function relates to fault-free element F_i and allows detecting the list of faults, which can be propagated to the output of the element F_i [8].

The synchronism of the model is defined by condition: $\Delta t = (t_{j+1} - t_j) >> \tau >> \tau_i$. The time between two neighbor input patterns $(t_{j+1} - t_j)$ is much greater than time-out delay τ of the circuit and of the element τ_i. Hence time can be considered as incidental parameter and excluded from consideration [8].

In general case, when function of the system is represented as truth table, by applying formula (1) fault propagation table for defined test-vector T_t can be obtained. The fault simulation deductive function can be also obtained by using this table. For example (the first component is test; the second and the third one are truth and fault propagation tables correspondingly):

X_1	X_2	Y_1
0	1	0

$\oplus$

X_1	X_2	Y_1
0	0	0
0	1	0
1	0	1
1	1	1

$=$

X_1	X_2	L_1
0	1	0
0	0	0
1	1	1
1	0	1

$L_1 = X_1 X_2 \vee X_1 \overline{X}_2;$

X_1	X_2	Y_2
1	1	1

$\oplus$

X_1	X_2	Y_2
0	0	0
0	1	0
1	0	0
1	1	1

$=$

X_1	X_2	L_2
1	1	1
1	0	1
0	1	1
0	0	0

$L_2 = X_1 X_2 \vee X_1 \overline{X}_2 \vee \overline{X}_1 X_2.$

Here the deductive functions L_1, L_2 are obtained from fault propagation tables.

Taking into account that test can be divided into test-vectors the Eq. (1) can be represented as $L_t = T_t \oplus F$. If digital device is described by the components (primitives), which form the values of all lines, then Eq. (4) is used to obtain deductive model L_{ti} on current test-vector T_t from fault-free model of primitive F_i.

$$L_{ti} = T_t \oplus F_i = f_{ti}[(X_{i1} \oplus T_{t1}), (X_{i2} \oplus T_{t2}), ...$$
$$..., (X_{ij} \oplus T_{tj}), ..., (X_{in_i} \oplus T_{tn_i})] \oplus T_{ti}, \quad (4)$$

This is the main equation in deductive analysis of digital projects [3, 6].

To define the algorithm of faults analysis on the basis of Eq. (4) let's introduce the following definitions:

Definition 1. The vector of stuck-at-0 faults (stuck-at-1 faults) $S^0 = (S_1^0, ..., S_i^0, ..., S_n^0)$ $(S^1 = (S_1^1, ..., S_i^1, ..., S_n^1))$, which have been detected by the test-vector $T_t \in T$ is a set of stuck-at faults put in order by line numbers. Stuck-at-0 fault (stuck-at-1 fault) on line i is detected by current test-vector, if $S_i^0 = 1; (S_i^1 = 1)$. Otherwise, if $S_i^0 = 0; (S_i^1 = 0)$, then there is no any fault has been detected on line i.

Definition 2. $D^0 = (D_1^0, ..., D_i^0, ..., D_n^0)$ $(D^1 = (D_1^1, ..., D_i^1, ..., D_n^1))$ is the vector of stuck-at-0 faults (stuck-at-1 faults) put in order by line numbers, that were detected by test T. If $D_i^0 = 1; (D_i^1 = 1)$ then stuck-at-0 fault (stuck-at-1 fault) on line i is detected by at least one test-vector $T_t \in T$. Otherwise, if $D_i^0 = 0; (D_i^1 = 0)$, and fault is not detected.

Definition 3. The matrix of faults $M = [M_{ij}]$, which have been detected by test-vector $T_t \in T$, is a form of representation of list of stuck-at faults. The dimension of the matrix is $n \times n$. The elements of the matrix are initialised according to the equation

$$[M_{ij}]\Big|_{(i,j=\overline{1,n})} = \begin{cases} 0 \leftarrow (i \neq j); \\ 1 \leftarrow (i = j). \end{cases} \quad (5)$$

During the simulation zero values of elements of the matrix can be changed to one $M_{ij} = 1$. It happens if fault is detected.

Taking into account those definitions the practical realization of Eq. (4) can be implemented by the following algorithm:

1. Determination of initial test-vector (t=0). Initialisation of detectable fault vectors: $\forall i(D_i^0 = 0; D_i^1 = 0)$.

2. Determination of the next input test pattern number t=t+1 for $T_t \in T$. If there aren't input patterns (t > k) then the end of simulation.

3. Fault-free simulation of all primitives $F_i(i = \overline{1,n})$ of digital circuit on input test pattern $T_t^X \in T_t$ for the purpose of determination of non-input coordinates $T_t^{\overline{X}} \in T_t$:

$$T_t^{\overline{X}} = f(T_t^X, F). \quad (6)$$

Condition of transition to the next step is identity of all good line values in the consecutive iterations $T_t^r = T_t^{r-1}$.

Note. The pair analysis of consecutive vectors (T_{t-1}, T_t) is used for processing of sequential circuits and organization of event-driven simulation. Primitive $F_i(i = \overline{1,n})$ should be simulated if there are different input line values $[T_{t-1}^X(F_i) \neq T_t^X(F_i)]$ on processed primitive element.

4. Initialisation of matrix of detected faults on applied test-vector: $M = [M_{ij}]$, according to the Eq.(5). Initialisation of vectors of detected faults $\forall i(S_i^0 = 0; S_i^1 = 0)$. Reconfiguration of all primitives $F_i(i = \overline{1,n})$ using Eq. (4) for the current binary vector $T_t \in T$ of the fault free behavior to obtain deductive model $L_t \leftarrow \forall i(L_{ti} = T_t \oplus F_i)$.

5. Forming of non-input lines values of detected fault matrix by the parallel simulation of primitives $L_{ti} \in L_t$.

6. Forming set of vectors of detectable faults:

$$S^0 = (\bigvee_{\forall i \in Y} M_i) \wedge T_t; \; S^1 = (\bigvee_{\forall i \in Y} M_i) \wedge \overline{T}_t \quad (7)$$

Formulas are applied to all matrix rows, corresponding to the primary output.

7. When the condition $(S^0 \vee S^1)^{r-1} = (S^0 \vee S^1)^r$ is true, the evaluation of test pattern $T_t \in T$ quality should be calculated by Eq. (8):

$$Q(T_t) = \frac{1}{2n}[\sum_{i=1}^{n}(S_i^0 + S_i^1)] \quad (8)$$

and go to step 8. Otherwise, if not all detectable faults that were detected on iteration r-1 can be detected on iteration r:

$$\exists i[(S_i^0 \vee S_i^1 = 1)^{r-1} \,\&\, (S_i^0 \vee S_i^1 = 0)^r],$$

then such defects should be eliminated from process of simulation according to the rule:

$$(S_i^0 = S_i^1 = 0) \leftarrow \forall i[(S_i^0 \vee S_i^1 = 1)^{r-1} \,\&\, (S_i^0 \vee S_i^1 = 0)^r]. \quad (9)$$

Transition to step 5.

8. Forming detectable fault vectors:

$$D^0 = D^0 \vee S^0, \;\; D^1 = D^1 \vee S^1 \quad (10)$$

and calculating test quality by following formula:

$$Q(T) = \frac{1}{2n}[\sum_{i=1}^{n}(D_i^0 + D_i^1)]. \quad (11)$$

Transition to step 2.

Represented algorithmic realization is oriented both on table description of complex primitives in RTL level and gate description of digital systems. Processing speed is invariant to the interpretative and compiler types of the model. Interpretative realization is more practically feasible from the point of software implementation.

For example hardware implementation of the resulting deductive function from 2input AND, OR elements is shown on Fig.1.

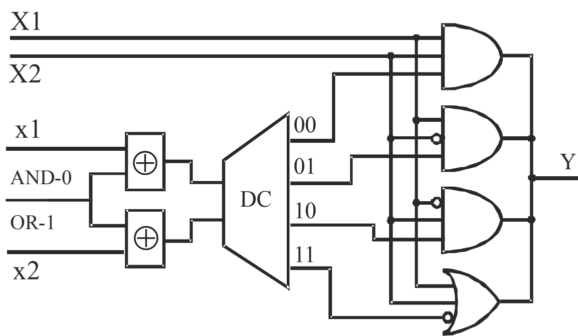

Fig. 1 Fault simulator

Such presentation is oriented on the creation of embedded hardware tools for deductive-parallel fault simulation acceleration that is 10x – 100x faster then available tools on the market today. At the same time, complexity ratio of fault and fault-free models volumes are 7:1.

Such hardware fault analysis approach can be considered as improvement of Aldec® HES™ (Hardware Embedded Simulator) for purpose of solving fault simulation tasks [9].

3. BDP fault simulation method

Presented interpretative-compiler model of deductive-parallel fault analysis is basic of BDP method. It guarantees that the time, required to find the set of all defects on the test vector, is proportional to squared number of lines. To reduce the computational complexity of the task, the new strategy of fault simulation is offered (Fig.9.).

Main idea of the strategy is to convert reconverging fan-outs into pseudo outputs. Then the superposition procedure for tree-like structures is executed only in the case of the appearance of the reconverging fan-out fault.

The software implementation of BDP fault simulation method consists of two main components: preprocessor of structural analysis and simulation algorithm.

The preprocessor is used to find the set of reconverging fan-outs in the circuit as binary vector $R=(R_1,R_2,...,R_i,...,R_n)$ (with the help of one of the described earlier structure analysis methods):

$$R_i=\begin{cases}1\leftarrow R_i\in R^{RC};\\0\leftarrow R_i\notin R^{RC},\end{cases}$$

The computational complexity of this procedure is $Q_r=n^2$. But this procedure is executed only once, at the point of preliminary analysis and hence almost has no influence on total simulation time.

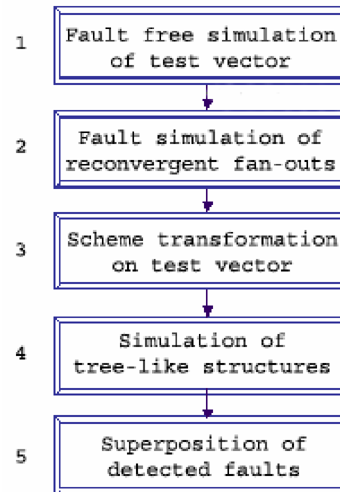

Fig. 2. BDP fault simulation method

The test vector simulation algorithm is used to find the list of detected faults. It includes:

1. Fault –free simulation. It's defined reaction of internal and output lines on applied test-vector $T_t\in T=[T_{ti}]$. It can be represented as

$$T_t=(T_t^X,T_t^Z,T_t^Y).$$

The vector of detected faults is represented as and defined for each row T_t.

2. Fault simulation of reconverging fan-outs by reconfiguration of the reconverging fan-outs into pseudo outputs. Initialization of vector of detected faults $S=(S_i^X=0,S_i^Z=0,S_i^Y=1)$. The stuck-at-fault is detected on line i, if $S_i=1$.

Then according to [5] there are generated initial defects of circuit reconverging fan-outs in form of matrix M=[Mij]. Matrix size is r x n, where r – number of reconverging fan-outs.

Then fault simulation of reconverging fan-outs is performed

$R^1\subseteq R=(R^1=\{R_1^1,R_0^1\},R^0)$ (R^1 - set of reconverging fan-outs; R_1^1 - reconverging fan-

outs, the faults on which are detected; R_0^1-reconverging fan-outs, the faults on which are not detected; R^0-lines, which are not reconverging fan-outs). The method is oriented on the schemes where the number of fan-outs is not more then 20%, which is common for majority of digital designs.

3. Model decomposition. The extra images (tree-like structures), on which lines faults can't be detected, are excluded from fault simulation

$$R = R \setminus f^*(R_0^1).$$

4. Fault simulation of rest lines, which don't belong to reconverging fan-outs ($R^1{}_1 v R^1{}_0$), and to tree-like structures excluded from simulation on step 3. The deductive- parallel algorithm is applied to matrix of detectable defects M of current element, not circuit. Such analysis can be performed deductively, by using input fault lists of every logic element.

5. Superposition of vectors of detected faults on the corrected model of digital design. It is performed disjunction of the input vector of detected faults of primitive i $S^i = (S_1^i, S_2^i, ..., S_j^i, ..., S_{n_i}^i)$ with vector of detected faults S of the circuit, in case if output line of element i is equal to "1", $S_i = 1$:

$$S(X_{ij}^a) = S(X_{ij}^a) \bigvee_{j=1}^{n_i - 1} S_j^i \leftarrow S_i = 1, \quad (12)$$

Where, $X_i^a = (X_{i1}^a, ..., X_{ij}^a, ..., X_{i(n_i-1)}^a) -$ is a vector of numbers of inputs for primitive i.

When applying such approach to the whole circuit, the superposition procedure is reduces to sequential union of vectors of detected faults for the primitives, which outputs are predecessors for the inputs and vectors of detected faults on reconverging fan-outs - pseudo outputs. Otherwise the fault simulation is performed only for visible output lines of the digital design, complemented with the reconverging fan-outs, on test pattern T_t: $R^Y = R^Y \cup R_1^1$, R^Y-outputs of the circuit; R_1^1 reconverging fan-outs, where faults can be detected.

4. Topological BDP fault simulation method

Superposition procedure modification is described in this section. The idea is to trace defects backwards through the topology of the circuit. But it is impossible to using general superposition procedure because of impossibility of one-dimensional activation. Such situation is illustrated below by an example.

Example 1. Let's consider the circuit on Fig.3 to define the set of faults, which can be detected on specified test-vectors. To achieve that superposition procedure should be used.

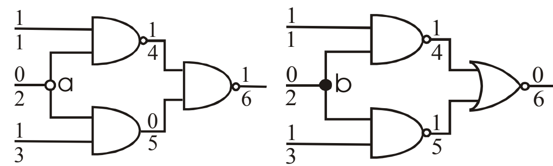

Fig.3. False faults detection and undetected faults

The activation of faults on lines a, b gives incorrect results for both circuits.

Let's consider the left circuit. Constant fault 2^1 is incorrectly detected on one-dimensional way 2-5-6 with the help of the back-tracing procedure. However the fact that this defect changes the value on line 4 from 1 to 0 is not considered. When the value of line 4 is changed from 1 to 0 the fault 2^1 can't be seen on output of the circuit. So the defect 2^1 cannot be detected on test pattern 101.

The right circuit on Fig. 3 is an example of another situation. There is no one-dimensional way to carry the defects from inputs (especially from the line b) to the output line 6. Nevertheless the fault on the line 2 can be detected on given test pattern. The fault on the line 2 (2^1) causes multiple defect on the lines 4 and 5, which will change the value of output line.

In both cases there is essential incorrectness. So it is not correct to use only the idea of one-dimensionality for tracing the way to carry faults from inputs to outputs of the circuit.

As long as mentioned incorrectness is concerned with one-dimensional activation of faults on reconverging fan-outs only, it is necessary first to process the fan-outs only and then exclude them from the circuit consideration. The circuit will have tree-like structure, acceptable for one-

dimensional back-tracing. On the stage of the preliminary analysis the additional procedure of defining all reconverging fan-outs should be performed. (Fig. 4, part P).

Further will be considered analysis according to the topology of the digital device, hence it is naturally to call the analysis algorithm - topological.

Thus, the topological algorithm for simulation of digital devices Fig.4 includes following steps:

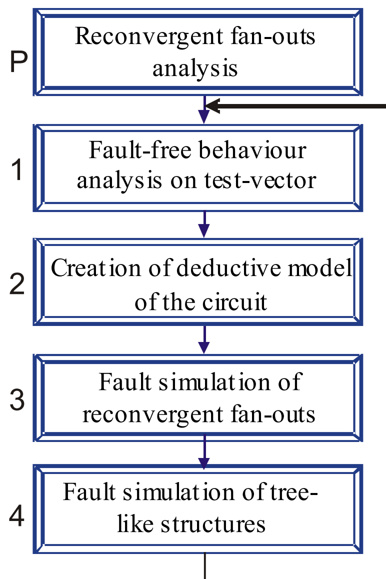

Figure 4. Topological simulation algorithm

1. Analysis of fault-free behaviour of digital circuit on specified input test-vector.

2. The conversion of the circuit into deductive model on the current test-vector.

3. Fault simulation of reconverging fan-outs on deductive model of the circuit.

4. Back tracing of detectable faults on tree-like structure of deductive model.

Point 3 is oriented on processing of the reconverging fan-outs only. The number of them is significantly less then the number of the rest lines. Point 4 is oriented on fault simulation of lines, which belong to the tree-like sub-graphs.

The proof of the theorems and consequences listed below is the theoretical basis of point 4.

Lemma1. The reconverging fan-outs $R_i^1 \in R^1$ are the reason of divisible defects appearance on input lines of combinational circuit.

Theorem 1. *For tree-like structure of deductive scheme the inverse input of the AND primitive:* $\overline{X}_i \in L$ prohibit to *carrying all the faults of the lines-predecessors to the output.*

Theorem 2. *If there is AND primitive in the tree-like structure of deductive scheme L and this primitive has more than one non inverse input* $X_i X_j$ *then such a primitive prohibit to carry all the faults, which belong to lines-predecessors of all its inputs to the output.*

Consequences: 1) Inverse input of deductive element AND prohibits to activate all faults on lines- predecessors, which belong to this input. 2) If deductive element has more then one non inverse inputs, then all its inputs must be defined as inverse. 3) The deductive AND element will allow to carry the faults of lines-predecessors only through non inverse input. The element should have only one such input. 4) Deductive OR element can't have inverse inputs. 5) Reconverging fan-out is marked with the inversion (circle on fan-out line) if the fault on this line is not detected by the test-vector. 6) The inversion on input or output line is a condition to stop tracing the faults through this branch of tree-like structure to the output. 7) If on the line with fan-out (on topological figure of the circuit it is further marked with the bold circle) can be detected fault on the test-vector, then it should be considered as the observable output during applying the back-trace procedure. 8) Interpretation of topological simulation results: the faults on the lines, which are not marked with the inversion on the deductive model of the circuit, are detectable.

To illustrate the main stages of topological simulation let's consider example given below.

Example 2. Lets consider the digital device on Fig. 5 (first circuit from the top), which includes 3 reconverging fan-outs. The device has 16 lines, 7 inputs. Let's find the list of stuck-at faults, which can be detected by test-vector 1011111. The values of lines after fault-free simulation are in brackets. The result of conversion of fault-free model of digital device into deductive model and simulation of reconverging fan-outs is presented on Fig. 5 (second circuit from the top). The results of fault simulation of reconverging fan-outs are also represented here. It is defined

that faults of all the fan-outs (2, 10, 13), inverse to fault-free state, are detected by this test-vector. These lines are marked with black circles.

The back-tracing procedure lies in building of maximal tree-like sub graphs. They are bounded on topology with transparent circles. Here the black circles define the reconverging fan-outs, which faults are detected. These fan-outs should be considered as observable outputs on Fig.5 (third circuit from the top.). All the faults, which are detected by test-vector, are also represented on this figure: {2, 8, 9, 10, 11, 12, 13, 14, 15, 16}. The following statement is true for simulation of the given digital device: the faults of the lines, which are not marked with transparent circles (inversion), are detected by test-vector.

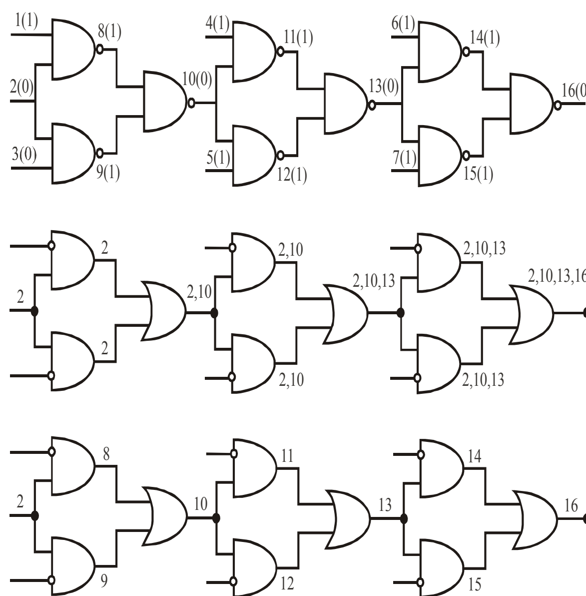

Fig.5. Simulation of the circuit with fan-outs

The structure of evolutionary development of fault simulation methods is represented on Fig. 6.

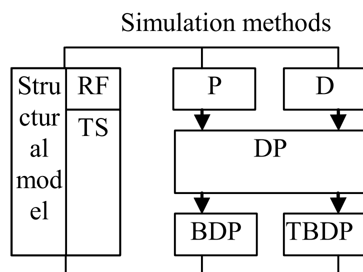

Figure 6. The evolution of simulation methods

Deductive and parallel algorithms were developed first. Then the deductive-parallel algorithm was developed. It is universal but relatively slow. After it the back traced deductive-parallel method was realized. It is oriented on high-speed processing of digital devices. Then it was modified into topological fault-simulation method, oriented on the gate-level description of the circuits. According to this algorithm firstly the set of reconverging fan-outs and tree-like structures is defined. Then for fault simulation of reconverging fan-outs the deductive-parallel algorithm is used. For the analysis of tree-like structures the topological fault simulation method is used. Such task sharing allows speeding up fault simulation in comparison with basic methods (deductive and parallel).

5. Conclusion

The offered fault simulation method is oriented on the processing of complex digital devices targeted into ASIC and containing millions of gates. The program implementation of the method was tested on several hundreds of combinational and sequential benchmarks and showed good speed-up results in comparison with classic parallel and deductive fault simulation algorithms. Benchmarks are presented in Figure 7. 1000 test patterns were generated and simulated for each circuit. The simulation speed was increased at least in 10 times. The benchmarks for three different fault simulation methods are shown on Fig.8. Where it is easy to see clear advantage of BDP and TBDP-methods in comparison with deductive-parallel is illustrated. The advantage in speed is more efficient for the VLSI circuits. The number of RFO in samples is about 20% from total number of lines. The main results of given work is improving of deductive-parallel method that consists from:

1) Creation of general deductive-parallel model of digital circuit analysis based on back-traced superposition procedure. Computation complexity dependency is linear to number of equipotent lines;

2) Development of algorithms for structural and functional analysis of digital circuits with purpose of the RFO set definition and circuit structure reconfiguration for superposition procedure realization;

3) Creation of internal interpretative-compile model of digital device.

4) Development of topological fault simulation method according to the topology of the digital device circuit.

ELECTRICAL TEST IS NOT ENOUGH FOR QUALITY

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Electrical test means Functional Test (FT), In Circuit Test (ICT) or Boundary Scan Test (BST) or even a combination of these technologies. However, with modern technology, like SMD (Surface Mounted Devices) technology, BGA (Ball Grid Array) components and extremely small component dimensions, electrical test alone does not meet the quality requierments.

Electrical test can not identify bad soldering and bad alignment of components, as examples. Missing decoupling capacitors and so on can not be detected because of it is hard to get physical access for testprobes. Do not forget that digital designs contains a lot of analogue devices!

The tutorial will discuss today test technology with equipment for ICT and BST as well as its pros and cons. And as the addition of this, Inspection. Inspection has traditonally been performed manually but this is not realistic today with board crowded by components. Today Inspection is performed by machine vision. Optical technique named Automated Optical Inspection (AOI) and more advanced X-ray inspection (AXI). AOI and AXI is not the future, it is here today.

EMC /EMI is also a growing challenge and some new ideas will be discussed how to test for these phenomenas.

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