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10th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2012)

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The main target of the **IEEE East-West Design & Test Symposium (EWDTS)** is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contributions to EWDTS'12 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
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- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
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- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
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- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television

The Symposium will take place in Kharkov, Ukraine, one of the biggest scientific and industrial center. Venue of EWDTS 2012 is Kharkov National University of Radioelectronics was founded 81 years ago. It was one of the best University of Soviet Union during 60th - 90th in the field of Radioelectronics. Today University is the leader among technical universities in Ukraine.

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CONTENTS

An Efficient Fault Diagnosis and Localization Algorithm for Successive-Approximation Analog to Digital Converters Melkumyan T., Harutyunyan G., Shoukourian S., Vardanian V., Zorian Y.	15
Application of Defect Injection Flow for Fault Validation in Memories Amirkhanyan K., Davtyan A., Harutyunyan G., Melkumyan T., Shoukourian S., Vardanian V., Zorian Y.	19
SSBDDs and Double Topology for Multiple Fault Reasoning Raimund Ubar, Sergei Kostin, Jaan Raik	23
Self Compensating Low Noise Low Power PLL design Vazgen Melikyan, Armen Durgaryan, Ararat Khachatryan, Manukyan Hayk, Eduard Musaelyan	29
Optimization Considerations in QCA Designs Zahra NajafiHaghi, Marzieh Mohammadi, Behjat Forouzandeh, Zainalabedin Navabi	33
Implementation of Address-Based Data Sorting on Different FPGA Platforms Dmitri Mihhailov, Alexander Sudnitson, Valery Sklyarov, Iouliia Skliarova	38
Comparison of Model-Based Error Localization Algorithms for C Designs Urmaz Repinski, Jaan Raik	42
Synthesis of Clock Trees for Sampled-Data Analog IC Blocks Bilgiday Yuce, Seyrani Korkmaz, Vahap Baris Esen, Fatih Temizkan, Cihan Tunc, Gokhan Guner, I. Faik Baskaya, Iskender Agi, Gunhan Dundar, H. Fatih Ugurdag	46
Experiences on the road from EDA Developer to Designer to Educator H. Fatih Ugurdag	50
Multi-Beam Constant Modulus Adaptive Arrays in Real-Valued Arithmetic Victor I. Djigan	54
Simulation of Total Dose Influence on Analog-Digital SOI/SOS CMOS Circuits with EKV-RAD macromodel Petrosyants K. O., Kharitonov I. A., Sambursky L. M., Bogatyrev V. N., Povarnitcyna Z. M., Drozdenko E. S.	60
Models for Embedded Repairing Logic Blocks Hahanov V.I., Litvinova E.I., Frolov A., Tiecoura Yves	66
Real-time Interconnection Network for Single-Chip Many-Core Computers Harald Richter	72
Invariant-Oriented Verification of HDL-Based Safety Critical Systems Kharchenko V., Konorev B., Sklyar V., Reva L.	76
An Improved Scheme for Pre-computed Patterns in Core-based SoC Architecture Elahe Sadredini, Qolamreza Rahimi, Paniz Foroutan, Mahmood Fathy, Zainalabedin Navabi	80

Synthesis of Moore FSM with transformation of system in CPLD Aleksander Barkalov, Larysa Titarenko, and Sławomir Chmielewski	85
A WSN Approach to Unmanned Aerial Surveillance of Traffic Anomalies: Some Challenges and Potential Solutions David Afolabi, Ka Lok Man, Hai-Ning Liang, Eng Gee Lim, Zhun Shen, Chi-Un Lei, Tomas Krilavičius, Yue Yang, Lixin Cheng, Vladimir Hahanov, and Igor Yemelyanov	91
Synthesis of Qubit Models for Logic Circuits Wajeb Gharibi, Zaychenko S.A., Dahiri Farid, Hahanova Yu.V., Guz O.A., Ngene Christopher Umerah, Adiele Stanley	95
Theory of Optimal Nonlinear Filtering in Infocommunication's Problems Victor V. Panteleev	102
Verification of Specifications in the Language L with respect to Temporal Properties Expressible by GR(1) Formulas Anatoly Chebotarev	110
Properties of code with summation for logical circuit test organization Anton Blyudov, Dmitry Efanov, Valery Sapozhnikov, Vladimir Sapozhnikov	114
Loop Nests Parallelization for Digital System Synthesis Alexander Chemeris, Julia Gorunova, Dmiry Lazorenko	118
Decreasing the Power Consumption of Content-Addressable Memory in the Dataflow Parallel Computing System Levchenko N.N., Okunev A.S., Yakhontov D.E., Zmejcev D.N.	122
WebALLTED: Interdisciplinary Simulator Based on Grid Services Zgurovsky M., Petrenko A., Ladogubets V., Finogenov O., Bulakh B.	126
Malfunctions Modeling of Converters and Homogeneous-chain Distributed Structure Devices Artur Gulin, Zhanna Sukhinets	130
On structure of quasi optimal algorithm of analogue circuit designing Zemliak A., Michua A., Markina T.	134
A Neuro-Fuzzy Edge Based Spectrum Sensing Processor for Cognitive Radios Mohammadreza Baharani, Mohammad Aliasgari, Mohammadreza {Najafi, Jamali}, Hamid Noori	138
Qubit Model for Solving the Coverage Problem Hahanov V.I., Litvinova E.I., Chumachenko S.V., Baghdadi Ammar Awni Abbas, Eshetie Abebech Mandefro	142
PDF testability of the circuits derived by special covering ROBDDs with gates Matrosova A., Nikolaeva E., Kudin D., Singh V.	146
Compositional Microprogram Control Unit with Operational Automaton of Transitions Alexander Barkalov, Roman Babakov, Larisa Titarenko	151
Observability Calculation of State Variable Oriented to Robust PDFs and LOC or LOS Techniques Matrosova A., Ostanin S., Melnikov A., Singh V.	155

Low-Voltage Low-Power 2.5 GHz Linear Voltage Controlled Ring Oscillator Hayk H Dingchyan	161
High Speed IC Output Buffer with Reduced Power Consumption Karine Movsisyan	165
Engineering-Maintenance Methods of the Calculation Service Area Fixed BWA-paths Sergey I. Myshlyakov, Victor V. Panteleev	170
Analyses of two run march tests with address decimation for BIST procedure Ireneusz Mrozek, Svetlana V. Yarmolik	176
Design of Area Efficient Second Order Low Pass Analog Filter Andranik Hovhannisyan	180
Power Consumption Analysis of Content-Addressable Memories Levchenko N.N., Okunev A.S., Yakhontov D.E.	183
IC Physical Design Optimization Due to Effects of Device Physical Geometries Avag Sargsyan	187
System-on-Chip FPGA-Based GNSS Receiver Alexander Fridman, Serguey Semenov	190
Testware and Automatic Test Pattern Generation for Logic Circuits Victor Zviagin	196
Artificial Neural Network for Software Quality Evaluation Based on the Metric Analysis Oksana Pomorova, Tetyana Hovorushchenko	200
Self-Compensation of Influence of Parasitic Gate-Drain Capacitances of CMOS Transistors in Analog Microcircuitry Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov	204
Hash-based Detection of OFDM Watermarking Symbol for Radiotelephone Identification Aleksandr V. Shishkin, Aleksandr A. Lyashko	208
A Novel Wideband Circular Ring DGS Antenna Design for Wireless Communications Rakesh Sharma, Abhishek Kandwal, Sunil Kumar Khah	211
Universal technique of the analysis of round-off noise in digital filters with arbitrary structure described by topological matrixes Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev	215
Hardware Reduction for Compositional Microprogram Control Unit Dedicated for CPLD Systems Barkalov A., Titarenko L., Smolinski L.	219
Conservative Finite-difference Scheme for the Problem of Laser Pulse Propagation in a Medium with Third-order Dispersion Vyacheslav A. Trofimov, Anton D. Denisov	225
A Four Bit Low Power 165MSPS Flash-SAR ADC for Sigma-Delta ADC Applications Hasan Molaei, Khosrow Hajsadeghi	229
Matrix Implementation of Moore FSM with Nonstandard Presentation of State Codes Titarenko L., Hebda O.	233

Alowpower1.2GS/s4-bitflashADCin0.18mCMOS Mohammad Chahardori, Mohammad Sharifkhani, Sirous Sadughi	237
Symmetrical Differential Stages on CMOS Transistors with Circuits of Self-Compensation and Cancellation Sergey G. Krutchinsky, Grigory A. Svizev, Alexey E. Titov	241
Lower Bound of Error in AOA Based Passive Source Localization Using Single Moving Platform Hejazi F., Norouzi Y., Nayebi M.M.	245
A Design for Testability Technique for Quantum Reversible Circuits Joyati Mondal, Debesh K. Das, Dipak K. Kole, Hafizur Rahaman	249
A Flexible Design for Optimization of Hardware Architecture in Distributed Arithmetic based FIR Filters Fazel Sharifi, Saba Amanollahi, Mohammad Amin Taherkhani, Omid Hashemipour	253
Models for Quality Analysis of Computer Structures Murad Ali Abbas, Chumachenko S.V., Hahanova A.V., Gorobets A.A., Priymak A.	258
Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology Daniel Foty, Bruce Smith, Saurabh Sinha, Michael Schröter	264
Sampling Theorem for Finite Duration Signal in Limited Frequency Band Gamlet S. Khanyan	270
SiGe HBT Performance Modeling after Proton Radiation Exposure Konstantin Petrosyants, Maxim Kozhukhov	274
Classical Models of Test used in Advanced Electronics Quality Assurance Surendra Batukdeo	278
The Use of Natural Resources for Increasing a Checkability of the Digital Components in Safety-Critical Systems Drozd A., Kharchenko V., Antoshchuk S., Drozd J., Lobachev M., Sulima J.	283
New version of Automated Electro-Thermal Analysis in Mentor Graphics PCB Design System Petrosyants K.O., Kozyrko P.A., Kharitonov I.A., Sidorov A.V., Chichkanov Y. N.	289
An Approach to Testing of Planar Integrated Antennas in Frequency Range of 5–7 GHz Aleksandr Timoshenko, Ksenia Lomovskaya, Victor Barinov, Andrey Tikhomirov	293
Optimal project solution decision making in telecommunication systems using multicriteria optimization methods Valery Bezruk, Alexander Bukhanko	298
Software implementation and debugging of forward error correction codes Alexey Smirnov, Danila Migalin, Ilya Muravyev, Leonid Pertsev	303
Architecture of Built-In Self-Test and Recovery Memory Chips Andrienko V.A., Moamar Daa, Ryabtsev V.G., Utkina T.Yu.	307
The methods of exclusion of variables in symbolic time models of linear periodically time-variable circuit Yuriy Shapovalov, Dariya Smal	311

Two-Component Encoding of Approximating Picture Pixels in Telecommunication Facilities Barannik V., Dodukh A., Safronov R.	315
Development of parameterized cell using Cadence Virtuoso Vadim Borisov	319
Simulation Methods of Diffusion Alloying Process by Means of Taurus TSUPREM-4 Programme Lagunovich N.L., Borzdov V.M.	321
Control and Diagnosis by Complexity Indicators of System Functioning Process Tverdokhlebov V.A.	323
Features of the Transfer of Information with Different Reliability in a Single Channel Alexander Bakhtin, Leonid Pertsev, Olga Timofeeva	327
Construction of Signals with Controlled Peak-Factor Koshevyy V. M., Dolzhenko D.O.	330
The Effective Method of Space Filtering of Noise in Rayleigh Communication Channel with the Adaptive Antenna Maistrenko G. V., Rybalko A. M., Shokalo V. M., Strelnitskiy A. A.	333
A New Structure for Interconnect Offline Testing Somayeh Sadeghi-Kohan, Shahrzad Keshavarz, Farzaneh Zokaei, Farimah Farahmandi, Zainalabedin Navabi	336
Researching of Mathematical Models Based on Optimal Control Approaches for Congestion Control in Telecommunication Network Lemeshko A.V., Semenyaka M.V.	341
Higher Order Propagation Modes Error and Its Compensation Zaichenko O. B., Klyuchnyk I. I., Martynenko L. G.	345
Strategy of analyzing most common algorithms for path finding in discrete labyrinth using software statistic data collector Krasnov Evgeniy, Dmitry Bagaev	349
Method of Implementation of Technology of Orders Based Transparent Parallelizing for Solving Computationally Complex Problems on Cluster Vitaliy D. Pavlenko, Viktor V. Burdejnyj, Sergey V. Pavlenko	353
Scheduling Tests for 3D SoCs with Temperature Constraints Indira Rawat, Gupta M.K., Virendra Singh	356
Automated application mapping into Network-on-Chip topologies Bykov S. O.	360
MIMO Radar with Phase-coded waveforms Amirsadegh Roshanzamir, Bastani M. H.	363
BBN-based Approach For Assessment of Smart Grid And Nuclear Power Plant Interaction Eugene Brezhnev, Vyacheslav Kharchenko	367
Design, Test and Fault Detection in QCA 4-to-1 Multiplexer Zahra NajafiHaghi, Behjat Forouzandeh	374

The Evaluation of Statistical Characteristics of the Retransmission Meter Signal Frequency and Initial Phase on the Basis of VHDL-model Dmitry A. Velychko, Iegor I. Vdovychenko	378
A Research of Heuristic Optimization Approaches to the Test Set Compaction Procedure Based On a Decomposition Tree for Combinational Circuits Valentina Andreeva, Kirill A. Sorudeykin	382
Power Reduction of 7T Dual-Vt SRAM Cell Using Forward Body Biasing Sahba Sabetghadam Jahromi, Raziye Bounik	388
VLSI: An Investigation into Electromagnetic Signatures (EMS) for Non-Invasive Testing and Signal-integrity Verification Kadim HJ, Coulibaly L. M.	392
Secure Data over GSM based on Algebraic Codebooks Kazemi R., Nashtaali D., Boloursaz M., Behnia F.	397
Simulation of Telecommunication Channel Using Volterra Model Vitaliy D. Pavlenko, Viktor O. Speransky	401
Extracting Complete Set of Equations to Analyze VHDL-AMS Descriptions Arezoo Kamran, Vahid Janfaza, and Zainalabedin Navabi	405
A Data Modem for GSM Adaptive Multi Rate Voice Channel Boloursaz M., Hadavi A. H., Kazemi R., Behnia F.	409
Trends and prospects of development of techniques for extracting acoustic sounding information of the atmospheric boundary layer Klyuchnik I., Panchenko A., Umyarov R.	413
Decision-Making in Robotics and Adaptive Tasks Tsybal A.M., Bronnikov A.I.	417
Design of Nonvolatile Memory Based on Magnetic Tunnel Junction for Special Electronic Systems Aleksandr Kostrov, Vladislav Nelayev, Viktor Stempitsky, Anatoly Belous, Arkady Turtsevich	421
Improving the Dependability of a Water Supply System via a Multi-Agent based CPS Teodora Sanislav, Liviu Miclea, Paolo Prinetto	425
Cyber Security Lifecycle and Assessment Technique for FPGA-based I&C Systems Illiashenko Oleg, Kharchenko Vyacheslav, Kovalenko Andriy	432
FPGA Technologies in Medical Equipment: Electrical Impedance Tomography Perepelitsyn Artem, Shulga Dmitry	437
A Trend-based Design Space Exploration of Multi-core Systems Using Regression Modeling Fazeleh Hajari Taheri, Omid Fatemi	441
Synchronous Rectifiers Enable High Efficiency for Buck-Boost Converter Yurii Shynkarenko and Igor Klyuchnyk	445

Test Data Compression Strategy While Using Hybrid-BIST methodology Elmira Karimi, Mohammad Hashem Haghbayan and Mahmood Tabandeh	449
Self-Adaptive Mobile Wireless Hotspot Zones Yanovsky M., Kharchenko V., Gorbenko A.	454
The Systolic Compositions of Two-dimensional and Multidimensional Lattice Filters for Space-Time Signal Processing David I. Lekhovytskiy, Andrii V. Semeniaka, and Dmytro S. Rachkov	458
Power Efficient Implementation of Homogenous Multi-Core Processors Aram Poghosyan	462
Assertion Based Method of Functional Defects for Diagnosing and Testing Multimedia Devices Vladimir Hahanov, Karyna Mostova, Oleksandr Paschenko	465
Improved Scaling-Free CORDIC algorithm Leonid Moroz, Taras Mykytiv, Martyn Herasym	470
Coding Tangible Component of Transforms to Provide Accessibility and Integrity of Video Data Barannik V.V., Hahanova A.V., Krivonos V.N.	475
Review of the botnet detection techniques Oleg Savenko, Sergiy Lysenko, Kryshchuk Andrii	479
MEMS Intellect Multiprobes Contacting Devices for Electrical Checking-up of Multilayers Commutative Boards and BGA/CSP Electronic Components Neвлиudov I.Sh., Palagin V.A., Razumov-Frizjuk E.A., Zharikova I.V.	483
Internet of Things: A Practical Implementation based on a Wireless Sensor Network Approach Michele Mercaldi, Andrea D’Oria, Davide Murru, Hai-Ning Liang, Ka Lok Man, Eng Gee Lim, Vladimir Hahanov, Mischenko Alexander	486
Investigation of EM Wave Propagation of the Wireless Capsule in Human Body Eng Gee Lim, Zhao Wang, Jin Hui Chen, Tammam Tillo, Ka Lok Man	490
Using pyroelectric detectors in the design of temperature measuring devices Bondarenko A.Yu, Klyuchnik I.I.	494
Transaction Level Model of Embedded Processor for Vector-Logical Analysis Irina V. Hahanova, Volodymyr Obrizan, Alexander Adamov, Dmitry Shcherbin	497
Embedded Intelligent Control Systems on the Basis of Elementary Fuzzy-Logic Cells Dontsova A., Vassiliev A.E.	502
Interconnection Analysis of the Integral Reliability Characteristics of the Monoergative Computer System and User’s Competency Krivoulya G., Shkil A., Kucherenko D.	505
System approach to determination of ADC parameters Knyshev Ivan	511
Methodological Aspects of Complex Ecological Estimation of Man-Caused Territory State and Mathematical Modelling of Processes in a Environment System Kozulia T. V., Sharonova N. V. , Emelianova D. I., Kozulia M.M.	514

Method for “Failure on Demand” Latent Faults Diagnosis of NPP Safety Control Systems Gerasymenko K.E.	519
Informational Saturation of Noise Signals Kolodiy Z. A., Kolodiy A.Z.	523
The Positional Structural-Weight Coding of the Binary View of Transformants Barannik V., Krasnoruckiy A., Hahanova A.	525
Synchronization of a Fuzzy Automata Speranskiy Dmitriy	529
Models for SoC Infrastructure of Radio Frequency Identification with Code-Division Multiple Filippenko I.V., Hahanova I.V., Filippenko I.O, Maksimov M., Chugurov I.	535
Factorization of Rhythmograms Parametric Spectra on the Base of Multiplicative Linear Prediction Models Nataliia V. Kudriavtseva, Iryna O. Fil	538
Logi-Thermal Analysis of Digital Circuits Using Mixed-Signal Simulator Questa ADMS Petroshyants K.O., Rjabov N.I.	541
Method of Hybrid Regression Analysis in the Calibration Experiments Ordinartseva N. P.	545
Keynotes speeches and Invited Reports	548
AUTHORS INDEX	554

Models for Embedded Repairing Logic Blocks

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Abstract

The models of combinational circuits, focused on solving practical problems of embedded repairing components of the logic units are proposed. The logical circuit is complemented by operational and control automata for modeling digital devices, which increases processing time and hardware costs for creating a wrap of addressable elements. The structures can also be used for hardware modeling functionalities of digital projects by using PLD, which allows improving the performance of software model verification. The proposed solution of embedded gate repair for combinational circuits makes it possible to comprehensively solve the problem of autonomous repairing digital systems on chips due to the time and hardware project redundancy [1-12].

1. Introduction

If executing with failures within a single chip, the strategy of increasing the reliability of the system based on reconfiguring the functionality can be used, but it has two disadvantages: 1) considerable time of this operation is incompatible with the functioning of critical systems; 2) significant complication of reconfiguring related to the existence of faulty areas on the chips.

The second way of improving the reliability of digital systems-on-chips can be the addition of redundant elements to the basic functionality, which are designed to compensate for negative effects of faulty components by their readdressing in the testing loop and fault detection. It requires smaller time cycle in comparison with reconfiguration of functional areas of the chip. Implementation of the second way, proposed in [9-12], lies in adding (modifying) three components (spare functional elements and ports for reading/writing data, advanced multiplexers for switching the first two ones) in SoC functionality, which enables the replacement of faulty elements in the cycle BIST/BISR. The reliability of a discrete area on the chip that implements the complete functionality of a digital system is characterized by the criterion with

an exponential distribution depending on the intensity λ of uncorrelated failures, which are constant over time: $R_A(t) = e^{-\lambda t}$. To consider the reliability of the original structure as a whole, the following estimation can be used [9]: $R_O(t) = R_A(t)^{A_O}$, $A_O = M \times A_{FU}$. At that the system is unable to compensate for the failures, resulting it in inoperable state. When considering the complexity of the hardware (Area) of the system with redundancy A_O , containing M main components and N spares, to repair functional modules with faults the following conversions of expressions for determining the reliability evaluation R_{BISR} can be used:

$$\begin{aligned} R_{BISR} &= R_{SW} \times R_{MN}; \\ R_{MN} &= \sum_{i=M}^N \binom{N}{i} R_{FU}^i \times [1 - R_{FU}]^{N-i}; \\ R_{SW} &= R_O^{(A_{SW})/A_O} = R_O^{(A_{SW})/(M \times A_{FU})}; \\ R_{FU} &= R_O^{(A_{FU})/A_O} = R_O^{1/(M)} = R_O^{-M}; \\ R_{BISR} &= R_O^{(A_{SW})/(M \times A_{FU})} \times \\ &\times \sum_{i=M}^N \binom{N}{i} R_O^{i-M} \times [1 - R_O^{-M}]^{N-i}. \end{aligned}$$

Here A_{FU}, A_{SW} – a number of discrete elements (hardware complexity) in functional and spare component of the structure A_O ; R_{MN}, R_{SW}, R_{FU} – reliability indexes of the system with redundant components, auxiliary hardware for switching, and functional component respectively. The best value of reliability index of the system is fixed when the parameter of switching (addressed) hardware A_{SW} tends to zero. Thus, the reliability of the system with redundancy will always be higher than the reliability of the structure without spare components, if the volume of the switching hardware is less than the functional one. The exception is the case when $M=1, N=0$, and reliability of the systems with redundancy and without it are equal.

The ability to create circuits with built-in self-testing and self-repairing is considered in [10-12]. Now

these problems are well solved for regular structures, such as memory. At the same time for the circuits that have combinational organization of logic elements, this problem is much more difficult. In paper [10] it is proposed to divide the circuit on separate blocks and add one spare for every three basic blocks or two spares for 6 basic blocks, Fig. 1. If a fault is detected a spare can replace one of the base functional modules. To manage the repairing it is necessary the input and output switching circuits, decoder of block selection, and two bits of memory to store the system state.

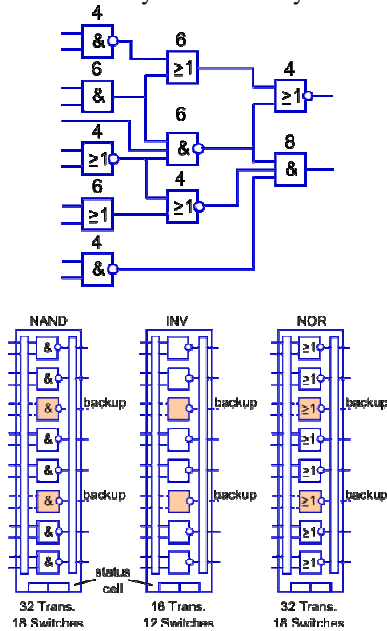


Fig. 1. Reconfigurable logic and mapping circuits

It has been found that the higher dimension of system blocks the smaller the percentage of redundant hardware that is necessary for the implementation of self-testing and repairing circuits. For 32-bit ALU, a number of redundant elements is equal to 38%, while for the AND-NOT gate – 200%. To reduce redundancy and simplify the self-test circuit spares are controlled by the same circuit. At that the model of errors is based on the assumption that only one block of a subsystem can be faulty at the current time. Self-test and self-repair circuits are initiated by turn-on power, and they perform test functions when configuring FPGA. In [9] a strategy for creating self-testable logic circuits without description of realization is proposed. It is shown the abstract architecture of reconfigurable block with unlimited number of sub-blocks and without taking into account the redundancy for creating it.

Disadvantages and comments: 1. There is mentioned FPGA, but the results don't focused on real chip architecture with configurable CLB, which are

basic elements for implementation of combinational circuits. Gates, standard elements are considered but not blocks CLB. 2. Replacing a single logic element in CLB is hard to implement, because the function on the blocks is presented in tabular form. The minimum block for the construction of self-testable circuits can be only CLB. 3. The proposed self-testing method does not apply to specific parts of the adder and devices based on them. Adders are realized on through carry lines, directed along the CLB columns of FPGA. Impossible to exclude a block from the adder without violating the integrity of the device. Therefore, redundancy can be realized only for whole component or it is necessary to change FPGA circuit, but at microelectronics level. 4. Creating self-test circuit at the level of logic elements leads to a high redundancy of hardware. The topical problem is generating register or system-level descriptions of digital devices to obtain a uniform circuit, which can be transformed in self-repairable structure. A method for self-repairing based on the use of regular FPGA structure and exclusion CLB column or row with faulty element is proposed, Fig. 2.

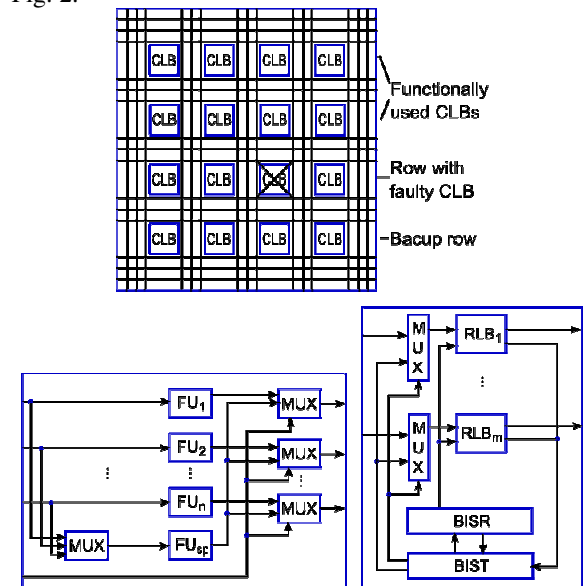


Fig. 2. Built-in-self repair for RLBs

The authors argue that the method needs to be improved. In fact, it seems more realistic and technologically advanced, because it is permissible to add redundant CLB columns, introducing an additional shadow configuration.

The concept of addressed performing logical operations, implemented in the memory elements LUT of programmable logic devices (PLD), provides the potential possibility to create on-chip address space only for embedded repair of all components involved

in functionality [1-8]. The tendency of increasing the memory leads to the possibility of embedded repair of faulty cells by providing additional spare logic cells. The problem of autonomous removal of logic element faults (self-repair) is associated with the lack of addresses. But it can be solved if flexible connections between logic elements will be formed by using structure description program located in memory and connected the logical components in the circuit. In addition to the structure of element interaction the memory must contain a procedure for their processing. In the event of a fault in one of the addressable logical elements, the BISR system will repair it by readdressing to a known-good spare.

The aim of this paper is to improve the quality and reliability of digital systems-on-chips by creating an infrastructure for embedded testing, diagnosis, optimization and repairing through hardware redundancy and reduction of the speed of functional operations [1-8].

Problems and references: 1) Analysis of modern repair technologies for SoC components [4-11]. 2) Development of mathematical model for embedded repairing of logic elements, involved in combinational structure of the functionality, implemented in SoC [4-8]. 3) Creation of operational and control automata to emulate the functionality of combinational circuit in a chip PLD [1-3].

2. Model of combinational structure

The few works devoted to repair of logic circuits [6, 9-12] describe the two ideas. The first one is the reconfiguration of the structure of logical components off-line, which provides the possibility of replacing each of the faulty primitives. The second one creates the conditions for replacement of faulty components through the use of spare components and extension of multiplexers for readdressing failed primitives. An example for the considering the theory and practice of addressing primitives of combinational circuits for built-in repairing functional failures of the logic elements by using the simplest circuit structure is presented below (Fig. 3).

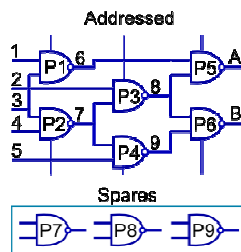


Fig. 3. Addressable logic elements

It contains six logic elements of the same type, which can be represented in the address space by the following list (two-dimensional array):

$$S = \begin{array}{c|cccccc|ccc} \text{No} = & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\ \text{P} = & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ \text{L}_1 = & 1 & 3 & 2 & 7 & 6 & 8 & X & X & X \\ \text{L}_2 = & 3 & 4 & 7 & 5 & 8 & 9 & X & X & X \\ \text{L}_3 = & 6 & 7 & 8 & 9 & A & B & Y & Y & Y \end{array}$$

$$M = \begin{array}{c|cccccc|ccc} \text{No} = & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & A & B \\ \text{M} = & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 \end{array}$$

$$F(1) = \begin{array}{c|cc|c} & X_1 & X_2 & Y \\ \hline & 0 & 0 & 1 \\ & 0 & 1 & 1 \\ & 1 & 0 & 1 \\ & 1 & 1 & 0 \end{array}$$

Each column corresponds to a logical element of the circuit, and the primitives with the numbers 7, 8, 9 are the spares, which are used to replace any three of the six elements when diagnosing in them any functional failures. In the line P the primitive types are indicated, lower – the number of input and output variables; the simulation vector M contains the result of analysis for the input word 11111 of the circuit structure (see Fig. 3). The process model for generating the output values of the circuit, depending on the concatenated state of inputs, which form the address of the cell of output state, can be represented in abstract form or hardware-focused on the use of the state vector M, as follows:

$$\left[\begin{array}{l} Y_6 = P_1(X_1 * X_3); \\ Y_7 = P_2(X_3 * X_4); \\ Y_8 = P_3(X_2 * X_7); \\ Y_9 = P_4(X_7 * X_5); \\ Y_A = P_5(X_6 * X_8); \\ Y_B = P_6(X_8 * X_9). \end{array} \right] \rightarrow \left[\begin{array}{l} M_6 = P_1(M_1 * M_3); \\ M_7 = P_2(M_3 * M_4); \\ M_8 = P_3(M_2 * M_7); \\ M_9 = P_4(M_7 * M_5); \\ M_A = P_5(M_6 * M_8); \\ M_B = P_6(M_8 * M_9). \end{array} \right]$$

Here M is a state vector for circuit lines; P_i is logic function AND-NOT that has two inputs and realized as the memory element LUT. Since all of six primitive elements implement a single logic function AND-NOT then the previous expression can be simplified by replacing all the structural elements by the function primitive F with subsequent use for concatenation of two-dimensional array of lines (L) between the inputs and outputs of logic gates:

$$\left[\begin{array}{l} M_6 = F(M_1 * M_3); \\ M_7 = F(M_3 * M_4); \\ M_8 = F(M_2 * M_7); \\ M_9 = F(M_7 * M_5); \\ M_A = F(M_6 * M_8); \\ M_B = F(M_8 * M_9). \end{array} \right] \rightarrow \left[\begin{array}{l} M_6 = F[M(L_{11}) * M(L_{12})]; \\ M_7 = F[M(L_{21}) * M(L_{22})]; \\ M_8 = F[M(L_{31}) * M(L_{32})]; \\ M_9 = F[M(L_{41}) * M(L_{42})]; \\ M_A = F[M(L_{51}) * M(L_{52})]; \\ M_B = F[M(L_{61}) * M(L_{62})]. \end{array} \right]$$

4. Concatenation (#) of word bits for generating of the input stimulus $\#_{j=1}^k M(L_{ij})$ for logic element P_i ;

performing the procedure for determining the state of its output and subsequent writing into the correspondent coordinate of the modeling vector:

$$M(L_{k+1}) : M(L_{k+1}) = P_i \left[\#_{j=1}^k M(L_{ij}) \right].$$

5. Iteration of items 3 and 4 in order to obtain the states of the outputs of all the logic elements to satisfy the condition: $i = n$.

6. Iteration of items 2–4 for simulating all input test patterns to the equality: $t = \eta$, where η is length of the test.

7. The end of the simulation of digital device.

Verification of models for embedded repairing are implemented on 10 test case studies (26 – 1024 logic elements), which confirmed the fact that the cost characteristics of the hardware redundancy (x1,5–x2,5) and the reliability of combinational circuits is not worse than in the reference publications [9-12].

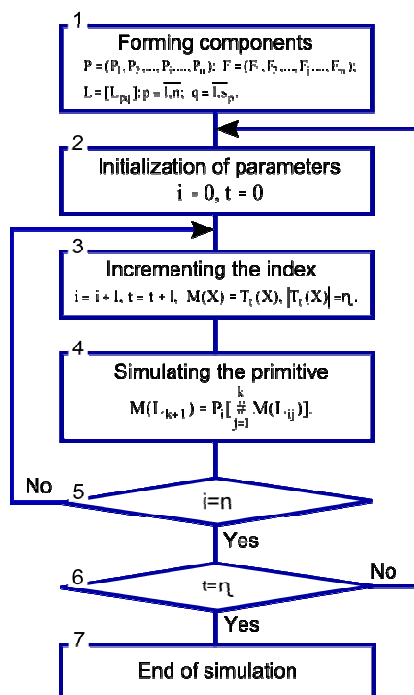


Fig. 5. Flow-chart for simulating the structure of combinational circuit

4. Conclusion

The scientific novelty lies in the following. The proposed operational and control automata for

simulating digital combinational circuits are focused on two real-world problems: 1) Embedded repairing components of combinational logic circuits by increasing the processing time of digital device and hardware redundancy for creating the infrastructure for simulating addressable elements. 2) Hardware simulating the functionalities of digital projects by using PLD, which makes it possible to substantially improve the performance of verification of software models. The practical value of the research lies in obtaining the solution of the problem of embedded repairing logic elements of the combinational circuits that makes it possible to solve the problem of autonomous repair of digital systems-on-chips due to the time and hardware redundancy of the project, which has a positive impact on the reliability of the system and its life cycle.

Areas for further research are associated with the following problems: 1) Models for switching failed primitives. 2) Parallelization of computations by levels of combinational circuit elements. 3) Replace the types and primitives of the structure. 4) Creating the operational device or infrastructure for simulating sequential elements and structures. 5) Simulating circuits consisting of functional complex primitives. 6) Development of infrastructure for embedded testing, diagnosis and repairing elements of combinational and sequential devices. 7) Testing and repairing infrastructure IT for combinational circuit is solution of the problem «watching the Watchmen». 8) Creating the analytical models for estimating the efficiency of the infrastructure IP for embedded repairing the combinational digital systems with different complexity levels of the entities and structures.

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