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Logic and Fault Simulation Based on Shared-Memory Processors

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Abstract

Existing software in Electronic Design Automation shows lack of dual-core processors support. As a result, we see bad processing resources utilization. This work-in-progress is devoted to exploration of existing approaches to parallel logic and fault simulation on dual-core workstations.

1. Introduction

The scale of modern digital system-on-chips continuously increases the complexity of testing during design and manufacturing. It makes the problem of fault simulation and automatic test pattern generation more and more relevant. The performance of fault and fault-free simulation software and the speed of workstations grow noticeably slower, than the structural and functional complexity of digital systems, or the verification cost.

In the era of embedded systems, it is easy to create complex devices using system-level approach, but at the same time it is hard to simulate, verify and test such devices. Previously, engineers used high-performance workstations to reduce simulation run time. But nowadays, microprocessors frequencies stop rising, and to solve performance problems, computers enter an era of a multi-core processing. Multiprocessors came to home and office desktops, not only to supercomputer centers. Thus, GHzs don't determine the performance of the workstation anymore. Also it's well known, that single-threaded application or serial algorithm (even best optimized for serial processing) shows no expected acceleration on multi-processor systems. In the present days, each application must be designed to gain maximum performance of multi-core architectures. This statement is a baseline of the proposed research.

The goal of research – reduce simulation run-time using efficient shared-memory processing.

Research tasks: 1) analyze existing algorithms and software products on the subject of serial and parallel data processing; 2) develop parallel algorithms for efficient shared memory utilization; 3) develop software implementation and conduct verification and testing.

2. Motivation

2.1 Forecasts and plans

In two years, Intel platforms – performance clients (desktops and mobile) and servers – will be mainly based on multi-core capability. The first processors are dual-core; a typical 2-way server with dual-core processors will support eight threads in Q1 2006. By the end of this decade, Intel expects to offer 32 threads running on an enterprise server platform (see fig. 1).

In fact, Intel is already working on a multi-core architecture that could eventually feature hundreds of execution cores in a single processor [1].

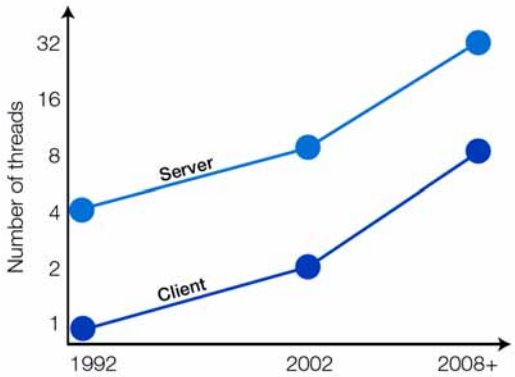

Figure 1. Intel plans on multi-core processors

2.2 Existing software

Let's see – does existing software ready for such changes?

We used Aldec Active-HDL 7.1 logic verification software to check simulation performance on single – core and dual-core workstations. In the first case we have seen 100% processor load (using Windows Task Manager). It means effective resource utilization. In the second case, we have seen only 50% of used computational resources and allocation of only one thread for logic simulation tasks.

Thus, the traditional logic simulation tool doesn't support dual-core workstation, and as a result – ineffective computational resources utilization.

3. Parallelism exploration

What is a solution for mentioned problem?

Effective utilization of multi-core processors supposes using of parallel algorithms in software. First of all, software architect need to decide: which part of algorithm should be parallelized?

There are several approaches to parallelize simulation tasks. Among them:

– process separate subcircuits in parallel;

– test sequences; different test vectors and test will be simulated in parallel;

– simulation events; scheduling and activations tasks on simulation cycles are good candidates to run in parallel;

– fault lists is a good subject for parallelization in fault simulation algorithms.

4. Practical results

Practical results were obtained using Sigetest logic and fault simulation tool [2] developed in Design Automation Department of Kharkiv National University of Radio Electronics. Its serial version was rapidly parallelized using OpenMP® library and Intel® Threading Tools.

We use third approach to parallelization – simulation events. Acceleration of simulation on dual-core workstation is about 30%. A lot of time is spent on serial scheduling and test vector applying.

Also, we noticed that software can be easily parallelized with low efforts using OpenMP library. But it can not be used in micro-optimization (folded loop and cycles), because a lot of computation time is spent on thread's creation, destroying and synchronization.

5. Future work

Our further steps will be: investigation on the related approaches to parallelization; comparing them with each other.

Also it is very interesting to apply multi-threaded technologies to different electronic design automation algorithms: test generation, synthesis, and optimization.

6. References

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