

KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2011)

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9th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2011)

Sevastopol, Ukraine, September 9-12, 2011

The main target of the IEEE East-West Design & Test Symposium (EWDTS) is to exchange experiences in the field of design, design automation and test of electronic circuits and systems, between the technologists and scientists from Eastern and Western Europe, as well as North America and other parts of the world. The symposium aims at attracting attendees especially from the Newly Independent States (NIS) and countries around the Black Sea and Central Asia.

We cordially invite you to participate and submit your contribution(s) to EWDTS'11 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level TPG
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Test
- Power Issues in Testing
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- Signal and Information Processing in Radio and Communication Engineering
- System Level Modeling, Simulation & Test Generation
- Using UML for Embedded System Specification

CAD Session:

- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless Systems Synthesis
- Digital Satellite Television

The EWDTS'2011 will take place in Sevastopol, Ukraine. Sevastopol is a port city, located on the Black Sea coast of the Crimea peninsula. The city, formerly the home of the Soviet Black Sea Fleet, is now home to a Ukrainian naval base and facilities leased by the Russian Navy and used as the headquarters of both the Ukrainian Naval Forces and Russia's Black Sea Fleet.

The symposium is organized by Kharkov National University of Radio Electronics in cooperation with Sevastopol National Technical University and Tallinn University of Technology. It is technically co-sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Virage Logic, Synopsys, Aldec, Kaspersky Lab, DataArt Lab, Tallinn Technical University, Cadence.



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Infrastructure for Testing and Diagnosing Multimedia Devices

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Abstract

In this paper HW/SW systems testing and faults diagnosing approach is described, also method for effective faults detection and defects localization within the system-under-test is proposed.

1. Introduction

Essential increase of consumer requirements for complex electronic devices leads to substantial growth of complexity for HW and SW components, services, and system interfaces. Such tendency increases the importance to provide high quality for HW, SW, and networking components and services. One of the main goals which comes to the foreground of industry is to decrease the cost of exploitation by creating the standardized infrastructures for maintenance which providing service exploitation, testing, disposal and, elimination of functional defects. Well known rule of ten for hardware components stating that fault detection cost increases in ten times on the next following design or manufacturing stages. Nowadays fast growing complexities of hardware is transforming this rule into rule of twenty which makes even more important to detect the fault on early design stages, rather than on chip/PCB manufacturing, or system assembling stages [1].

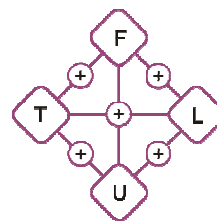
Goal of this work is to develop method which increases product quality by means of developing sufficient HW/SW test and diagnosis approach, also decreasing faults detection and defects localization time in order to improve system performance on example of multimedia devices.

2. Components interconnection technology tests model

In this thesis proposed model of tests generating, faults modeling, and defects localization based on xor-dependencies of four main components or characteristics of

the system: $G=(F, U, T, L)$, where: F – functionality under test, U – unit under test, T – functional test, L – faults and defects coverage.

Such components of technical diagnosis are interconnected in the way, represented on the figure 1 and can be described with four possible equations listed below. These equations represent complete set of interconnections which are forming the goal of technical diagnosis [2].



- 1) $T \oplus F \oplus L = 0$
- 2) $T \oplus L \oplus U = 0$
- 3) $T \oplus F \oplus U = 0$
- 4) $F \oplus L \oplus U = 0$

Figure 1. Technical diagnosis components interconnection schema

This model allows generalizing and classifying areas of technical diagnosis using xor-dependency for four key elements. This paper describes only the first equation which represents test, functionality, and defects coverage interconnection.

From equation $T \oplus F \oplus L = 0$ the next identities are following:

- 1) $T = F \oplus L$ - Tests generation, using the functionality model for the specified faults list.
- 2) $F = T \oplus L$ - Functionality model based on the specified test and the faults list.
- 3) $L = T \oplus F$ - Synthesis of the faults list of the specified functionality based on the specific test.

HW design effectiveness E can be defined by average and restricted integral criteria in the interval $[0,1]$:

$$E = F(L, T, H) = \min\left[\frac{1}{3}(L + T + H)\right],$$

$$Y = (1 - P)^n; L = 1 - Y^{(1-k)} = 1 - (1 - P)^{n(1-k)};$$

$$T = [(1 - k) \times H^S] / (H^S + H^a); H = H^a / (H^S + H^a).$$

Above is described the level of product errors L , verification time T , SW/HW redundancy, defined by assertion mechanism and maintenance instruments H .

Level of production errors is characterized by Y – yield and depends on k – product testability, P – existing probability of the defect, and the number of not detected errors – n . Verification time is defined by product testability k multiplied by the structural HW/SW complexity and divided by general complexity of the product measured in SW code strings. HW/SW redundancy is dependant on assertions code complexity and other redundancies related to general code complexity. At the same time HW/SW redundancy should provide required level of functional defects diagnosis during yield's time to market defined by customer.

3. Multi-matrix processor of binary operations

Multi-matrix processor (MMP) is the minimal architecture of instructions targeted for parallel execution of single (and, or, xor, slc) operations with dedicated 2D array. Quantity of operation-related single arrays defines heterogeneous MMP of binary operations with buffer M (figure 2) [2]

Standard blocks: DM – Data module, PM – Program module, CU – Control unit, I-face interface and I-IP service module, MMP – Multi-matrix processor module. The scheme includes four memory blocks with A – and, B – xor, C – or, D – slc (shift left crowding) operations, and buffer memory M . MMP directed to perform one of four instructions (ISA – Instruction Set Architecture) that operates with binary matrix and same dimensions and stores results into buffer M :

$$M = M \{ \text{and, or, xor, slc} \} \{ A, B, C, D \}$$

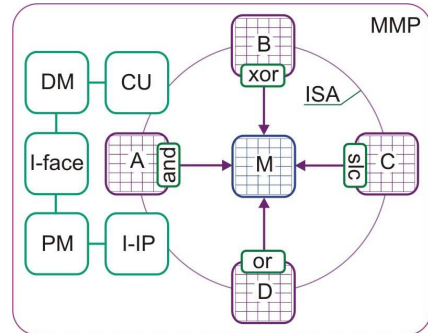


Figure 2. Multi-matrix processor of binary operations

Basing on MMP approach there was created infrastructure for UUT verification which is modification of I-IP standard 1500 [3, 4, 5]. On the figure 3 three process models for testing, faults detection and diagnosis, performance recovering are presented.

4. Method of Functional Violation

The analytic model verification based on temporal assertions is targeted for reaching required depth of diagnosis. The search of functional violation (FV) is based on xor-operation definition between the state of assertion (vector m) and the columns of FV table:

$$m \oplus (B_1 \vee B_2 \vee \dots \vee B_j \vee \dots \vee B_n)$$

$$B = \min_{j=1,n} [B_j = \sum_{i=1}^p (B_{ij} \oplus m_i)],$$

where

$$m = f(A, B) \oplus f^*(A, B, L)$$

The result of test experiment – comparing outputs states of golden sample $f(A, B)$ and actual $f^*(A, B, L)$ – UUT with defects L of test combination A .

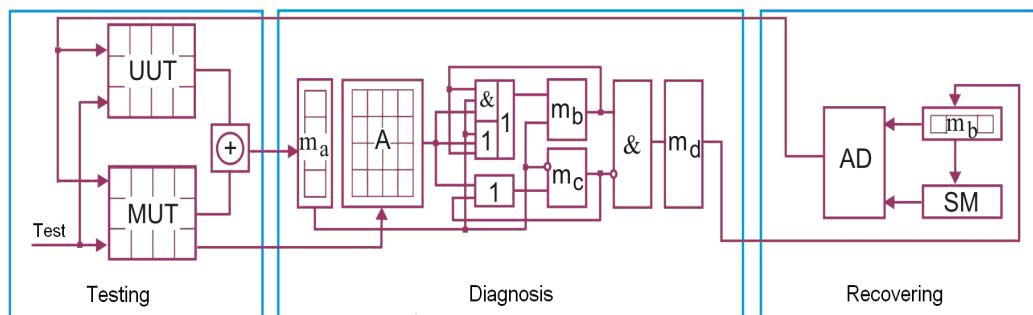


Figure 3. Testing, diagnosis, recovering process models

5. Functional blocks tree view

Figure 4 represents functional blocks tree view hierarchy for digital satellite receiver. Schema represents

the top list of the most occurring SW/HW faults and potential root-causes for specified faults. Chart represents 3-level hierarchy; however levels can be extended and decreased for better localization.

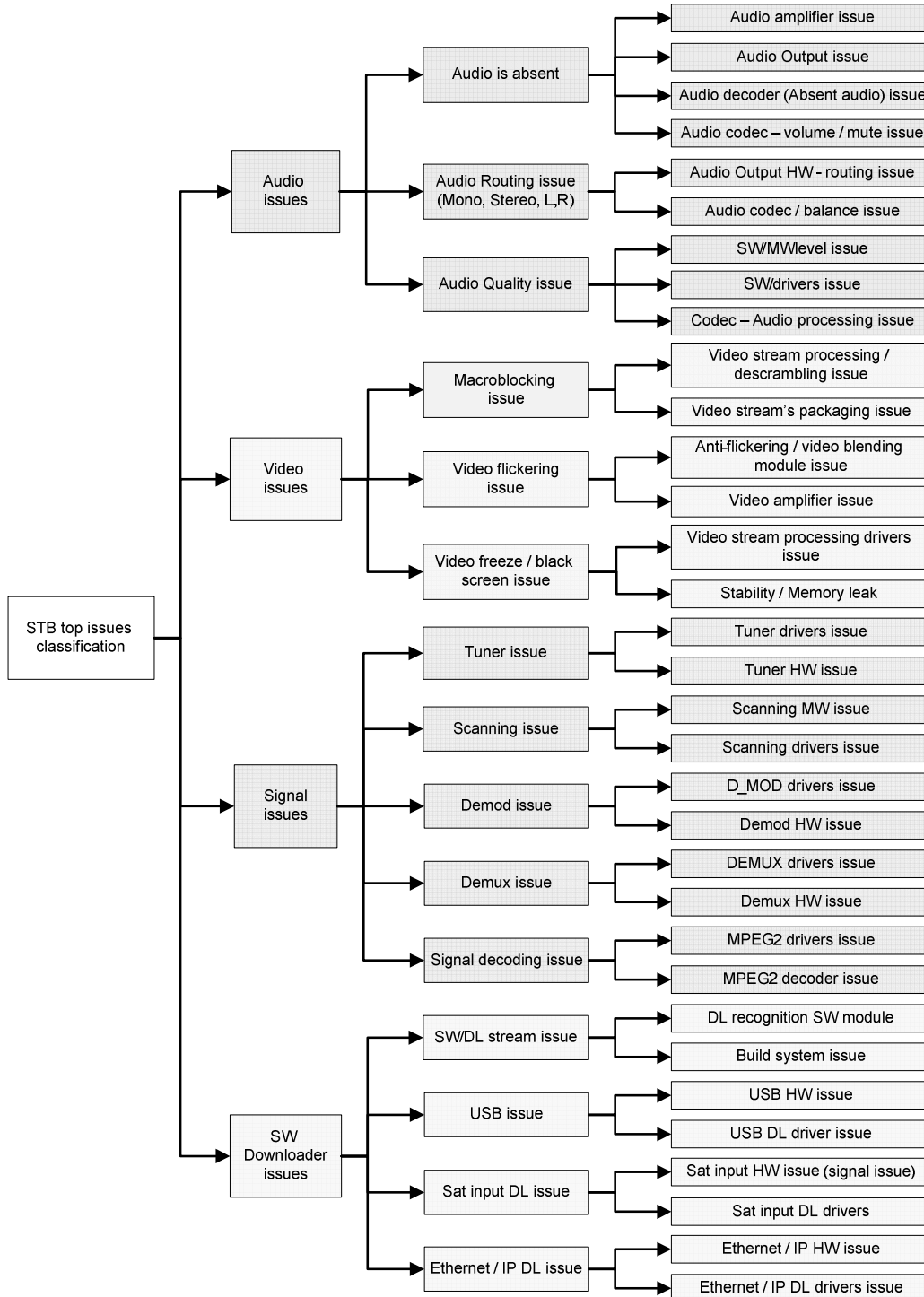


Figure 4. Digital satellite receiver tree-view hierarchy

6. Hierarchical testing process

Generic 3-level representation of tree view hierarchy is shown on the figure 5. Specific test sequence T_{ij} is applied to certain level of functional hierarchy. After testing is complete the result is being analyzed. If fault is detected, system returns block identifier B_{ij} with error description. Also there is considered false block automated reparation possibility R_{ij} . After fault detection and reparation the system should be retested from the very beginning [2, 6].

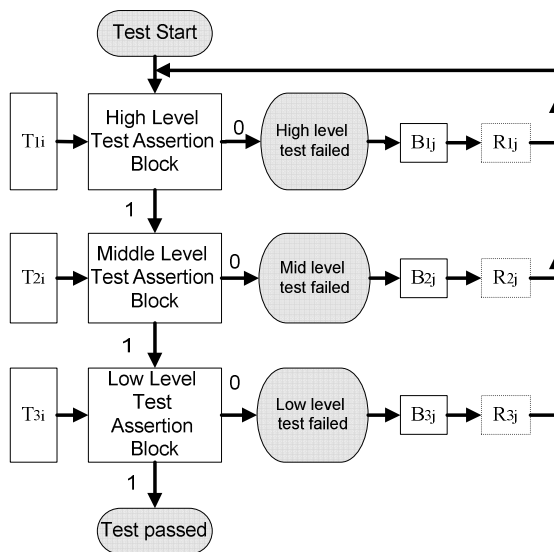


Figure 5. 3-level hierarchical testing process

7. Assertion based coverage graph

The analytic model verification, based on temporal assertions is targeted for reaching required depth of diagnosis and can be represented in the next way:

$$M = f(F, A, B, S, T, L), \quad F = (A * B) \times S; \quad S = f(T, B);$$

$$A = \{A_1, A_2, \dots, A_i, \dots, A_n\}; \quad B = \{B_1, B_2, \dots, B_i, \dots, B_n\};$$

$$S = \{S_1, S_2, \dots, S_i, \dots, S_m\}; \quad S_i = \{S_{i1}, S_{i2}, \dots, S_{ij}, \dots, S_{ip}\};$$

$$T = \{T_1, T_2, \dots, T_i, \dots, T_k\}; \quad L = \{L_1, L_2, \dots, L_i, \dots, L_n\}.$$

$F = (A * B) \times S$ is represented by code-flow transaction graph - CFTG, or Assertion-Based Coverage Graph - ABC Graph, where

$S = \{S_1, S_2, \dots, S_i, \dots, S_m\}$ representing states of the HW/SW product while modeling test-segments.

Each state S is defined by functional key variables; chart chords are represented by functional blocks B , where

$$B = (B_1, B_2, \dots, B_i, \dots, B_n), \quad \bigcup_{i=1}^n B_i = B; \quad \bigcap_{i=1}^n B_i = \emptyset$$

Every block B can be verified by the assertion A , where

$$A_i \in A = \{A_1, A_2, \dots, A_i, \dots, A_n\}.$$

Every chord B_i represents the state $S_i = f(T, B_i)$, which is also dependant on the test sequence $T = \{T_1, T_2, \dots, T_i, \dots, T_k\}$.

Every state S is supplied with the Assertions Monitor

$$A(S_i) = A_{i1} \vee A_{i2} \vee \dots \vee A_{ij} \vee \dots \vee A_{in}.$$

The out-coming functional violation blocks multitude is represented with the list $L = \{L_1, L_2, \dots, L_i, \dots, L_n\}$.

For the functional block diagram, represented on the figure 4, the functional defects matrix is presented in Table 1 which covers all hierarchical (or activation levels).

Below there are presented the requirements for functional defects table definition:

1. The number of tests T should stay minimal, $|T| \rightarrow \min$,
2. To exclude equivalent defects vectors additional tests should be added to guarantee unique state for every defects vector, $|T_{new}| = |T| + t$, where t – minimal required additional number of the test vectors to guarantee defects vector unique state condition.
3. Diagnosability function is dependant on the test length T , number of assertions A and the number of functional blocks N ; at the same time diagnosability function should always tend to 1 [2, 3].

$$D = 1 \rightarrow \frac{|T| \times |A|}{\lceil \log_2 N \rceil} = 1 \rightarrow \lceil \log_2 N \rceil = |T| \times |A|$$

Basing on diagnosing procedure and the matrix of functional defects faulty components can be defined by analyzing functional defects table rows. For the functional defects matrix the next transaction graphs can be created, represented below (figure 6).

Table 1. Matrix of functional defects

1 st activation level					
	Audio	Video	Signal	SW Downloader	V
T_1	.	1	1	.	0
T_2	1	.	1	1	1
T_3	1	1	.	.	1
T_4	.	1	1	1	0

2 nd activation level				
	Signal inaccessible	Routing	Quality	V
T_1	1	1	1	1
T_2	1	1	.	0
T_3	1	1	.	0
T_4	.	1	1	1
T_5	.	1	1	1

3 rd activation level				
	SW/MW level	Codec - audio processing	SW/Drivers	V
T_1	1	.	1	0
T_2	1	1	.	1
T_3	.	1	1	1

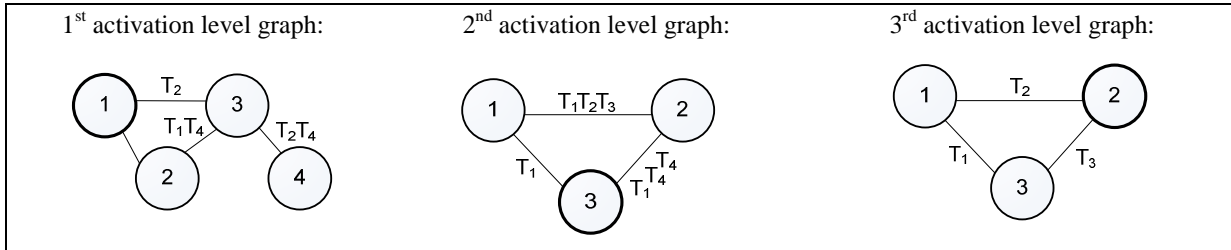


Figure 6. Code-flow transaction graph

8. Multi-level model for diagnosing digital systems

Multi-level model can be presented in a tree-like view B , where every vertex can be represented as a 3-dimensional functional modules activation table and arcs are representing navigation to lower diagnosis levels for the cases when functional block's defect was detected:

$$B = [B_{ij}^{rs}], \text{card}B = \sum_{r=1}^n \sum_{s=1}^{m_r} \sum_{j=1}^{k_{rs}} B_{ij}^{rs},$$

where n – number of multi-tree levels; m_r - number of the functional blocks and components on r level; k_{rs} - number of components in the B^{rs} table; $B_{ij}^{rs} = \{0,1\}$ - component of activation table which is defined by the test vector T_{i-A_i} applicable to the observing monitor A_i .

Multi tree-like model can be described in the way presented on the figure 7.

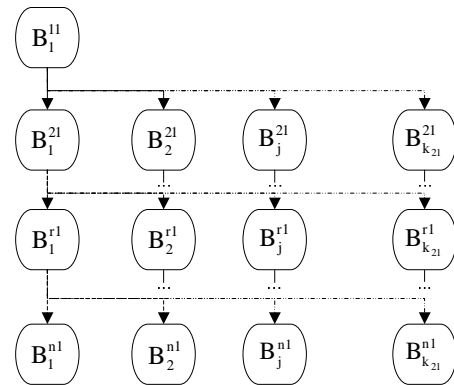


Figure 7. Multi tree-like model

Defects detection model is based on top-to-bottom navigation to the required detailing level:

$$B_j^{rs} \oplus A^{rs} = \begin{cases} 1 \rightarrow \{B_j^{r+1,s}, R\}; \\ 0 \rightarrow \{B_j^{r+1,s}, G\}. \end{cases}$$

Navigation approach is based on xor-operation between matrix rows B and experimental verification vector based on assertions obtained from monitors during all test segments activating process.

If the xor-sum equals 1 (fault detected), then algorithm assumes two possible actions: 1) to navigate to the next activation matrix level or 2) system repair R. The decision is based on execution time vs. repair cost importance.

If the xor-sum is 0 (no faults detected) then algorithm moves to the next activation matrix level $B_j^{r+1,s}$ with good quality status G.

Detailed diagnosis algorithm for multi-tree navigation is presented on the figure 8.

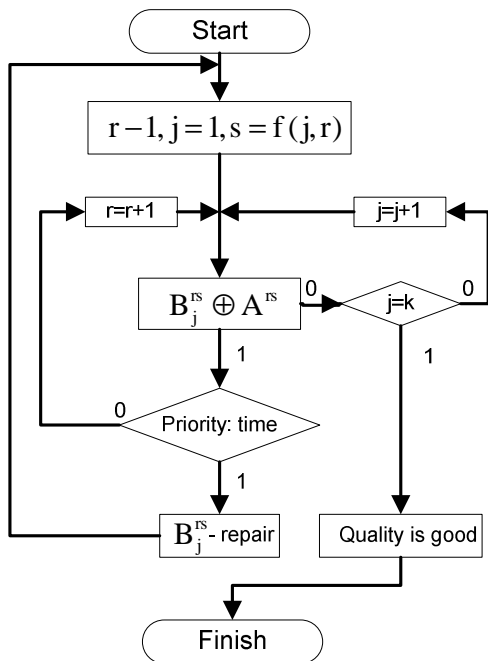


Figure 8. Multi-tree navigation algorithm

9. Conclusions

This paper represents faults detection and localization technique. Described models and algorithms providing possibility to perform effective service for complex digital SW/HW systems.

Benefit for such approach is in simplicity of technical information representation and diagnosing preparation, based on minimized activation table applied to HW/SW system-under-test and in particular to functional blocks segments testing which are invariant to hierarchy levels.

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Camera-ready was prepared in Kharkov National University of Radio Electronics
Lenin Ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 26.08.2011. Format 60×841/8.

Relative printer's sheets: 42. Circulation: 150 copies.

Published by SPD FL Stepanov V.V.

Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозиуму «Схід-Захід Проектування та Діагностування – 2011»
Макет підготовлено у Харківському національному університеті радіоелектроніки

Редактори: Володимир Хаханов, Світлана Чумаченко, Євгенія Литвинова

Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 26.08.2011. Формат 60×84¹/₈.

Умов. друк. Арк. 42. Тираж: 150 прим.

Видано: СПД ФЛ Степанов В.В.

Вул. Ак. Павлова, 311, Харків, 61168, Україна