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Hierarchical Systems Testing based on Boundary Scan Technologies

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Abstract

We propose models of complex program-technical systems testing; these models solve diagnosis tasks in real time. Models use IEEE standard boundary scan technologies to observe internal lines, and methods of testability evaluation to define critical places in digital objects. Models and methods are oriented to test distributed control systems of critical technologies.

1. Introduction

Basic requirements for modern informational and control systems for complex objects and critical technologies [1-5] are: 1) provide high reliability during operation [5]; 2) online monitoring and control of all the parameters of critical system of object; 3) testing, diagnostics and repair in technically and standard acceptable time; 4) provide desired diagnosis depth of system or its components, automatically and in real time.

New generation of modern technologies and design flows introduces additional criteria, related to design, manufacture and operation of digital devices: time-to-market, Design-for-Manufacturability, Testability, Diagnosis, Verification [6-8]. Major design stage is verification process, aimed to eliminate all design errors on the early stages; it leads to considerable time and costs savings. Acceptable testable overhead (assertion), added at early design stage, is interesting here, because it considerable decreases main parameter – time-to-market, using verification and testing methods; it is very urgent and attractive design model [2-4, 10].

Talk is about use of verification test, obtained at system design stage, to check device with minimal additional hardware and software expenses using boundary scan technologies [6, 9]. At the same time, hardware/software overhead mechanism must include additional control points, which must be introduced into design using Boundary Scan Register of special (ad-hoc) technologies at synthesis stage. As a result, design redundancy created once maybe used many times to check components of digital system during all stages of its lifecycle.

At present, complex digital devices are considered as objects with several levels of hierarchy. At the lowest level, system is represented as a set of modern integrated circuits (PLD, ASIC), which implements SoCs, NoCs, memory, processors. Second level is formed by system on boards, where integral circuits are represented as primitives. Third level represents set of boards, which integrated into crates. Fourth level combines set of crates or boxes into complex distributed control system of technological process, manufacturing or critical technologies (aviation, cosmonautics, nuclear-power engineering, meteorology, defense, ecology) [5]. Fifth level may be considered as geographically distributed system, e.g. Internet. In this research, we consider from first to fourth levels of hierarchy, in order to creation of models and methods of its testing with defined diagnosis depth.

Research objective – considerable decrease of complex digital system testing time during operation based on creation of general model of organization and execution of diagnostic experiment, including unconditional algorithms of faults finding using IEEE standards of testable design [6-9].

Research problems: 1) choosing appropriate methods and tools for testing of all mentioned levels of hierarchy; 2) development of hierarchical model of organization and execution of diagnostic experiment, including conditional and unconditional algorithms of faults finding, oriented to testable design standards; 3) practical implementation of complex digital devices testing models and experimental evaluation.

2. Digital system testing model

Object of inquiry – digital control system, represented as several levels of hierarchy, designed using IEEE testable design standards. Especially, we consider program-technical complex F, as unit-under-test, which can be represented as tuple: $F = \langle C,B,P,M \rangle$, where $C = \{c_1,c_2,...,c_n\}$ – finite nonempty set of crates in digital system, $B = \{b_1,b_2,...,b_m\}$ – set of boards in crate, $P = \{p_1,p_2,...,p_k\}$ – set of integral circuits on board, $M = \{m_1,m_2,...,m_g\}$ – set of functional IP-Cores on chip (integrated circuit). At the same time, following conditions of folding or hierarchy are true:

$$m_{ijrs} \in p_{ijr} \in b_{ij} \in c_i \in F, (i=\overline{1,n}; j=\overline{1,m}; r=\overline{1,k}; s=\overline{1,g}) \quad (1)$$

General equation of diagnosis for considered object of research maybe represented as following:

$$D = R^* \wedge L = (R^+ \oplus R^-) \wedge L = [(T \oplus F) \oplus (T \oplus F^*)] \wedge L \quad (2)$$

where formula's parameters are defined as: D – set of detected faults during testing; $L(T_i)$ – fault list, detectable by test pattern $T_i \in T = (T_1,T_2,...,T_i,...,T_h)$, represented in the form of table

$$L(t_i) = [L_{ij}], i=\overline{1,p}; j=\overline{1,q},$$

where each test is associated with subset of detectable faults, p – number of observed outputs, q – whole number of lines; $R^-(T_i) = (R_1^-,R_2^-,...,R_i^-,...,R_p^-)$ – binary vector of experimental check (VEC), equal to number of observed outputs; $R^+(T_i) = (R_1^+,R_2^+,...,R_i^+,...,R_p^+)$ – reference vector of outputs' states; F – reference device model; F* – real device.

For diagnosis process organization, vector $R^*(T_i) = (R_1^*,R_2^*,...,R_i^*,...,R_p^*)$ is formed correspondingly to the following rule:

$$R_i^* = R_i^+ \oplus R_i^-. \quad (3)$$

Ideal model for fault diagnosis is represented as the following structure: $F = \{T \times L \times R\}$. But complexity of such 3D table is defined as: $|F| = h \times 2q \times p$. .

If test's dimension, in the best case, is square of number of lines, then this equation transforms to the following: $|F| = \{q^2 \times 2q \times p\} = 2q^3 p \approx q^4$. If number of lines is from 100 000 to 1 000 000, then power of diagnosis table will be in interval $10^{20} \ge |F| \ge 10^{24}$. Naturally, such amount of diagnostic information is impossible to process to find fault in digital system. Data compression problem has occurred. In fact, we can compress all of three components {T, L, R} [11]: test, fault lists, output responses, but at the same time we loose diagnosis accuracy or diagnostic experiment time. Further, we propose diagnosis method with maximum possible diagnosis depth, based on real-time diagnostic experiment, when we can exclude parameter T, and whole data can be represented as 2D table, because we lost test length information. We propose the following diagnostic model:

$$1) \begin{cases} L(T_i) = F \oplus T_i; \\ R^*(T_i) = f(F,T_i,D^*); \\ D(T_i) = g[L(T_i),R^*(T_i)]. \end{cases}$$

$$2) \begin{cases} D^s(T_i) = \underset{\forall j(R_j^*=1)}{\wedge} L_j \& \overline{\underset{\forall j(R_j^*=0)}{\vee} L_j}; \\ D^m(T_i) = \underset{\forall j(R_j^*=1)}{\vee} L_j \& \overline{\underset{\forall j(R_j^*=0)}{\vee} L_j}. \end{cases} \quad (4)$$

$$3) \begin{cases} D_0^s(T) = D_0^s(T) \vee D^s(T_i) \& S^+(T_i); \\ D_1^s(T) = D_1^s(T) \vee D^s(T_i) \& \overline{S}^+(T_i). \end{cases}$$

$$4) \begin{cases} D_0^m(T) = D_0^m(T) \vee D^m(T_i) \& S^+(T_i); \\ D_1^m(T) = D_1^m(T) \vee D^m(T_i) \& \overline{S}^+(T_i). \end{cases}$$

First three equations present procedures: forming detectable fault lists; calculating output responses; detecting actual faults during real experiment. Second equations system allows defining single or multiple stuck-at faults by executing two operations on the fault table L, detectable by input sequence T_i and vector of experimental check R*. Third equations system allows calculating vector of single faults, detected during test process, as function of fault-free vector $S^+(T_i)$ and complete test T. Fourth equations system allows collecting multiple faults into vector, detected during test process, also as function of fault-free vector $S^+(T_i)$. The real-time diagnostic experiment result is set of single or multiple faults, detected in digital system. At the same time, memory consumption is:

$$Q^M = (p^x \times q^2) + (q \times p) + 7q + 3p. \quad (5)$$

If we use built-in test pattern generator, so it is no need to store test data, then amount of memory will be minimal:

$$Q_A^M = (q \times p) + 7q + 3p. \quad (6)$$

Naturally, computational complexity is function of memory consumption, provided with (5) and (6).

Fig. 1 represents structure of processor to perform diagnostic experiment, which built on equations (4).

Advantage of this processor is ease of performing table and vector operations, which can be implemented both in computer and PLD.

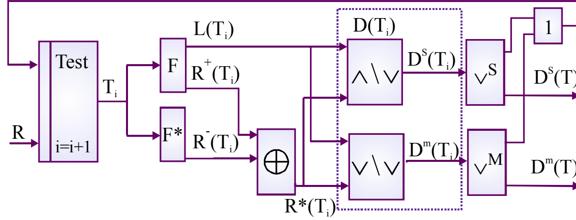

Figure 1. Structure model of digital system diagnostics

As data structures example, necessary to perform the diagnostic experiment, we show tables and vectors to illustrate procedures, defined by mentioned processor (fig. 1) and equations (4):

$$L(T_i) = [L_{ij}] \quad q = 8 \quad R^*(t) = R^-(t) \oplus R^+(t)$$

$$p = 4 \qquad \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&1&0&1&1&1&1\\ \hline 0&0&0&1&0&0&0&0\\ \hline 1&1&1&1&0&1&0&1\\ \hline 0&0&1&0&1&1&0&1\\ \hline \end{array} \quad \begin{array}{|c|}\hline 1\\ \hline 0\\ \hline 1\\ \hline 0\\ \hline \end{array} \quad \begin{array}{|c|}\hline 0\\ \hline 0\\ \hline 1\\ \hline 1\\ \hline \end{array} \quad \begin{array}{|c|}\hline 1\\ \hline 0\\ \hline 0\\ \hline 1\\ \hline \end{array}$$

$$D^s(T_i) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&0&0&0&0&0&0\\ \hline \end{array}$$

$$D^m(T_i) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&0&0&0&0&1&0\\ \hline \end{array}$$

$$S^+(T_i) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&0&0&1&1&0&0\\ \hline \end{array}$$

$$D_0^s(T) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&0&0&0&0&0&0\\ \hline \end{array}$$

$$D_1^s(T) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 0&0&0&0&0&0&0&0\\ \hline \end{array}$$

$$D_0^m(T) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 1&1&0&0&0&0&0&0\\ \hline \end{array}$$

$$D_1^m(T) = \begin{array}{|c|c|c|c|c|c|c|c|}\hline 0&0&0&0&0&0&1&0\\ \hline \end{array}$$

Here we consider unit under diagnostics, having 4 outputs (p=4) with associated fault list, equal to number of lines (q=8). Detectable fault is identified with 1, undetectable one – with 0. Type of stuck-at fault is defined by inverted fault-free value of corresponding line in $S^+(T_i)$. Values of vector of experimental check are calculated as XOR function of two vectors: fault free $R^+(T_i)$ and actual results $R^-(T_i)$ of real unit-under-test. Thus, one (zero) value of vector $R^*(Ti)$ identifies coincidence (non-coincidence) of pattern and real responses. At the same time, we use two strategies: searching for single and multiple faults on each test-vector, shown by vectors $D^s(T_i), D^m(T_i)$ correspondingly. Saving of information is performed separately in vectors $D_0^s(T), D_1^s(T), D_0^m(T), D_1^m(T)$, which form single and multiple fault lists. Equations (3) and (4) are used.

Thus, for hierarchically complex digital system, it is more economically to execute diagnostic experiment in real-time. In this case, it is necessary to store information about output responses and fault simulation results.

3. Testing using IEEE standards

Main disadvantage of existing design methods and flows [20-22] is inability to insert self-testing hardware overhead. At the same time, overhead requires additional timing and money costs. Nevertheless, developers are trying to follow modern requirements and to comply to IEEE testable design standards. What do mentioned standards give in the view of test process and diagnostic result for complex hierarchical systems? Naturally, effectiveness criterion is considered: diagnostics time with desired quality, defined by fault location depth.

Existing methods have time-consuming and high-cost elementary checks, which help to identify type and location of fault in system. The best solution is to use unconditional experiment, which removes uncertainty of testing and diagnosis defining by including additional observation points based on existing IEEE standards.

Which lines do need additional observation? Such lines, that allow splitting equivalent faults [23] and make them diagnosable. E.g., if number of observable outputs is p, and test length is h, then q is number of detected faults and it is defined by the following equation:

$$q = 2^{p \times h} \quad (p \neq 0, h \geq 2) \qquad (7)$$

But equivalent faults may be your best friend in huge designs with millions of gates. They may decrease size of test (parameter h), but also they make diagnostic properties very bad. To recover mentioned property, it is necessary to increase parameter p in equation (7). Thus, additional observable internal lines increase diagnostic depth.

CAMELOT ideology [8, 13] is used to find additional observable lines. They are defined by calculation of observability $O(X_i)$ for each internal variable. Then we need to select a set of such lines X_i provided that predefined value of observability is reached:

$$X_i \in Y \leftarrow [O(X_i) \leq \{O_{max}, T^*_{max}\} \vee X_i \in R]. \quad (8)$$

It is necessary to exclude all input lines from set Y. Moreover, it is necessary to calculate controllability, observability and testability for each line. Thus, testability evaluation methods give ability to find bottlenecks in design in the view of controllability, observability and testability. Further, IEEE Boundary Scan Standards 1149.1 and IEEE P1500 [6,9] make

lines observable (controllable), due to scan technologies.

As to hierarchy of design, its structure may be represented as tree, where each node – component in relation to the higher level of hierarchy – having one input arc and several outgoing (see fig. 2).

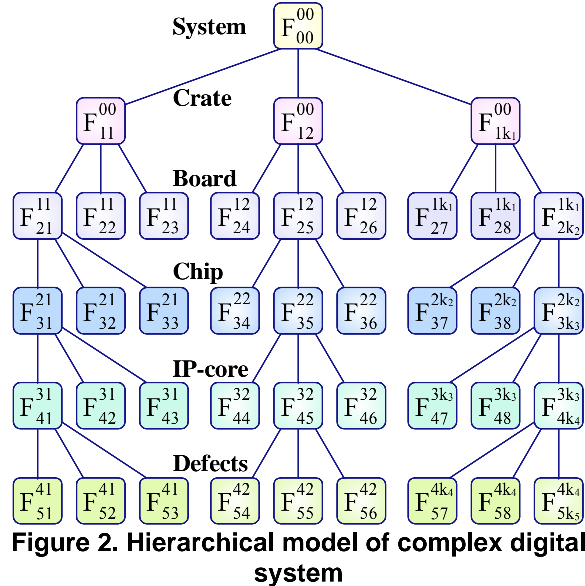

Figure 2. Hierarchical model of complex digital system

Mathematical model of such hierarchy is represented as equations system:

$$\begin{cases} F=\left[F_{ij}^{rs}\right],\ (i=\overline{0,5};\ j=\overline{1,k_j};\ r=\overline{0,4};\ s=\overline{1,k_{j-1}}); \\ T=\left[T_{ij}^{rs}\right];\ L=\left[L_{ij}^{rs}\right]; \\ F_{ij}^{rs}\oplus T_{ij}^{rs}=L_{ij}^{rs}. \end{cases} \quad (9)$$

Complete identifier of system's component $F=\left[F_{ij}^{rs}\right]$ has four indexes. Lower indexes (ij) are used to identify level of hierarchy and number of component. Upper indexes are used to identify relation to parent node.

There are two testing strategies. First one uses functional test, which allows defining unit's fault. Only at the lowest level, test gives fault list. The second strategy is more intellectual due to complex and huge diagnostic tests. Testing of current component gives exact fault's address.

Test of higher level identifies faulty components of one lower level:

$$\begin{aligned} F_{1j}^{rs}\oplus T_{1j}^{rs} &= L_{1j}^{rs}=\{L_{21}^{1j},L_{22}^{1j},...,L_{2k_j}^{1j}\}; \\ F_{2j}^{rs}\oplus T_{2j}^{rs} &= L_{2j}^{rs}=\{L_{31}^{2j},L_{32}^{2j},...,L_{3k_j}^{2j}\}; \\ F_{3j}^{rs}\oplus T_{3j}^{rs} &= L_{3j}^{rs}=\{L_{41}^{3j},L_{42}^{3j},...,L_{4k_j}^{3j}\}; \\ F_{4j}^{rs}\oplus T_{4j}^{rs} &= L_{4j}^{rs}=\{L_{51}^{4j},L_{52}^{4j},...,L_{5k_j}^{4j}\}. \end{aligned} \quad (10)$$

One more test generation strategy: for each IP-core single stuck-at fault test is generated. Then, already generated tests are combined with upper level tests.

Following cooperation strategy of boundary scan technology with hierarchical object model illustrates accessibility to inputs and outputs of each component during diagnostic procedure (see fig. 3).

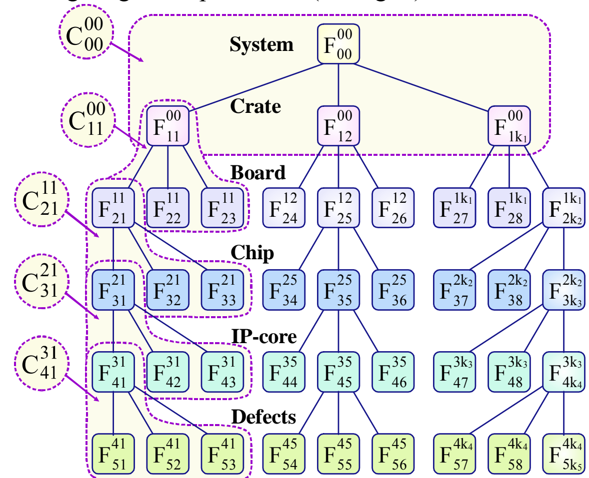

Figure 3. BS-wrapper of hierarchical model of digital system

Model of B/S-controller is universal in relation to parent node and nearest components-successors:

$$F_{ij}^{rs}=\{F_{i+1,1}^{ij},F_{i+1,2}^{ij},...,F_{i+1,k_j}^{ij}\}. \quad (11)$$

E.g., controller: $C_{31}^{21}\approx F_{31}^{21}=\{F_{41}^{31},F_{42}^{31},F_{43}^{31}\}$, see fig. 3, scans data in the one chip, containing three IP-cores: $\{F_{41}^{31},F_{42}^{31},F_{43}^{31}\}$. Applying equation (11) to system's model (see fig. 4), we may obtain hierarchical structure of B/S-controller, represented at fig. 4.

Hardware overhead of B/S testing system is 2-5% of whole functional component, which is acceptable for modern chip sets of companies like Xilinx and Altera. Performance overhead is no more than 0,5%. There is time consumption during diagnostic experiment. It can be calculated using equation:

$$Q(F)=\sum_{j=1,5} k_j\times p_j\times t^*. \quad (12)$$

k_j – number of boundary scan registers at k-level of hierarchy, p_j – number of latches in register of j-level of hierarchy, t* – information shift time. For 1 000 000 gates design, number of observable lines may be up to 1 000. In such case hardware overhead will be 2,1%, testing speed will be reduced in 1 000 times and will be not greater than 100 msec/test-vector.

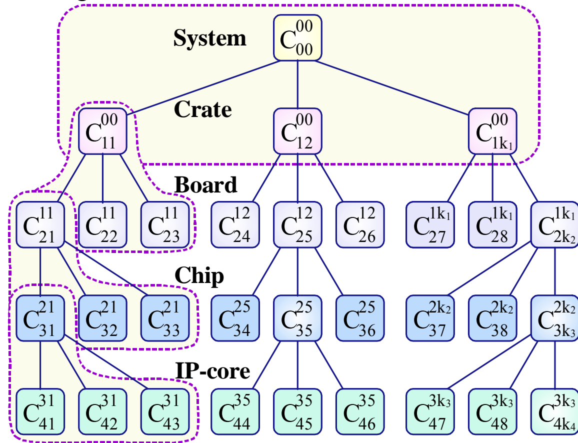

Figure 4. Hierarchical structure of B/S-controllers of complex system

Main idea of boundary scan standards is ease of control and observation of internal lines by using hardware overhead in form of Boundary Scan Register and Test Access Port controller. Typical B/S-structure is shown at fig. 5. Integrated circuit is divided into separate modules; tests and diagnostic algorithms are generated for them.

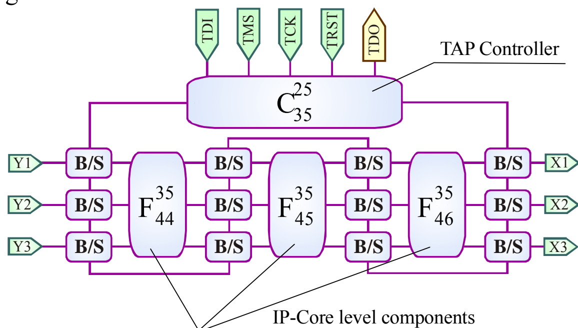

Figure 5. IEEE scan's standards circuit

General test process model is shown at fig. 6.

Principles of testing system organization:

1) Use the most appropriate IEEE standards [6-9] for verification of components on the current level of hierarchy;

2) Determine given depth diagnosis automatically, without using of conditional defect finding algorithms;

3) Only single component may be faulty;

4) Testing procedure after repair begins from the top level to low level of hierarchy – descending diagnosis;

5) Testing procedure may begin from any level of hierarchy and may finish on the desired level by engineer.

Suggested testing model detects single fault and at least one multiple fault [8,12].

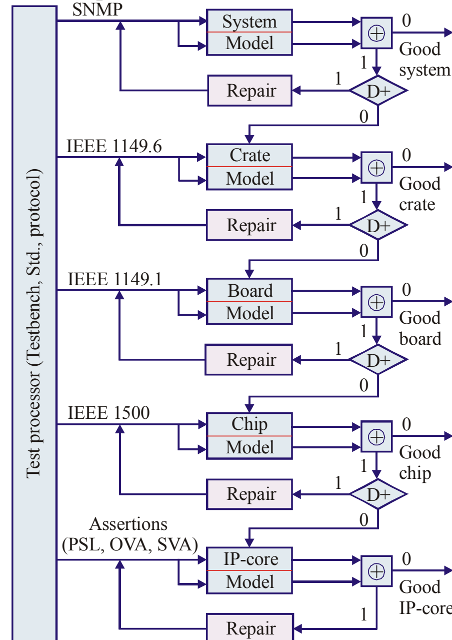

Figure 6. Testing structure for digital system

4. Conclusions

During current research international IEEE standards are considered, which are suitable for testing and diagnosis of program-technical complexes and broad range of electronic system: starting with components inside IC, ending with complex systems, consisting of boards and crates.

Considered IEEE standards 1149.1, 1149.4, 1149,6 and 1500 offer wide ability for solving tasks: component functional testing; interconnection testing; system on board functional testing; system on crate functional testing.

Units under test are: analog components; digital components; mixed components; discrete elements; printed circuit boards, consisting of mentioned components.

Scientific novelty of obtained results lies in using of ad hoc technologies, combining existing IEEE testability standards with specialized schematic solutions, which allow reducing in several times testing and diagnosis time of complex digital systems [11]:

1) Analytic and structure diagnostic models are presented aimed to real-time experiments using fault simulation;

2) Unit-hierarchical testing method is developed. Main idea is to represent system as hierarchy of simpler components. For this model, network of boundary scan registers is developed.

3) Suggested diagnostic method considerable decrease diagnostic information.

Thus, Boundary Scan technologies allow designers to meet the modern requirements and tendencies during design, verification, debug, manufacturing, testing, embedded software design and operation of different systems. Compliance of final software or hardware product to the international IEEE standards – is a guarantee of successful distribution on the world market.

Practical importance lays in significant (50-70%) decrease of time for fault identification by using IEEE testability standards [5-7, 9]. At the same time, diagnostic depth is increased on 10-30% (fig. 7) with increased observability on 3%.

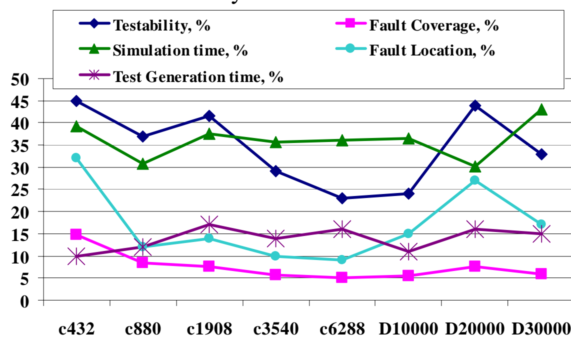

Figure 7. Digital system characteristics improvement

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