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HIERARCHICAL HYBRID APPROACH TO COMPLEX DIGITAL SYSTEMS TESTING

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Abstract. This paper offers approach to complex digital system testing based on hierarchy scaling during diagnosis experiment. Several models of testing are proposed. Main principles of testing system organization are given. Such approach allows significant reducing overall system testing and verification time.

Keywords: Testability, testing, diagnosis, standards, program-technical complex.

1. Introduction

Complex digital devices nowadays are considered as objects with several levels of hierarchy. At the low level system consists of modern integrated circuits (IC) like PLD and ASIC, which implement SoCs (System-on-Chip), NoCs (Network-on-Chip), memories, processors [1-4]. The second level is formed by digital devices assembled as a single system on a board, where low level ICs represent the elements. The third level consists of boards, which united to conception of system on a crate. Typical representative of such system is personal computer IBM PC. The fourth level unifies sets of crates or boxes into complex control system of manufacturing processes or critical technologies (aviation, airspace, nuclear-power engineering, meteorology, defense, ecology) [5]. The fifth level may be considered as geographically distributed system (Internet). Further in this report, it's considered hierarchies from the first to the fourth levels with the purpose to create models and methods of its testing with prior defined diagnosis depth.

The *purpose* of research – testing and diagnosis time reducing of complex digital systems, based on general model of organization and execution of diagnostic experiment, including conditional and unconditional algorithms of defect finding using testability standards.

Object of research – digital system, represented as several hierarchy levels, designed using testability standards. Specifically, it's considered program-technical complex F, as object of testing, can be represented as quadruple $F = \langle C, B, P, M \rangle$, where $C = \{c_1, c_2, ..., c_n\}$ – finite nonempty set of crates in system, $B = \{b_1, b_2, ..., b_m\}$ – set of boards in crate, $P = \{p_1, p_2, ..., p_k\}$ – packages on board, $M = \{m_1, m_2, ..., m_l\}$ – set of IP modules in IC.

Essential equation of diagnosis for concerned object of research can be written in the following way:

$$D = R \wedge L = (R_m \oplus R_r) \wedge L = [(T \oplus F) \oplus (T \oplus F_r)] \wedge L$$

where parameters $D, L, R, R_m, R_r, T, F, F_r$ – are respectively: set of detected faults in system; fault coverage; binary vector of experimental validation (VEV), equal to number of observed outputs; reference vector of output states; vector of experimental validation of output states; test; reference device model; real device.

2. Ad hoc technologies of digital system testing

Three parameters: manufacturing yield ratio, design time-to-market and operational reliability are deciding during efficiency analysis of available testing tools. Naturally, revolutionary transformations in micro- and nano-technologies of chip manufacturing and its use for SoC and NoC creation set up new challenges in testing and diagnosis of complex digital systems and networks [6,7]. Solving one of the mentioned problems is concerned with reducing number of faulty products DL depending on test quality T: $DL = 1 - Y^{(1-T)}$. If test covers 100% defects then yield ration will be maximal or faulty production will not be shipped to the customers. As regards the time-to-market, here one of the essential criteria is test quality too, which impacts the verification and testing time. Also fault coverage test quality is deciding for ensuring the reliability of operating device, as long as untimely appearing defect diagnosis can lead to disastrous effects. To address mentioned problems leading corporations use experience of design for testability, generalized into IEEE standards [8-11]: IEEE 1149.1-2001 Standard Test Access Port and Boundary-Scan Architecture; IEEE Std 1149.4-1999 Standard for a Mixed-Signal Test Bus; IEEE Std 1149.6-2003, Standard for Boundary-Scan Testing of Advanced Digital Networks; IEEE 1500-2005, Standard Testability Method for Embedded Core-based Integrated Circuits.

In an effort to minimize IP-cores testing time it's offered [12] important extension to IEEE Boundary Scan standard [8]. Its main idea as the following: each IP-core has its own BIST, which generates pseudorandom test sequence. All IP-cores are tested in parallel. Test schedule may introduce idle periods, due to the test conflicts between the deterministic tests of different cores. It is used AMBA bus for test distribution. Thus it's offered solution, based on hybrid BIST architecture, where

test consists of pseudorandom test sequences, which are generated in on-line mode, and deterministic test pattern, which is generated in off-line mode and stored in system memory. Authors offer methodology for finding the optimal (in the view of time cost) combination of pseudorandom and deterministic tests for whole system, consisting of multicores. Further it's offered specialized testing technologies for complex digital systems, which advance hybrid methodology [13], combines mentioned standards and heuristics.

Testing system (fig. 1) utilizes bus for test sequences transportation from test processor to unit-under-test and its responses backwards.

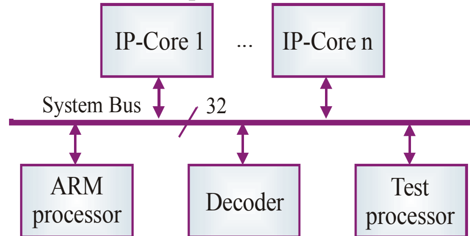

Fig. 1. Bus architecture for digital system testing

Such architecture with using decoder allows testing of several IP-cores or ICs, as well as ARM processor itself. Preparation for diagnostic experiment lies in prior tests and patterns generation for all modules in digital system. Diagnostic library (tests, responses and defect location algorithms) is stored in test processor. During execution of test procedures ARM processor gives control to the test processor with interruption of main functions of digital system. Advantages of such system consist in ease of configuration, ability of diagnosis with IC resolution and high performance, defined by clock frequency and bus width:

$$\varphi = \frac{k_t \times n_t}{f \times r}, \quad (1)$$

where k_t, n_t, f, r – number of rows and columns (dimension) of test, clock frequency and data transfer bus width respectively.

Disadvantage of given architecture consists in impossibility of defect location and identification inside the IC.

To remove this disadvantage, it's offered structure (fig. 2) that combines advantages of data transfer bus organization between IP-cores with high diagnosis resolution, as in IEEE 1149 standard. Payment for diagnosis quality is significant slowing down of testing experiment; its duration is defined as:

$$\varphi = \frac{k_t \times n_t}{f \times r \times L_{bsr}}, \quad (2)$$

where L_{bsr} – length of boundary scan chain of IP-core under test. It's necessary to underline that such approach is oriented on functional testing of system components, and it doesn't consider interconnections between IP-cores.

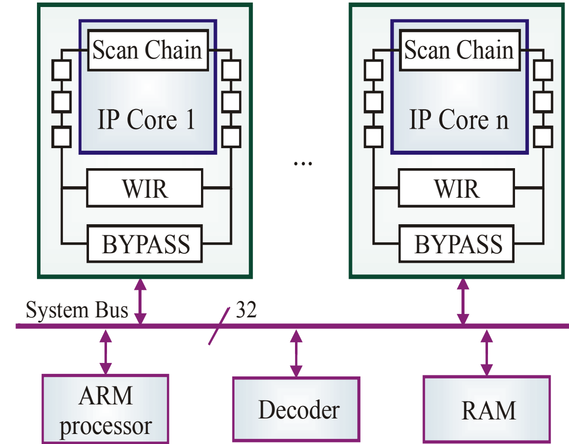

Fig. 2. Bus architecture and Boundary Scan standard

The next architecture (fig. 3) combines advantages of bus organization, Boundary Scan standard and BIST tools. It gives significant reducing of test experiment execution time for high defect diagnosis resolution within single system component:

$$\varphi = \frac{\eta(k_t \times n_t)}{f \times r \times L_{bsr}}, \quad (4)$$

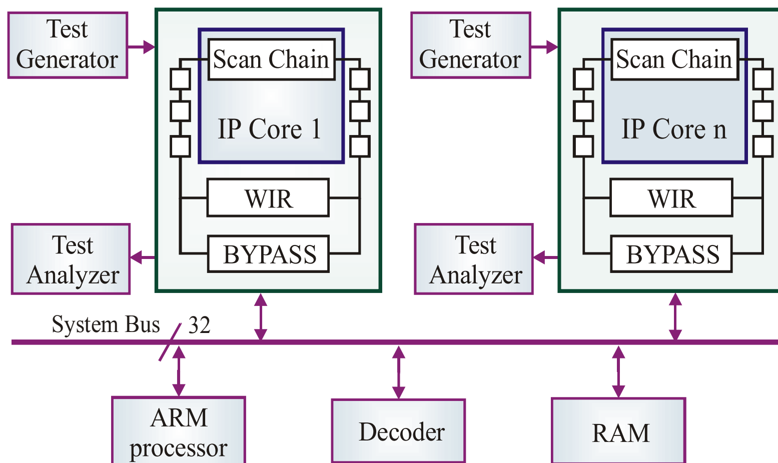

Fig. 3. Bus architecture, BIST and Boundary Scan standard

where η – coefficient, which taking into account the part of deterministic test in whole test sequence length (plus pseudorandom sequences) for IP-core testing.

Naturally, it's necessary to perform N such experiments for verification of all digital system components in an effort to diagnose.

General structure of testing process of complex hierarchical digital system in an effort to check operability, locate and identify defects is shown at fig. 4.

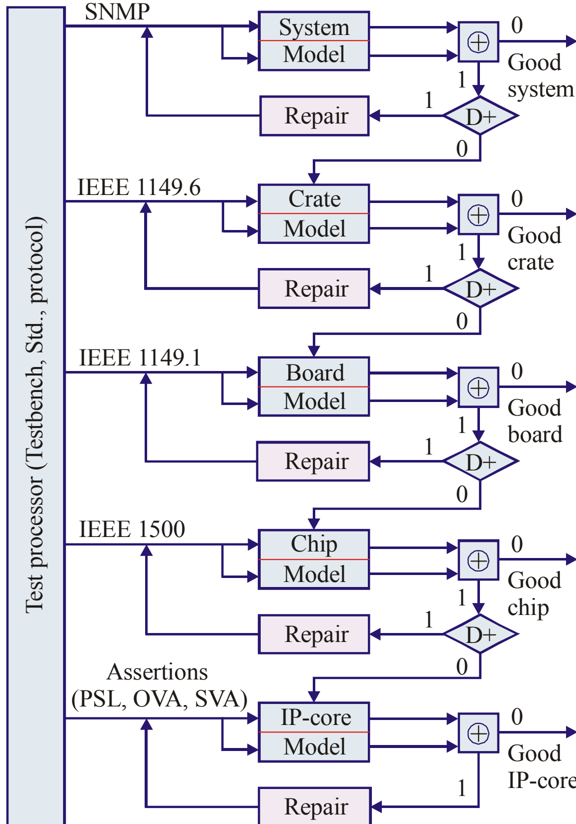

Fig. 4. Structure of complex digital system testing process (D+ – user is satisfied with diagnosis resolution)

Principles of testing system organization: 1) use the most appropriate IEEE standards [8-11] for verification of components on the current level of hierarchy; 2) determine given diagnosis resolution automatically, without using of conditional defect location algorithms; 3) only single component may be faulty; 4) testing procedure after repair begins from the top level to low level of hierarchy – descending diagnosis; 5) testing procedure may begin from any level of hierarchy and may finish on the desired level by engineer.

Test processor regulates feeding of input sequences in necessary format with defined properties for specific components of considered level of hierarchy $\{C, B, P, M\} \in F$. Each component has its own standard of test description for checking and diagnosis of custom defects. Testing supports automatic mode of defects location with the required diagnosis resolution – up to gate level or piece of source code. On user request, process can be finished on reaching required diagnosis resolution with further repairing and returning to the top level of diagnosis experiment.

3. Conclusions

During current research international IEEE standards are considered, which are suitable for testing and diagnosis of program-technical complexes and broad range of electronic systems: starting with components inside IC, up to complex systems, consisting of boards and crates. Considered IEEE standards 1149.1, 1149.4, 1149.6 and 1500 offer wide ability for testing of: functional components, interconnections, systems on board, systems on crate. Units under test are the following components: analog, digital, mixed, as well as discrete elements, printed circuit boards, consisting of mentioned components. Unit-hierarchical testing and diagnosis method is considered, which lies in offering of complex system in the form of hierarchy of simpler units. Thus, Boundary Scan technologies allow designers to meet the modern requirements and tendencies during design, verification, debug, manufacturing, testing, embedded software design and operation of different systems. Compliance of final software or hardware product to the international IEEE standards – is a guarantee of successful distribution on the world market. Scientific novelty of obtained results lies in using of ad hoc technologies, combining existing testability standards with specialized schematic solutions, which allow reducing in several times testing and diagnosis temporal expenses of complex digital systems. Practical significance consists in application of offered diagnosis process model to complex hierarchical digital systems design, which control critical technologies.

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