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Hierarchical Analysis of Testability for SoCs

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Abstract

This paper presents the strategy of testable SoC design procedure. This approach based on the testability analysis on different levels of abstractions (gate level, register transfer level, system level). Analysis is based on structural analysis of SoC. Proposed methods give possibility to simplify the verification task and to generate test synthesis and and/or to improve faults covering for the given inputs. The main goal of the presented algorithms is to increase fault coverage before test generation and to decrease verification time. It could be reached by improving of testability and simplification of the verification task.

1. Introduction

As a complexity of today's ASIC designs continues to increase, the challenge of verifying these designs intensifies at an even greater rate [1]. Testability is one of the most important factors that are considered at digital devices design along with reliability, speed and the cost. The low level of device testability leads to increasing of number of non-tested faults and verification time at design, production and operations stages. Therefore, the cost of diagnostic (a degree of faults concentration) decreases essentially during techniques of testability design.

The cost of a fault essentially increases in the process of ASIC crystal implementation (Fig. 1). Hence analysis of testability needs to be done at earlier level of device description. This is the main reason of development of the methods of testability analysis at the different levels of abstraction: system, RT, and gate levels.

Object under test – system on chip, which can be presented on different levels of abstraction.

Goal of work – maximal decreasing of test procedure cost; to provide digital circuit testability on all design levels of abstraction, till device manufacturing stage. To provide device testing possibility with minimal test by adding of scan cells on bottlenecks in circuit (circuit's parts, which hard to test).
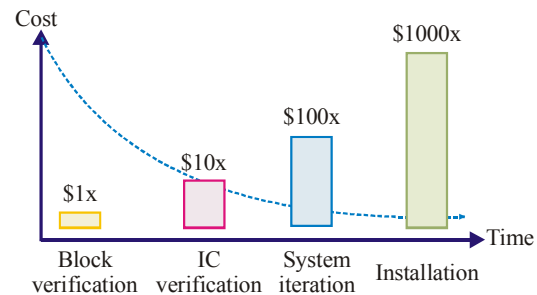
Figure 1. Dependence between cost and verification

Tasks: 1) to develop the method of testability analysis on different levels of abstraction. 2) Minimal increasing of observable lines in circuit or code lines, which will provide the best fault coverage. 3) To develop strategy of minimal additional lines selection. 4) To develop algorithm of circuit modification. 5) Verification and testing of developed methods on standard benchmarks.

It is need to provide testability analysis of developed system model on all of design stages. Here, the most adequate analysis is corresponding to most accurate model, represented on gate level. In this case, circuit is presented by the most detailed structure. Nevertheless, testability analysis on the more high levels of abstraction, where project model is represented as structure of interconnected components, laboriousness of analysis procedure is minimal, but testability values and further project modification based on boundary scan technology can essentially influence on diagnostic assurance and maintenance costs (time and economic expenses directed on test synthesis, fault simulation and diagnosis for each design stages). Using of IEEE DFT standards is presented on Fig. 2. Standard instructions are ensuring the scan and test modes of System on Chip (SoC) components.

Thus, for test procedure organization on the gate level is enough to use scan path, which consist of easy tested, modified boundary scan cells [2],[4],[7].

For testing procedure organization on register transfer level is practicable to use such DFT standards as IEEE 1149.1BS [4] or IEEE 1500SECT [5].

For device analysis and test procedure realization on system (algorithmic) level is proposed to present

the program code as oriented marked Moore graph (FSM). To test such structure is supposed to use System JTAG standard [6].
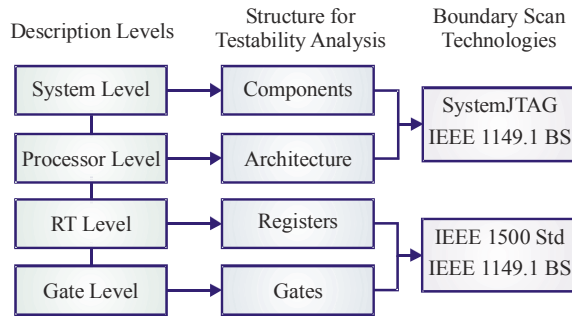
Figure 2. Levels of abstraction

To succeed goal of work it is need to provide scan procedure of internal weakly observable and controllable lines in circuit.

Developed device, as a rule, can be presented as composition of control automata and operational automata. Structure of relations between control automata and operational automata could be specified by model on figure 3.

$$M = <X, Y, Z, f, g>, \qquad (1)$$

where $X = \{X_1, X_2,..., X_i,..., X_m\}$,

$Y = \{Y_1, Y_2..., Y_j,..., Y_h\}$, $Z = \{Z_1, Z_2..., Z_r,..., Z_k\}$ — sets of inputs, internal and outputs variables. Relations between these variables could be described by generalized equations:

$$Y(t) = f[X(t-1), X(t), Y(t-1), Z(t-1)];$$
$$Z(t) = g[X(t-1), X(t), Y(t-1), Y(t), Z(t-1)]. \qquad (2)$$
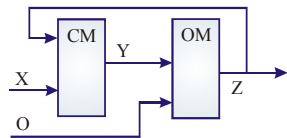
Figure 3. Model of device

Structure of control automata could be presented as oriented marked Moore graph. Operational device, as usually, could be presented by regular structure, which easy to analyse on gate level or register transfer level. Such decomposition of control and operational automata is presented on figure 4.
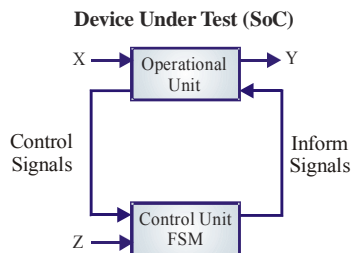
Figure 4. Decomposition of CM and OM.

2. Testability analysis for FSM

In a FSM all hard reachable states have to be tested. The deadlock situation is also need to be tested. The places of branches localization and code feedbacks (if, case, loop, while operators) is also needed to be tested. The proposed method calculates the value of the vertex reachability (testability). The analysis is done on the marked Moore graph-scheme.

2.1. Calculation of reachability (controllability)

The reachability of the initial vertex is $R(a_1)=1$. The controllability of each vertex depends of the value of reachability of the previous vertex and of the reachability index. The reachability can take the relative value from [0; 1]. The initial vertex has 100% of controllability. $R(a_i)=0$ has the vertex that can not be accessible by any graph path

$$R(a_j) = \sum_{i=1}^{m} R(a_{i-1}) \times \frac{1}{n} \times w_{ij} \qquad (3)$$

where n is the number of all possible set of graph path to the vertex a_i; w_{ij} is edge weight: $w_{ij}=1/k_i$: k is the number of outgoing edges, m is the number of incoming edges.

The Fig. 5 depicts the marked graph-scheme of Moore machine. The total controllability before modification is equal $R_{total}=0,333455$.
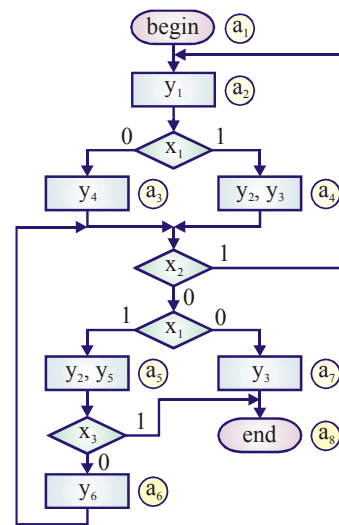
Figure 5. Marked flow-chart of Moore FSM

$R(a_1) = 1;$ $\qquad$ $R(a_2) = 1;$
$R(a_3) = 0,2863533467;$ $\quad$ $R(a_4) = 0,2863533467;$
$R(a_5) = 0,035794183;$ $\quad$ $R(a_6) = 0,008948545;$
$R(a_7) = 0,0363545;$ $\qquad$ $R(a_8) = 0,045301.$
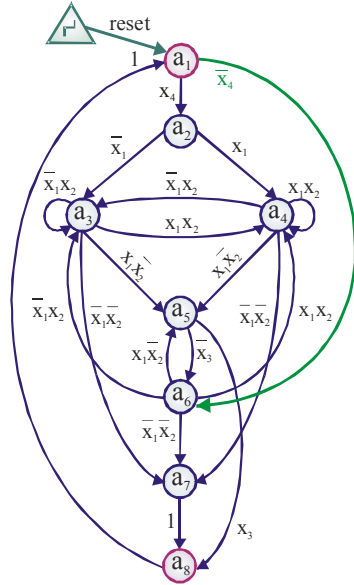
Figure 6. Modified graph of Moore FSM

For our example the worth case of controllability is exists for the vertex a_6 (Fig. 6).

So the additional condition x_4 could be added to flowchart structure.

The total controllability before modification is equal $R_{total}=0{,}41725$ (Figure 5).

$$R(a_1) = 1; \qquad R(a_2) = 1;$$
$$R(a_3) = 0{,}2863533467; \quad R(a_4) = 0{,}2863533467;$$
$$R(a_5) = 0{,}035794183; \quad R(a_6) = 0{,}05894;$$
$$R(a_7) = 0{,}039462; \qquad R(a_8) = 0{,}0484105;$$

3. Testability analysis for RTL

Table presentation of digital devices is used to present models of functional elements and for their analysis. Table representation is the most practically feasible information perception form for user and computer, which based on cubic computation, mathematical tool for compact description of digital structures. Main disadvantage of table representation of finite state machine is dimension. It is could be decreased by using redundancy in alphabet for binary Boolean variables states coding. Thus, estimation of the testability is based on the topological analysis of the circuit. In probabilistic approaches values of controllability, observability, and testability are depend on truth table of primitive. In this case the extended probabilistic method for gate level could be used [3].

However, when device is presented by cubic coverage, problem of simulation of value 'X' is occurring. For obtaining of accurate analysis of cubic coverage,

which stored in memory, it is proposed to redefine the symbol 'X'. Testability analysis algorithm for RT level is following. Values of controllability for primary inputs are equal to $P(X_i) = 0{,}5$ (input of circuit could be set in logic one or logic zero as well). Values of controllability are calculated from primary inputs to primary outputs through circuit structure. Output values of block under test are dependent of values of controllability of inputs and logic zero (one) propagation ratio. Ratio could be calculated by formulas:

$$K(0) = \frac{n(0)}{n(0) + n(1)}; \quad K(1) = \frac{n(1)}{n(0) + n(1)}; \qquad (4)$$

Thus, values of controllability of each node are calculated by following formulas:

$$P^0(X_{i+1}) = K(0) \cdot \prod_{i=1}^{m} P^0(X_i); \qquad (5)$$

$$P^1(X_{i+1}) = K(1) \cdot \prod_{i=1}^{m} P^1(X_i); \qquad (6)$$

where $n(1)$, $(n(0))$ is number of vectors, which gives logic one (zero) on the output of device; m – number of inputs in logic block.

Values of the testability are calculated for each line (node). Indexes, that calculated are intended for comparative analysis of the testability of the nodes of the circuit. Analysis of the topology of the device is performed on the register transfer level description of the circuit. In case when convergent fan-outs are present in circuit, formulas have to be modified to following:

$$P^0(X_{i+1}) = K(0) \cdot \prod_{i=1}^{m} P^0(X_i) \cdot 2^{k+1}; \qquad (7)$$

$$P^1(X_{i+1}) = K(1) \cdot \prod_{i=1}^{m} P^1(X_i) \cdot 2^{k+1}; \qquad (8)$$

where k – number of convergent fan-outs. This rule is valid for testability analysis on gate level as well.

4. Testability analysis for gate level

More detailed and adequate analysis is executed on the gate level. Here values of controllability, observability, and testability are calculated for each line in circuit. Such analysis is executed for circuits, which can not be tested by deterministic test.

Controllability CY – the quantity of ability of the device to generate on a set line value 0 (CY^0) or $1(CY^1)$ which depends on a logic function of the device. It decreases with the increasing of a distance of a line from external inputs of the circuit. Controllability can take the relative value, which belong to [0; 1] interval.

CY = 1 – has primary inputs of the device, where it is possible to set logic '0' and '1'. CY = 0 – has line, that can not be set in any of the logic values.

Practically, most values of the controllability are situated between the limits of range [0; 1]. In general case, controllability of inputs of the gates is not equal 100%. Therefore controllability must consider ability to transmit logic values from gate and values of the controllability on its inputs:

$$CY^0(Y) = KCY^0 \cdot f^0, \quad CY^1(Y) = KCY^1 \cdot f^1 \quad (9)$$

where KCY – coefficient of the controllability transfer, that defined by the logic function of the gate (KCY^1 – for setting of logic one on the output of the gate, KCY^0 – for setting of logic zero on the output of the gate);

Coefficients of the controllability transfer are defined by these expressions:

$$KCY^0 = \frac{N(0)}{N(1) + N(0)}, \quad KCY^1 = \frac{N(1)}{N(1) + N(0)} \quad (10)$$

where N(0) (N(1)) – number of all methods of setting of logic zero (one) on the primitive output line. f^0 – function, which defined by formula:

$$f^0 = [\sum_{\forall z^0} \frac{CY^i(X_1) + CY^j(X_2) + \dots + CY^k(X_n)}{n}]/m \quad (11)$$

where n – number of gate's inputs; z^0 – input patterns $(X_1, X_2, \dots, X_n)$, which allow to obtain logic '0' on the output Y; m – number of patterns z^0; i,j,…, k $\in \{0,1\}$ and equal to 0, if $X_1, X_2, \dots, X_n$ on z^0 are equal to zero value; and equal to 1, if $X_1, X_2, \dots, X_n$ on z^0 are equal to one value. f^1 – function, which defined by formula:

$$f^1 = [\sum_{\forall z^1} \frac{CY^i(X_1) + CY^j(X_2) + \dots + CY^k(X_n)}{n}]/p \quad (12)$$

where n – number of gate inputs; z^1 – input patterns $(X_1, X_2, \dots, X_n)$, which allow to obtain logic '1' on the output Y; p – number of patterns z^1; i,j,…, k $\in \{0,1\}$ and equal to 0, if $X_1, X_2, \dots, X_n$ on z^1 and take on '0' values, and, equal to 1, if $X_1, X_2, \dots, X_n$ on z^1 take on '1' values. Sum of z^0 and z^1 patterns is equal to 2^n.

Calculation of controllability is beginning from primary inputs to primary outputs. It is not necessary to solve linear equations for sequential circuits, as in classical methods, because the fun-outs must be cut.

4.1. Calculation of the observability

Observability OY – the quantity of ability of the device to transport a condition of considered line on external outputs of the circuit which depends on logic functionality of the device.

Observability can take a relative value in [0; 1].

OY = 1 for primary output of the device.

OY = 0, if it is impossible to change the logic value on the primary output by changing logic value in the node. Practically, most values of the observability are situated between the limits of range [0; 1].

In general case (Fig. 7), transferring faults through primitive (logic gate) from inputs to output is depends on the ability to activate the appointed input. It is depends on the ability to set the fix values on the some/all inputs, which allows activating the path to appointed output of the device (the function of the controllability of these inputs).
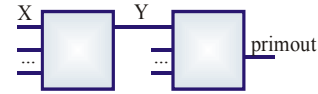
Figure 7. Observability calculation

Therefore, observability is defined by the equation:

$$OY(X - primout) = OY(Y - primout) \cdot g, \quad (13)$$

where primout – primary output of device; X – Y – primout – activation path; g – arithmetic mean of values of the controllability (on the inputs), which ensures activate of the input X to output Y.

$$g = \frac{CY^i(X_1) + CY^j(X_2) + \dots + CY^k(X_{n-1})}{n - 1} \quad (14)$$

where n – number of inputs of device, $(X_1, X_2, \dots, X_{n-1})$ – input patterns (z_a), which provides the activation of X_n – Y path, i,j,…, k $\in \{0,1\}$ and equal to 0, if $X_1, X_2, \dots, X_{n-1}$ on z_a take on '0' values, and, are equal to 1, if $X_1, X_2, \dots, X_{n-1}$ on z_a take on '1' values. Values of observability are calculated from primary outputs to primary inputs.

4.2. Calculation of the testability

Testability of node can be calculated as multiplication of it controllability and observability.

$$TY^0(Y) = CY^0(Y) \cdot OY(Y), \quad (15)$$

$$TY^1(Y) = CY^1(Y) \cdot OY(Y), \quad (16)$$

$$TY(Y) = (TY^0(Y) + TY^1(Y))/2, \quad (17)$$

where $TY^0(Y)$ $(TY^1(Y)) - 0$ – testability (1- testability) of node Y; TY(Y) – testability of node Y.

General value of circuit's testability can be presented as measure of average laboriousness of test generation for circuit's node; therefore, this measure can be presented as an arithmetic mean of testabilities of all nodes in circuit, i.e.

$$TY_{circuit} = [\sum_{i=1}^{L} TY(Y_i)] / L, \qquad (18)$$

$TY_{circuit}$ – general testability of circuit, L – number of nodes in circuit. For convenient interpretation of the results it is taken the 8-th root of the controllability, observability and testability values. Method complexity (performance) is linear.

5. Strategy of Testing and Modification. Experimental Results

Strategy of point selection for the circuit modification on the gate level is: 3% of lines are selected with the minimal value of controllability and observability at the same time to the selected lines the lines with maximal value is added. Usually the number of such selected lines is small; this is a feature of the evaluation method. 3% of selected lines have been selected from the restrictions on the external additional contacts in the device – no more than 2-5%. Results of fault coverage for this case are presented in table 1. The proposed modification strategy consists of separation of test and functional operations. A conditional vertex is added on each selected vertices in FSM and scan cells are placed on selected lines in circuit for gate level and register transfer level. Such approach allows to obtain 100% controllability on selected bottleneck.

Table 1. Fault coverage for combinational and sequential circuits on the gate level

Circuit ISCAS'85	FC before modification	FC after modification	Test
C432	87,173%	100 %	Determ.
C499	99,763%	100 %	Determ.
C880	93,563%	100 %	Determ.
C3540	97,798%	98,53 %	Random
C6288	99,653%	99,81 %	Random
C20000	72,094%	99,71%	Random
ISCAS'99			
sb01	96,667%	100%	Rand.
sb02	92,308%	100%	Rand.
sb03	98,077%	100%	Rand.
sb04	91,969%	100%	Rand.
ISCAS'89			
s208	99,537%	100%	Rand.
s298	98,750%	100%	Rand.
s344	99,123%	100%	Rand.

The testability index calculation for FSM and application of the strategy of device modification are presented in the Table 2 (index of reachability of graph modification: R_{BM} – before and R_{AM} – after). Here the variable with the least index of reachability is the operated variable.

Table 2. Analysis of testability for FSM

FSM	R_{BM}	R_{AM}	Differ	Increase
Traf_light	0,23306	0,3133	0,08	23,9%
Multiplier	0,44271	0,5508	0,11	25%
CSK_M	0,38360	0,5232	0,14	36,8%
MPA_Ma	0,24702	0,4001	0,16	64,7%
CA_M	0,33346	0,4173	0,08	23,9%

A one additional variable in the graph structure increases quality of faults covering approximately on 15-30%. In the Table 3 the quality of the test for the sample Multiplier is absent because the quality of faults covering before modification is equal 100 %.

Table 3. Faults coverage for FSM

FSM	Q_{BM}, %	Q_{AM}, %	Increase, %
Traf_light	50,00	62,5	12,5
CSK_M	71,43	85,71	14,28
MPA_M	37,5	75,0	37,5
CA_M	62,5	87,5	25

Practical importance and advantages: 1) methods simplicity; no needs to solve system of linear equations for sequential circuits; 2) simple strategy of bottlenecks selection; 3) simplicity and regularity of circuits modification; 4) scan cells could be completely tested independently of other circuit part; 5) possibility to provide high level of circuit testability (minimal or zero number of undetectable lines) before test generation; 6) spending of device analysis on the earliest design stages and increasing of Yield Ratio.

Disadvantages: 1) no absolutely guarantee to obtain 100% fault coverage; 2) increasing of testing time due to using of SP and F modes.

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