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Design of Wavelet Filter Bank for JPEG 2000 Standard

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Abstract

Models, method and hardware implementation of lifting-based wavelet filter scheme for JPEG 2000 standard are proposed. JPEG 2000 image compression standard is used for data transmission, print and scan of images, digital photography. Low-pass and high-pass filters for implementing JPEG 2000 transformation are described. Obtained results were compared with the same parameter of other discrete wavelet transformation (DWT) devices that were proposed in others references. This work purpose is essential speed growing of the ad hoc pipelining lifting-based DWT hardware implementation. JPEG2000 is new image compression algorithm based on discrete wavelet transformation of input data. This technique is a next development of JPEG group. It could be used for data transmitting in Internet, for image printing and scanning, for digital photography. Transform time reduce due to ad hoc SoC architectures essential increases the device feasibility attractiveness. To achieve this purpose the next challenges have been solved: 1. Digital models and their transformation methods were considered. 2. Lifting-based wavelet transformation hardware architecture was designed. 3. Control algorithm for DWT was created. 4. DWT-device on Xilinx FPGA was implemented. 5. Digital system testing and verification, different device version speeds and SNR were compared.

Keywords: *Discrete wavelet transform, DWT, JPEG2000, Lifting Scheme, Filter bank.*

I. Digital Image Models And Transformation Framework

In mathematical analysis, wavelets were defined as translates and dilates of one fixed function that could be used to analyze and represent general function. There are used biorthogonal wavelet transformations. Biorthogonality allows the construction of symmetric filter bank using wavelet and basic functions.

Haare wavelet is the simplest example of wallet transformation.

$$(x^*,y^*) = (x,y)\times\begin{pmatrix}\cos 45^\circ & \sin 45^\circ\\ -\sin 45^\circ & \cos 45^\circ\end{pmatrix} = (x,y)\times\frac{1}{\sqrt{2}}\times\begin{pmatrix}1 & 1\\ -1 & 1\end{pmatrix} = (x,y)\times R \quad (1)$$

where R is orthogonal matrix. Matrix orthogonality means that inverse transformation can be done using transposed matrix, R^T:

$$(x,y) = (x^*,y^*)\times R^{-1} = (x^*,y^*)\times R^T = (x^*,y^*)\times\frac{1}{\sqrt{2}}\times\begin{pmatrix}1 & -1\\ 1 & 1\end{pmatrix} \quad (2)$$

JPEG2000 filter bank consists of low-pass, h0, and high-pass, h1, filters described by impulse responses. In others words, wavelet transformation implementation is input data processing by low-pass and high-pass filters. Decimation is used in order to data volume not grow. The low-pass and high pass filter pair is known as analysis filter and forward wavelet transformation – as analysis (fig. 1). Inverse wavelet transformation is known as synthesis.

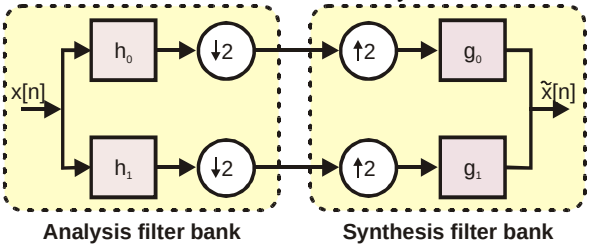

Figure 1. 1D wavelet analysis and synthesis filter-bank

2D discrete wavelet transformation is realized using 1D DWT. Each row of 2Dimage is first transformed using 1D horizontal analysis filters. Then each column of this transformation result is changed using the same filters bank.

Analysis result is two samples set $y[2n]=y_0[n]$, and $y[2n+1]=y_1[n]$ that correspond to low-pass and high-pass filters, correspondingly. Reconstruct image inverse transformation is called synthesis and uses g_0 and g_1 functions. 2D wavelet transformation sample is $y[2n_1+b_1, 2n_2+b_2] = y_{b1,b2}[n_1,n_2]$, где $b_1,b_2\{0,1\}$.

The convolution is used for forward and inverse wavelet transformation [4,5]:.

$$\breve{y}[n] = \sum_{i\in Z} h^t_{n \bmod 2}[i]\breve{x}[n-i]$$

$$\breve{x}[n] = \sum_{i\in Z} \breve{y}[n]g^t_{n \bmod 2}[n-i] \qquad (3)$$

Analysis and synthesis filter banks are related by expression:

$$g^t_0[n] = \alpha^{-1}(-1)^n h^t_1[n];\ g^t_1[n] = \alpha^{-1}(-1)^n h^t_0[n], \qquad (4)$$

where the gain factor, α, is given by:

$$\alpha = \tfrac{1}{2}(h^{dc}_0 h^{nyq}_1 + h^{dc}_1 h^{nyq}_0) \qquad (5)$$

where h^{dc}_b is DC frequency; h^{nyq}_b – Nyquist frequency:

$$h^{dc}_b = \sum_n h^t_b[n];\ h^{nyq}_b = \sum_n (-1)^n h^t_b[n], \qquad (6)$$

where $b=\{0,1\}$

A N level DWT is obtained by applying N DWT. The JPEG2000 standard supports values of N in the range $0 \le N \le 32$. Typical values are in the range N =4 through N =8 with D=5 sufficient to obtain near optimal compression performance for the full resolution image.

Part 1 of JPEG2000 standard describes two filter-banks Daubechies 9/7 and 5/3. The left part in pair indicates a number of low-pass filter's coefficients, the right part indicates a number of high-pass filter's coefficients. For example, for Daubechies 9/7 bank a low-pass filter has 9 coefficients, high-pass filter has 7 coefficients. Daubechies filters application allows to get better compression result, but lower quality. The loss of quality is caused by application of irrational coefficients and calculations. Also Daubechies filter-bank is more complex for realization.

5/3 analysis filter-bank is described by following expression.

$$\begin{pmatrix} h^t_0(z) \\ h^t_1(z) \end{pmatrix} = \begin{pmatrix} -\frac{1}{8}z^{-2} + \frac{1}{4}z^{-1} + \frac{3}{4} + \frac{1}{4}z - \frac{1}{8}z^2 \\ -\frac{1}{2}z^{-1} + 1 - \frac{1}{2}z \end{pmatrix}$$

II. Lifting Scheme

Lifting scheme is a second generation of wavelet transformation. It is not a scaling and shifting of the basic function and it has several additional advantages. Each wavelet transformation, based on FIR-filters could be realized by application of finite lifting steps. Moreover, lifting method allows biorthogonal wavelet constructing and has set of advantages in comparison with classical convolution wavelet implementation [1, 2, 3, 4].

Lifting scheme (fig 3) realized by four basic steps: splitting (S), prediction (P), updating (U) and scaling (K).

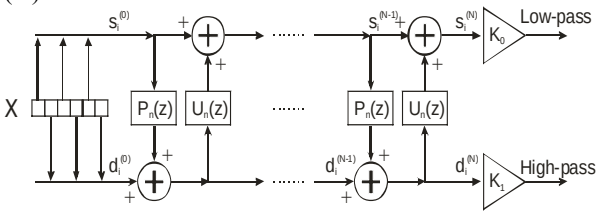

Figure 3. Lifting structure of forward wavelet transformation

The prediction and update steps are generally iterated N times, with different weights used at each iteration.

$$d^{(n)}_i = d^{(n-1)}_i + \sum_k P_n(k)s^{(n-1)}_k, n \in [1,2,...,N]$$

$$s^{(n)}_i = s^{(n-1)}_i + \sum_k U_n(k)d^{(n)}_k, n \in [1,2,...,N]$$

Where $s^{(0)}_i$ and $d^{(0)}_i$ denote the even and odd elements of input sequence. For 5/3 filter-bank N=1, $P_1 = -\frac{1}{2}$, $U_1 = \frac{1}{4}$, K0=K1=1.

So, lifting scheme for 5/3 filter bank consists of one prediction step and one update step that are calculated by following equations:

$$d^{(1)}_i = d^{(0)}_i - \tfrac{1}{2}(s^{(0)}_i + s^{(0)}_{i+1}),\ s^{(1)}_i = s^{(0)}_i + \tfrac{1}{4}(d^{(1)}_{i-1} + d^{(1)}_i)$$

III. Hardware Implementation Architectures

Among hardware wavelet implementation there are distinguished convolution-based architecture [5, 6] and lifting-based architecture [3, 4, 7, 8] .

I. Daubechies and W. Sweldens work about factoring application for wavelet transform realization and the lifting scheme offered there allows simplifying DWT implementation. By the way of external memory usage wavelet transform device architectures are divided into three groups [7] level-by-level, block-based, line-based.

Level-by-level architecture uses one computing unit for sequential image processing, first by rows, then by columns. External memory stores all data: input, intermediate and result data. As a result memory access time is a bottleneck of level-by-level architecture. Different memory blocks with parallel access could be used to store data on different stages of transformation. In that case blocks of different size with separate data ports (up to two for each block) are needed [4]. It seems to be unreal if the external memory is used. But internal memory resource could be not enough for whole input and result image storing.

Block-based architecture is similar to level-by-level architecture. The difference is that image is divided into blocks which can be saved in internal memory. The drawback is possibility of image block boundary artifact appearance.

Typical line-based architecture uses different calculating block for different wavelet transform levels. For data storing between raw and column processing internal buffer memory is used.

IV. Pipelining DWT Device Schema

In the considered works the main emphasis was done on size minimization of device arithmetic part. How ever the arithmetic part size is not very important for device that use internal memory. The more important ones are the memory size minimization, fast and simple control block developing that considering FPGA implementation features. The work goal is the device implementation in FPGA, device speeds analysis that depend on different FPGA chip.

The designed DWT block is intended for using as IP core for JPEG2000 encoder device. The proposed device architecture doesn't use any external memory to save any intermediate results. Data feed the device inputs sequentially by one sample per time unit. Then the DWT result samples feed to arithmetic or other entropic encoding block and after that compression data get to device output. Modern programmable device sizes allow to implement the several level DWT device into one chip without using external memory for intermediate data saving. The developed device makes five level wavelet transformation. The input image size is up to 128x128 8-bits pixels.

Figure 3 describes one level transformation device architecture for the 5/3 filter bank. Internal FPGA distributed and block memory is used for saving intermediate data. Row buffer is implemented on register memory resources. Column buffer of the first transformation levels are built on block memory, for last level ones are enough on distributed memory.

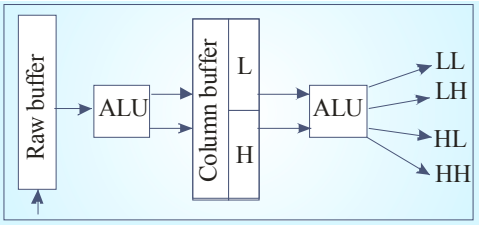

Figure 3. One level 2DWT device

Raw buffer size is three cells implemented on FPGA register memory. Arithmetic block for raw data processing (fig. 4) forms high-pass and low-pass output in turn. In contrast to existing DWT device our arithmetic block is designed for low-pass and high-pass filter implementation simultaneously.

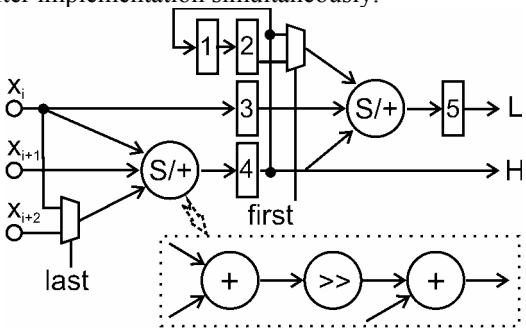

Figure 4. 2-step arithmetic block scheme

It is necessary to have three memory banks of N/2 size (fig. 5) for saving every sub-band result before doing wavelet transformation by column. Furthermore it is better to use block RAM (BRAM) for first wavelet transformation level blocks, and distributed RAM for last ones. The size of required buffer memory is equal to N/2*3*2=3N. Figure 5 shows memory block for one sub-band transformation and includes: d block that saves data formed on predicting step for preceding data; C0 block stores 1D DWT results for even rows; C1 block stores 1D DWT results for odd rows.

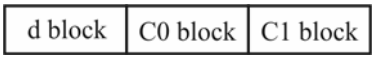

Figure 5. Memory block designation

It is enough to perform the transformation of first two rows and to save the results in C0 and C1 memory blocks to start processing by column.

The one arithmetic block (fig 6) can be used in column transformation to form low-pass and high-pass input data. It depends on the fact that data is fed to block input in interleave manner (Table 1).

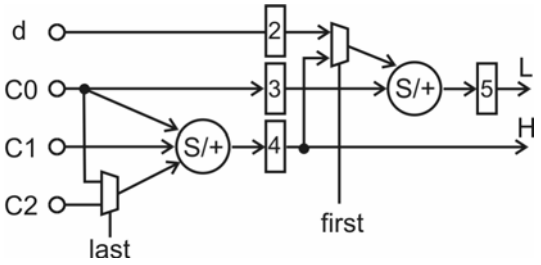

Figure 6. Arithmetic block for column data processing

Table 1. Order of column arithmetic block data generating

Step	Ariph block inputs		Ariph block output	
	H	L	H	L
1				
2			HH	
3			HL	LH
4			HH	LL
5			HL	LH
6			HH	LL
7			HL	LH
8			HH	LL
1			HL	LH
2				LL

The device has pipeline architecture. Control scheme is based-on counters (fig. 7). Control block of the device consists of two counters: counter1 and counter2. The control signal depends of their values. The counter1 counter counts sample number in the row from 0 to Tile_size+2 and form control signals, first_elem and last_elem, that describe first and last row samples. Also the data from fist counter, counter1, are used to form memory addresses (MEM_Li and MEM_Hi) for saving the intermediate transformation results. The other counter, counter2, counts the column numbers from 0 to Tile_size+1. It is applied to generate control first_colon and last_colon signals that indicate first and last columns of the image block. The both counters are used to generate control signals of output buffer: enable_LL, enable_LH, enable_HL, and enable_HH.

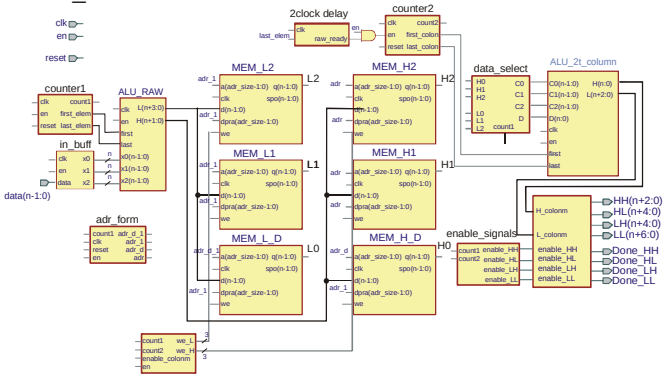

Figure 7. 1 level DWT device architecture

V. FPGA-based implementation Results

Device is implemented using internal memory of two types: distributed and block. In FPGA the distributed memory is built on look-up-table, block memory – on BRAM. The results of speed analysis have shown that block memory based devices are faster than those, based on distributed memory (fig. 8). The device speed depends on image size (especially for distributed memory based devices). In this case, device speed also depends on place&route algorithm which places device blocks into chip. One level wavelet transformation blocks are connected together to compose multilevel wavelet transformation.

The devices based on both types of memory (either distributed or block memory) have the same speed for small size images (fig 8). It allows to implement the devices for first wavelet transformation levels on BRAM. The devices for last transformation levels are implemented on distributed memory. It results in optimal by speed and area devices.

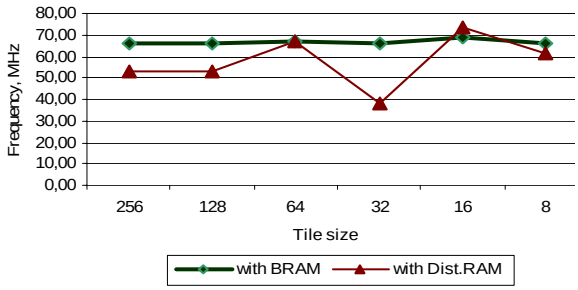

Figure 8. Depended on transformation image size and chip series frequency of implemented in xc3s4000-4 device

The device was compared with those, proposed by IP Core market on DWT and JPEG2000 coder/decoder (fig 9). The results of comparison show that proposed device has enough good speed for smaller size of implemented circuit.

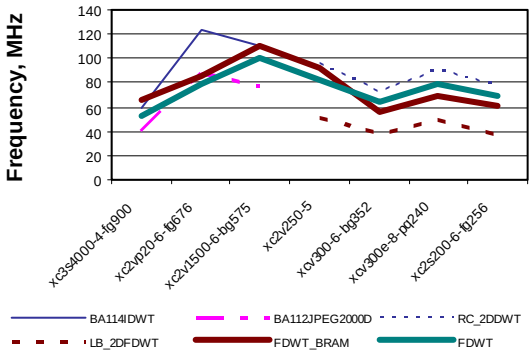

Figure 9. Device frequency comparison

VI. CONCLUSION

Discrete wavelet transformation device architecture, which doesn't use external memory that increase the device speed, was developed. Also it allows reducing device cost.

IP Core for JPEG2000 encoder/decoder SoC was proposed.

In this work it was put emphasis on the fast control block design, not only arithmetic blocks that was made in considering references. It allows increasing speed the whole device. The speed analysis for devices implemented on different Xilinx FPGA series with different memory types and transformation image sizes was done.

The device was compared with existing prototypes by speed and area.

Scientific novelty is the pipelining DWT device that is intent to use as IP core and implement in programmable chip. The proposed device has more simple ALU part, doesn't use external memory, and so is faster and chipper than existing analogs.

The practical significance is proposition of the simple, high technology and effective DWT device that have high speed and low power consumption. It is its advantage in over software implementation of the IEEE JPEG2000 standard.

Further work steps:

1. DWT and IDWT device design for 5/3 and 9/7 JPEG2000 filter banks.

2. DWT and IDWT device implementation using Xilinx Virtex-4 DSP processor.

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