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7th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)

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The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

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CONTENTS

Coverage Method for FPGA Fault Logic Blocks by Spares

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Abstract

A fault coverage method for digital system-on-chip by means of traversal the logic block matrix to repair the FPGA components is proposed. A method enables to obtain the solution in the form of quasioptimal coverage for all faulty blocks by minimum number of spare tiles. A choice one of two traversal strategies for rows or columns of a logic block matrix on the basis of the structurization criteria, which determine a number of faulty blocks, reduced to the unit modified matrix of rows or columns is realized .

1. Introduction

The problem of testing technologies adaptation for new digital system-in-package (SiP), which gradually develops the market of electronic technology [1-6] is considered. SiP forms new challenges of real-time Infrastructure IP for system functionalities, which differs from embedded diagnosis of SoC components essentially.

Yervant Zorian is leading scientist in the field of Design and Test in the world [3] and he said now the main problem of digital system repairing is designing the methods and technologies for on-chip logic repairing although it occupies no more 10% of chip area.

Objective of the research is design of a method for on-chip diagnosis of digital system-on-a-chip on the basis of traversal the rows and columns to increase SiP testability, quality and reliability.

The problems are: 1) design of a matrix model for the FPGA logic blocks in the form of tiles, which contain faults; 2) design of a coverage method for faulty logic blocks by spare tiles in the traversal of matrix rows or columns; 3) testing and verification of the method on examples of logic block matrixes, containing various faulty configurations.

2. Galls method for a logic block matrix to cover the faulty FPGA components by spare tiles

Topology of a chip is represented by the tile matrix $M = |M_{ij}| i = \overline{1,p}; j = \overline{1,q}$ scalable horizontal and vertical by integers ($p \times q$). Every tile M_{ij} has n^2 logic blocks. The matrix has an arbitrary number of faults, equal to k. There are less or equal n^2 faulty logic blocks in every tile. An example of a tile matrix with faults is shown in Fig. 1. Here the dimension of tile n is equal to 3 and matrix dimension in the number of tiles by rows and columns is equal to 5.

The traversal method for a matrix of logic blocks is represented by the steps below. It is designed to repair the FPGA components and enables to get quasi-optimal coverage of all faulty blocks by minimum numbers of spare tiles.

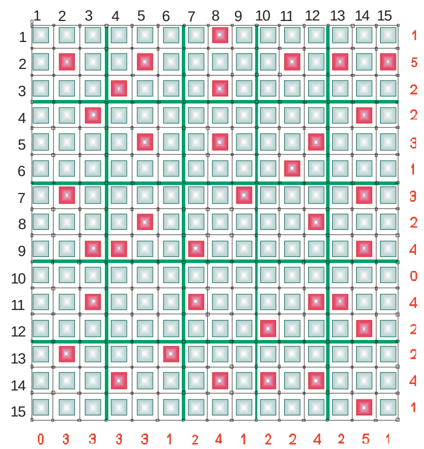


Figure 1. FPGA block matrix in the number of tiles

1. Determination of coordinates for all faulty blocks of the matrix $M = |M_{ij}|$, specifies the topology of a chip.

2. Construction of binary coverage matrixes for faulty blocks by traversal of the tiles in rows and columns, which dimension is determined by the parameters respectively:

$$M_r = |M^r_{ij}|, i = \overline{1, p/n}; j = \overline{1, q};$$

$$M_c = |M^c_{ij}|, i = \overline{1, p}; j = \overline{1, q/n}.$$

Here every n coordinates of a row (column) is replaced by one coordinate with value that is determined by $f^r(f^c)$ function Or of n coordinates.

$$M^c_{ij} = f^r(f^c) = \begin{cases} 0 \leftarrow (000); \\ 1 \leftarrow (1XX) \vee (X1X) \vee (XX1), X = \{0,1\}. \end{cases}$$

For instance, a procedure for obtaining a row traversal matrix gives the result

$$M = |M_{ij}| = \begin{vmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{vmatrix} \xrightarrow{f^r} M_r = |M^r_{ij}| = \begin{vmatrix} 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 1 \end{vmatrix}$$

Here each column is compressed in the two coordinates on the rules of logical operation Or, because the tile parameter n is equal to 3 here and below.

Similarly a procedure for obtaining a column traversal matrix gives the result

$$M = |M_{ij}| = \begin{vmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{vmatrix} \xrightarrow{f^c} M_c = |M^c_{ij}| = \begin{vmatrix} 0 & 1 \\ 0 & 1 \\ 1 & 1 \\ 1 & 1 \\ 0 & 1 \\ 1 & 1 \end{vmatrix}.$$

3. Determination of coverage quality criteria for faulty blocks by using the binary matrixes on the basis of counting the numbers of unit coordinates reduced to the actual unit matrix.

The row coverage criterion faulty blocks is determined by the following expression:

$$Q_r = \sum_{i=1}^{p/n} \left[\frac{1}{H^r_i - L^r_i + 1} \sum_{j=1}^{q} M^r_{ij} \right].$$

Here $H^r_i(L^r_i)$ – maximum (minimum) index of j-th coordinate for a row of the matrix $|M^r_{ij}|$, after (before) which there are only zero coordinates in a row. Actually $H^r_i - L^r_i + 1$ is the units spread interval in rows of the matrix $|M^r_{ij}|$, which gives the sum of unit row coordinates. Further reduced estimates for all rows are added, which is the criterion of row coverage for faulty blocks.

The column coverage criterion is the following:

$$Q_c = \sum_{j=1}^{q/n} \left[\frac{1}{H^c_j - L^c_j + 1} \sum_{i=1}^{p} M^c_{ij} \right].$$

Here $H^c_j(L^c_j)$ – maximum (minimum) index of j-th coordinate for a column of the matrix $|M^c_{ij}|$, after (before) which there are only zero coordinates in a column. Actually $H^c_j - L^c_j + 1$ is the units spread interval in columns of the matrix $|M^c_{ij}|$, which gives the sum of unit column coordinates. Further reduced estimates for all columns are added, which is the criterion of column coverage for faulty blocks.

4. The decision on the choice of strategy $S = \{S_r, S_c\}$ for coverage of faulty logic blocks by spares by means of comparing the values of the structurization criteria Q_r, Q_c for the rows and columns:

$$S = \begin{cases} S_r \leftarrow Q_r < Q_c; \\ S_c \leftarrow Q_r \geq Q_c. \end{cases}$$

In the first case, the faulty blocks coverage strategy is realized by sequential traversal of all tile rows. The second one – the traversal of tile columns is done.

5. The tile traversal strategy by rows is realized by the the modified matrix $|M^r_{ij}|$. Each matrix row is represented by the binary vector $M^r_i = (M^r_{i1}, M^r_{i1}, ..., M^r_{ij}, ..., M^r_{iq})$. Step 1. Nulling of a zero coordinate counter and a spare tile counter: $j = 0,\ Q = 0$. Step 2. Sequential scanning of the vector elements $j = j + 1 \leftarrow M^r_{ij} = 0$ up to the first "1" encountered $M^r_{ij} = 1 \rightarrow (Q = Q + 1, j = j + n - 1)$. From this "1" it is counted n tiles, which are covered by the spare tile. The number of spare tiles Q is increased by 1. Step 3. If the condition $j \geq q$ is true – the end of row processing. Otherwise – go to step 2. The procedure is applied to all rows of the modified matrix

$\left|M_{ij}^{r}\right|$ ($\left|M_{ij}^{c}\right|$), resulting in counter Q will contain the minimum number of spares to cover all faulty blocks. Similarly the tile traversal strategy by columns ($\left|M_{ij}^{c}\right|$) is performed. In this case the index i is changed instead of j in a traversal procedure.

6. Definition of the coverage quality for obtained solution by means of counting the number of faulty blocks of the matrix, reduced to the minimum number of spares N, covering all faulty blocks:

$$Q_{cr} = \frac{1}{N}\sum_{i=1}^{n} F_i \, .$$

7. The end of finding of a quasioptimal cover of faulty blocks by spares.

Example. For FPGA, shown in Fig. 1, according to item 2 of the repair model the construction of two matrixes is performed:

$$M_r = \left|M_{ij}^{r}\right| = \begin{array}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|} \hline 0&1&0&1&1&0&0&1&0&0&1&0&1&0&1 \\ \hline 0&0&1&0&1&0&0&1&0&0&1&1&0&1&0 \\ \hline 0&1&1&1&1&0&1&0&1&0&0&1&0&1&0 \\ \hline 0&0&1&0&0&0&1&0&0&1&0&1&1&1&0 \\ \hline 0&1&0&1&0&1&0&1&0&1&0&1&0&1&0 \\ \hline \end{array}$$

$$M_c = \left|M_{ij}^{c}\right| = \begin{array}{|c|c|c|c|c|} \hline 0&0&1&0&0 \\ \hline 1&1&0&1&1 \\ \hline 0&1&1&0&0 \\ \hline 1&0&0&0&1 \\ \hline 0&1&1&1&0 \\ \hline 0&0&0&1&0 \\ \hline 1&0&1&0&1 \\ \hline 0&1&0&1&0 \\ \hline 1&1&1&0&1 \\ \hline 0&0&0&0&0 \\ \hline 1&0&1&1&1 \\ \hline 0&0&0&1&1 \\ \hline 1&1&0&0&0 \\ \hline 0&1&1&1&0 \\ \hline 0&0&0&0&1 \\ \hline \end{array}$$

Further, in accordance with paragraph 3, the calculation of the structurization criteria is performed for the matrix above:

$$Q_r = \sum_{i=1}^{p/n}\left[\frac{1}{H_i^r - L_i^r + 1}\sum_{j=1}^{q} M_{ij}^{r}\right] = \frac{7}{14} + \frac{6}{12} + \frac{8}{13} + \frac{6}{12} + \frac{7}{13} = 2{,}64 \;;$$

$$Q_c = \sum_{j=1}^{q/n}\left[\frac{1}{H_j^c - L_j^c + 1}\sum_{i=1}^{p} M_{ij}^{c}\right] = \frac{6}{12} + \frac{7}{13} + \frac{7}{14} + \frac{7}{13} + \frac{7}{14} = 2{,}58 \cdot$$

As it can be seen from the above-mentioned criteria, the number of faulty coordinates in the columns reduced to the unit matrix is less than in the rows. Therefore, subject to item 4, the strategy for solving the coverage problem by column traversal is chosen: $S_c \leftarrow (Q_r = 2{,}64 \geq Q_c = 2{,}58)$.

Structural appeal of columns is higher than rows, because the number of faults reduced to the matrix is less than in the first case.

This strategy gives the actual quality of coverage – the number of faulty logic blocks of the matrix (by one spare tile), reduced to the necessary quantity of spares that is equal to:

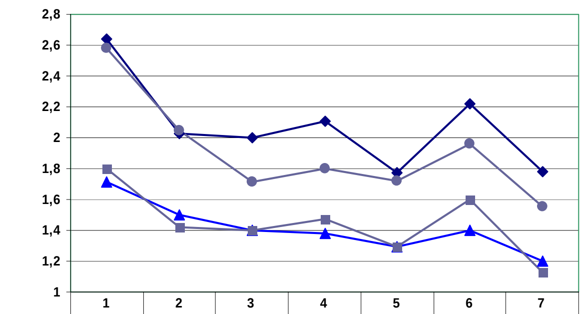
$$Q_c^* = \frac{1}{N}\sum_{i=1}^{n} F_i = 36/20 = 1{,}8.$$

For comparison – the row traversal procedure gives a lower quality:

$$Q_r^* = \frac{1}{N}\sum_{i=1}^{n} F_i = 36/21 = 1{,}71.$$

The final coverage of a fault set has one tile more (21) than the solution obtained by the first method (20). So, the choice of coverage strategy on the basis of calculation and comparison the criteria for counting the number of unit coordinates, reduced to the actual unit matrix, confirms their consistency and the subsequent optimality of obtained coverage.

Fig. 2 shows statistics of the processing of different types logic block matrixes with faulty components. It demonstrates correctness of applying the proposed criterion, which shows the optimal and efficient strategy of matrix traversal to obtain minimum coverage of faulty logic blocks by spare tiles in all cases except the last one. In the latest variant the structurization criteria by rows greater than by columns $Q_r = 1{,}78 > Q_c = 1{,}55$ that is the basis of covering the faults by columns. In this case the coverage quality is $Q_c^* = 1{,}125$ that corresponds to 16 spare tiles needed to repair all 18 faulty blocks. While the optimal solution is traversal of the matrix by columns, where the coverage quality is $Q_c^* = 1{,}2$ that corresponds to 15 spare tiles only.



	1	2	3	4	5	6	7
Qr	2,64	2,03	2	2,11	1,77	2,22	1,78
Qc	2,58	2,05	1,71	1,8	1,72	1,96	1,55
Q*r	1,71	1,5	1,4	1,38	1,29	1,4	1,2
Q*c	1,8	1,42	1,4	1,47	1,29	1,6	1,125

Figure 2. Structurization criteria and coverage quality for the examples

3. Software "aGalls" for covering of faulty FPGA components by spare tiles

Software «aGalls» is designed for covering of faulty FPGA components by spare tiles by using the traversal method for logic block matrix.

The initial information is represented by a matrix of tiles $M = \left| M_{ij} \right| i = \overline{1,p}; j = \overline{1,q}$, the dimension $p \times q$, where each tile has n*n logic blocks. The initial quantity of faults k is made to the matrix. The software detects the coordinates of all faults, constructs the binary coverage matrixes for faulty blocks by means of traversing the tiles by columns and rows, and calculates the quality criteria of fault coverage (Fig. 3).

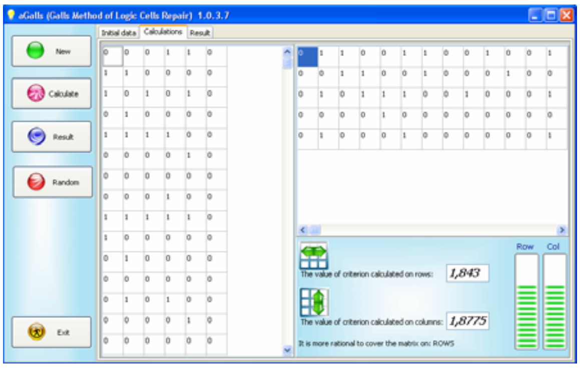


Figure 3. Calculation results

The program provides the opportunity to review the changes of temporary matrixes after covering the faulty blocks both horizontally and vertically. In addition, the actual number of spare tiles needed to cover all faults is displayed; it enables to estimate the correctness of the selected solution on the basis of calculating the criteria (Fig. 4).

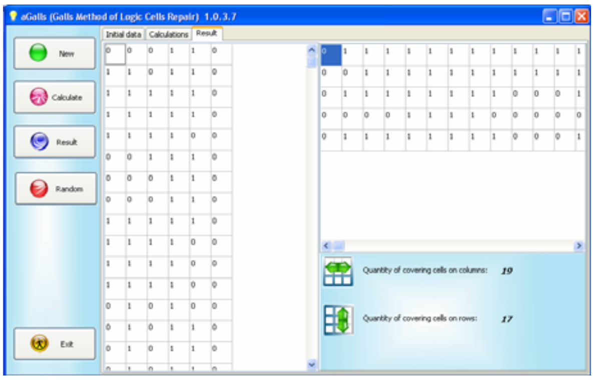


Figure 4. Coverage of a matrix with faults and spares

An algorithm for solving the coverage problem implemented in the software is represented below and in Fig. 5.

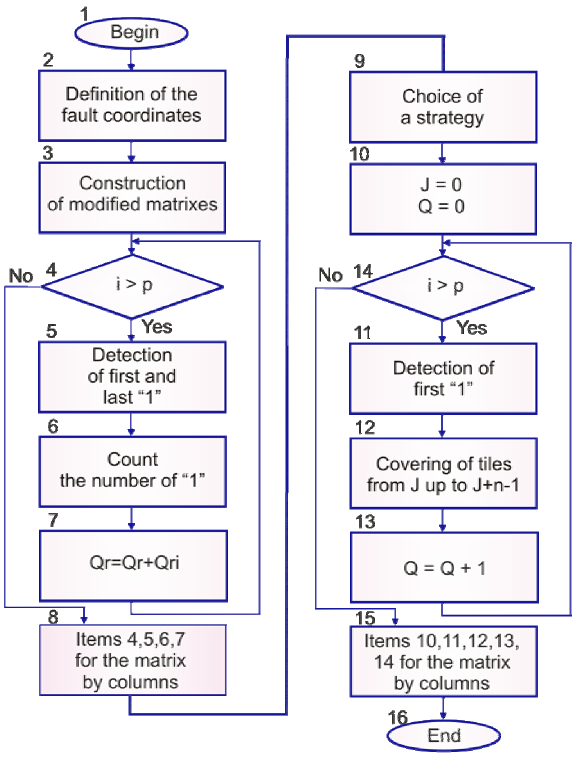


Figure 5. Model of solving the optimal coverage task

1. Beginning of solving the coverage problem for a logic block matrix by spare tiles. 2. Determination of the coordinates for all faulty blocks of the matrix. 3. Construction of the binary coverage matrixes for faulty blocks to traverse the tiles by rows and columns. 4. Construction the fault coverage for the modified matrix by means of their traversal by rows. 5. Detection the first and last "1". 6. Counting the number of "1" in a row. 7. Increment number of rows processed. 8. Calculation of the structurization criteria by rows. 9. Implementation of items 4, 5, 6, 7 for columns. 10. The decision on the choice of faulty blocks coverage strategy in the direction corresponding to the lower value of the criterion. 11. Nulling of zero coordinates counter and spare tile counter $j = 0, Q = 0$. 12. Sequential scanning of the vector elements $j = j + 1 \leftarrow M^r_{ij} = 0$ up to the first "1' $M^r_{ij} = 1 \rightarrow (Q = Q + 1, j = j + n - 1)$ by rows. 13. From this "1" it is counted n tiles, which are covered by the spare. 14. The value Q is incremented by 1. 15. If

$j \geq q$ – the end of row proceeding, otherwise – item 11. 16. Implementation of items 10, 11, 12, 13, 14 at traversal by columns. The end of searching the quasioptimal coverage of faulty blocks by spare tiles.

To check the validity of the criteria 200 experiments for the matrix M was carried out; the dimension of matrix is p*q, the number of blocks in the tile is n horizontally and vertically, and the number of faults is k, where

$$p = \overline{3,7};\ n = \overline{2,5};\ q = \overline{3,7};\ k = \overline{3,(n \times p \times q)}.$$

As a result, by using the criteria the most efficient way to repair has not been determined in 29% of cases, respectively a positive result – 71%. Fig. 6 presents diagrams showing the values of structurization criteria and coverage quality at the traversal of the modified matrix by rows and columns for the 10 examples. The dimension of the matrix was constant: 4 tiles in the horizontal and 5 ones vertical, the dimension of the tiles was 3*3 blocks.

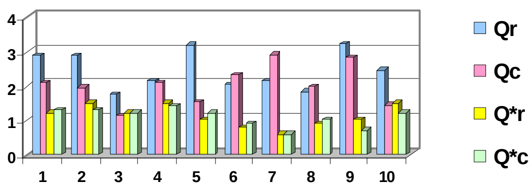


Figure 6. Structurization criteria and coverage quality

The software is used to verify and test the method for obtaining the quasioptimal fault coverage by minimum quantity of spare tiles. It can be implemented into a chip as embedded Infrastructure IP component, where the initial information about the topology of a chip has to be memorized during Place and Route process.

4. Conclusion

The traversal method for a logic block matrix is designed to repair the FPGA components by obtainment the solution in the form of quasioptimal coverage for all faulty blocks by minimum number of spare tiles. It is proposed a choice one of two traversal strategies for rows or columns of a logic block matrix on the basis of the structurization criteria, which determine a number of faulty blocks, reduced to the unit modified matrix of rows or columns.

The scientific novelty. The matrix model for FPGA logic blocks in the form of functional tiles, containing faults, is proposed. The model allows repairing of the FPGA components by means of the developed coverage method for faulty logic blocks by spare tiles through traversal of FPGA rows and columns. The method enables to obtain a solution in the form of quasioptimal coverage for a set of faulty blocks by minimum quantity of spare tiles.

The practical significance lies in the attractiveness of the proposed method for the market of electronic technology, which allows determining the minimum number of spares for repair of digital product, implemented into a chip SoC/SiP.

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