

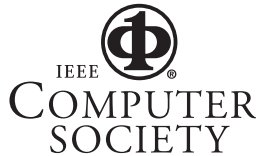
KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

# Proceedings of IEEE East-West Design & Test Symposium (EWDTS'09)

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**Moscow, Russia, September 18 – 21, 2009**

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## 7<sup>th</sup> IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)

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The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

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- Failure Analysis, Defect and Fault
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- Memory and Processor Test
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## CONTENTS

Simulation-based Verification with APRICOT Framework using High-Level Decision Diagrams <b>Maksim Jenihhin, Jaan Raik, Anton Chepurov, Raimund Ubar</b> .....	13
Fault-Detection Capability Analysis of a Hardware-Scheduler IP-Core in Electromagnetic Interference Environment <b>J. Tarrillo, L. Bolzani, F. Vargas, E. Gatti, F. Hernandez, L. Fraigi</b> .....	17
Hardware Reduction in FPGA-Based Compositional Microprogram Control Units <b>Barkalov A.A., Titarenko L.A., Miroshkin A.N.</b> .....	21
Optimization of Control Units with Code Sharing <b>Alexander A. Barkalov, Larisa A. Titarenko, Alexander S. Lavrik</b> .....	27
SAT-Based Group Method for Verification of Logical Descriptions with Functional Indeterminacy <b>Liudmila Cheremisinova, Dmitry Novikov</b> .....	31
MicroTESK: Automation of Test Program Generation for Microprocessors <b>Alexander Kamkin</b> .....	35
Verification Methodology Based on Algorithmic State Machines and Cycle-Accurate Contract Specifications <b>Sergey Frenkel and Alexander Kamkin</b> .....	39
Coverage Method for FPGA Fault Logic Blocks by Spares <b>Vladimir Hahanov, Eugenia Litvinova, Wajeb Gharibi, Olesya Guz</b> .....	43
Testing and Verification of HDL-models for SoC components <b>Vladimir Hahanov, Irina Hahanova, Ngene Christopher Umerah, Tiecoura Yves</b> .....	48
The Model of Selecting Optimal Test Strategy and Conditions of ICs Testing During Manufacturing <b>Sergey G. Mosin</b> .....	54
A Technique to Accelerate the Vector Fitting Algorithm for Interconnect Simulation <b>Gourary M.M., Rusakov S.G., Ulyanov S.L., Zharov M.M.</b> .....	59
Frequency Domain Techniques for Simulation of Oscillators <b>Gourary M.M., Rusakov S.G., Stempkovsky A.L., Ulyanov S.L., Zharov M.M.</b> .....	63
Distributed RLC Interconnect: Estimation of Cross-coupling Effects <b>H.J. Kadim, L.M. Coulibaly</b> .....	67
Constrained-Random Verification for Synthesis: Tools and Results <b>D. Bodean, G. Bodean, O. Ghincul</b> .....	71
Discussion on Supervisory Control by Solving Automata Equation <b>Victor Bushkov, Nina Yevtushenko, Tiziano Villa</b> .....	77
Generalized Faulty Block Model for Automatic Test Pattern Generation <b>F. Podyablonsky, N. Kascheev</b> .....	80
Self Calibration Technique of Capacitor's Mismatching For 1.5 Bit Stage Pipeline ADC <b>Vazgen Melikyan, Harutyun Stepanyan</b> .....	84
Applied Library of Adaptive Lattice Filters for Nonstationary Signal Processing <b>Victor I. Djigan</b> .....	87
On-chip Measurements of Standard-Cell Propagation Delay <b>S.O. Churayev, B.T. Matkarimov, T.T. Paltashev</b> .....	93
FPGA FFT Implementation <b>S.O. Churayev, B.T. Matkarimov</b> .....	96

Reconfiguration and Hardware Agents in Testing and Repair of Distributed Systems <b>G. Moiş, I.Ştefan, Sz. Enyedi, L. Miclea</b> .....	99
Symmetrization in Digital Circuit Optimization <b>Natalia Eliseeva, Jie-Hong R. Jiang, Natalia Kushik, Nina Yevtushenko</b> .....	103
Embedded Processor Power Reduction via Power aware Custom Instruction Selection <b>Hoda Ahmadinejad, Saeed Safari, and Hamid Noori</b> .....	107
Level Quantization Effects in Digital Signal Processing by Discrete Fourier Transform Method <b>Gamlet S. Khanyan</b> .....	111
A New Paradigm in Design of IIR Digital Filters <b>Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich, Sergey V. Armishev</b> .....	115
Evolutionary Approach to Test Generation of Sequential Digital Circuits with Multiple Observation Time Strategy <b>Yu. A. Skobtsov, V. Yu. Skobtsov</b> .....	119
SMT-based Test Program Generation for Cache-memory Testing <b>Evgeni Kornikhin</b> .....	124
Critical Path Test Generation in Asynchronous QDI Circuits <b>Fahime Khoramnejad, Hossein Pedram</b> .....	128
Model-driven & Component-based Development Method of Multi-core Parallel Simulation Models <b>Nianle Su, Wenguang Yu, Hongtao Hou, Qun Li and Weiping Wang</b> .....	135
Minimizing of Number of Discrete Device's Controllable Points <b>Dmitriy Speranskiy, Ekaterina Ukolova</b> .....	142
VHPI-compatible Simulation and Test Generation System <b>Dmitriy Speranskiy, Ivan Ukolov</b> .....	147
Fault Tolerant HASH function with Single Element Correction and Minimum Delay Overhead <b>Costas A. Argyrides, Carlos A. Lisboa, Dhiraj K. Pradhan, Luigi Carro</b> .....	151
Analysis of the Control Vector Optimal Structure for a Minimal-Time Circuit Optimization Process <b>A.M. Zemliak, M.A. Torres, T.M. Markina</b> .....	156
Parallel Simulation of Boolean Functions by Means of GPU <b>Włodzimierz Bielecki, Alexander Chemeris, Svetlana Reznikova</b> .....	162
Two-Criterial DSSS Synchronization Method Efficiency Research <b>Kharchenko H.V., Tklich I.O., Vdovychenko Y.I.</b> .....	165
An Efficient March Test for Detection of All Two-Operation Dynamic Faults from Subclass $S_{av}$ <b>Gurgen Harutyunyan, Hamazasp Avetisyan, Valery Vardanian, Y. Zorian</b> .....	175
Large and Very Large-scale Placement <b>Bazylevych R.P., Bazylevych L.V., Shcherb'yuk I.F.</b> .....	179
An Educative Brain-Computer Interface <b>Kirill Sorudeykin</b> .....	183
Time-Hardware Resource: A Criterion of Efficiency of Digital Signal Search and Detection Devices <b>Alexander Fridman</b> .....	187
A New Principle of Dynamic Range Expansion by Analog-to-Digital Converting <b>Elina A. Biberdorf, Stanislav S. Gritsutenko, Konstantin A. Firsanov</b> .....	193
FREP: A Soft Error Resilient Pipelined RISC Architecture <b>Viney Kumar, Rahul Raj Choudhary, Virendra Singh</b> .....	196

System Remote Control of the Robotized Complex - Pegas <b>Dmitry Bagayev, Evsyakov Artem</b> .....	200
Use of Predicate Categories for Modelling of Operation of the Semantic Analyzer of the Linguistic Processor <b>Nina Khairova, Natalia Sharonova</b> .....	204
Methodological Aspects of Mathematical Modelling of Processes in a Corporate Ecological System <b>Kozulia T.V., Sharonova N.V.</b> .....	208
Getting Optimal Load Distribution Using Transport-Problem-Based Algorithm <b>Yuri Ladyzhensky, Viatcheslav Kourkchi</b> .....	212
Dialogue-based Optimizing Parallelizing Tool and C2HDL Converter <b>Steinberg B., Abramov A., Alymova E., Baglij A., Guda S., Demin S., Dubrov D., Ivchenko A., Kravchenko E., Makoshenko D., Molotnikov Z., Morilev R., Nis Z., Petrenko V., Povazhniy A., Poluyan S., Skiba I., Suhoverkhov S., Shapovalov V., Steinberg O., Steinberg R.</b> .....	216
The System for Automated Program Testing <b>Steinberg B., Alimova E., Baglij A., Morilev R., Nis Z., Petrenko V., Steinberg R.</b> .....	218
Development of the University Computing Network for Integrated Circuit Design <b>Atkin E., Volkov Yu., Garmash A., Klyuev A., Semenov D., Shumikhin V.</b> .....	221
Increase in Reliability of On-Line Testing Methods Using Natural Time Redundancy <b>Drozd A., Antoshchuk S., Martinuk A., Drozd J.</b> .....	223
An Algorithm of Carrier Recovery for Modem with M-ary Alphabets APK-Signals without PLL <b>Victor V. Panteleev</b> .....	230
At Most Attainable of Lengths a Symmetrical Digital Subscriber Line on xDSL-technologies: Engineering-Maintenance Methods of the Calculation <b>Victor V. Panteleev, Nikolay I. Tarasov</b> .....	234
New Approach to ADC Design <b>Stanislav S. Gritsutenko</b> .....	240
Simulation of Radiation Effects in SOI CMOS Circuits with BSIMSOI-RAD Macromodel <b>K.O. Petrosjanc, I.A. Kharitonov, E.V. Orekhov, L.M. Sambursky, A.P. Yatmanov</b> .....	243
Thermal Design System for Chip- and Board-level Electronic Components <b>K.O. Petrosjanc, I.A. Kharitonov, N.I. Ryabov, P.A. Kozyanko</b> .....	247
TCAD Modeling of Total Dose and Single Event Upsets in SOI CMOS MOSFETs <b>K.O. Petrosjanc, I.A. Kharitonov, E.V. Orekhov, A.P. Yatmanov</b> .....	251
Reduction in the number of PAL Macrocells for Moore FSM implemented with CPLD <b>A. Barkalov, L. Titarenko, S. Chmielewski</b> .....	255
Schematic Protection Method from Influence of Total Ionization Dose Effects on Threshold Voltage of MOS Transistors <b>Vazgen Melikyan, Aristakes Hovsepyan, Tigran Harutyunyan</b> .....	260
5V Tolerant Power clamps for Mixed-Voltage IC's in 65nm 2.5V Salicided CMOS Technology <b>Vazgen Melikyan, Karen Sahakyan, Armen Nazaryan</b> .....	263
Analysis and Optimization of Task Scheduling Algorithms for Computational Grids <b>Morev N. V.</b> .....	267
A Low Power and Cost Oriented Synthesis of the Common Model of Finite State Machine <b>Adam Klimowicz, Tomasz Grzes, Valeri Soloviev</b> .....	270

Comparison of Survivability & Fault Tolerance of Different MIP Standards <b>Ayesha Zaman, M.L. Palash, Tanvir Atahary, Shahida Rafique</b> .....	275
Hardware Description Language Based on Message Passing and Implicit Pipelining <b>Dmitri Boulytchev, Oleg Medvedev</b> .....	279
V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non-Linear Analog Circuits <b>Suraj Sindia, Virendra Singh, Vishwani Agrawal</b> .....	283
GA-Based Test Generation for Digitally-Assisted Adaptive Equalizers in High-Speed Serial Links <b>Mohamed Abbas, Kwang-Ting (Tim) Cheng, Yasuo Furukawa, Satoshi Komatsu, Kunihiro Asada</b> .....	287
Between Standard Cells and Transistors: Layout Templates for Regular Fabrics <b>Mikhail Talalay, Konstantin Trushin, Oleg Venger</b> .....	293
On-Chip Optical Interconnect: Analytical Modelling for Testing Interconnect Performance <b>H J Kadim</b> .....	300
The Problem of Trojan Inclusions in Software and Hardware <b>Alexander Adamov, Alexander Saprykin</b> .....	304
Design methods for modulo $2n+1$ multiply-add units <b>C. Efstathiou, I. Voyiatzis, M. Prentakis</b> .....	307
Geometrical Modeling and Discretization of Complex Solids on the Basis of R-functions <b>Gomenyuk S.I., Choporov S.V., Lisnyak A.O.</b> .....	313
Selective Hardening: an Enabler for Nanoelectronics <b>Ilia Polian and John P. Hayes</b> .....	316
Parameterized IP Infrastructures for Fault-Tolerant FPGA-Based Systems: Development, Assessment, Case-Study <b>Kulanov Vitaliy, Kharchenko Vyacheslav, Perepelitsyn Artem</b> .....	322
Generating Test Patterns for Sequential Circuits Using Random Patterns by PLI Functions <b>M. H. Haghbayan, A. Yazdanpanah, S. Karamati, R. Saeedi, Z. Navabi</b> .....	326
A New Online BIST Method for NoC Interconnects <b>Elnaz Koopahi, Zainalabedin Navabi</b> .....	332
Low Cost Error Tolerant Motion Estimation for H.264/AVC Standard <b>M. H. Sargolzaie, M. Semsarzadeh, M. R. Hashemi, Z. Navabi</b> .....	335
Method of Diagnosing FPGA with Use of Geometrical Images <b>Epifanov A.S.</b> .....	340
Performance Analysis of Asynchronous MIN with Variable Packets Length and Arbitrary Number of Hot-Spots <b>Vyacheslav Evgrafov</b> .....	344
System in Package. Diagnosis and Embedded Repair <b>Vladimir Hahanov, Aleksey Sushanov, Yulia Stepanova, Alexander Gorobets</b> .....	348
Technology for Faulty Blocks Coverage by Spares <b>Hahanov Vladimir, Chumachenko Svetlana, Litvinova Eugenia, Zakharchenko Oleg, Kulbakova Natalka</b> .....	353
The Unicast Feedback Models for Real-Time Control Protocol <b>Babich A.V., Murad Ali Abbas</b> .....	360
Algebra-Logical Repair Method for FPGA Logic Blocks <b>Vladimir Hahanov, Sergey Galagan, Vitaliy Olchovoy, Aleksey Priymak</b> .....	364

The Method of Fault Backtracing for HDL - Model Errors Searching <b>Yevgeniya Syrevitch, Andrey Karasyov, Dariya Kucherenko</b> .....	369
Handling Control Signals for the Scan Technology <b>Olga Lukashenko, Dmitry Melnik, Vladimir Obrizan</b> .....	373
Robust Audio Watermarking for Identification and Monitoring of Radiotelephone Transmissions in the Maritime Communication <b>Vitaliy M. Koshevyy, Aleksandr V. Shishkin</b> .....	377
An Interconnect BIST for Crosstalk Faults based on a Ring LFSR <b>Tomasz Garbolino, Krzysztof Gucwa, Andrzej Hławiczka, Michał Kopeć</b> .....	381
Generation of Minimal Leakage Input Vectors with Constrained NBTI Degradation <b>Pramod Subramanyan, Ram Rakesh Jangir, Jaynarayan Tudu, Erik Larsson, Virendra Singh</b> ....	385
Very Large-Scale Intractable Combinatorial Design Automation Problems – Clustering Approach for High Quality Solutions <b>Roman Bazylevych and Lubov Bazylevych</b> .....	389
Flexible and Topological Routing <b>Roman Bazylevych and Lubov Bazylevych</b> .....	390
An Algorithm for Testing Run-Length Constrained Channel Sequences <b>Oleg Kurmaev</b> .....	391
Constructing Test Sequences for Hardware Designs with Parallel Starting Operations Using Implicit FSM Models <b>Mikhail Chupilko</b> .....	393
Redundant Multi-Level One-Hot Residue Number System Based Error Correction Codes <b>Somayyeh Jafarali Jassbi, Mehdi Hosseinzade, Keivan Navi</b> .....	397
Parallel Fault Simulation Using Verilog PLI <b>Mohammad Saeed Jahangiry, Sara Karamati, Zainalabedin Navabi</b> .....	401
IEEE 1500 Compliant Test Wrapper Generation Tool for VHDL Models <b>Sergey Mikhtonyuk, Maksim Davydov, Roman Hwang, Dmitry Shcherbin</b> .....	406
Early Detection of Potentially Non-synchronized CDC Paths Using Structural Analysis Technique <b>Dmitry Melnik, Olga Lukashenko, Sergey Zaychenko</b> .....	411
An Editor for Assisted Translation of Italian Sign Language <b>Nadereh Hatami, Paolo Prinetto, Gabriele Tiotto</b> .....	415
Architecture Design and Technical Methodology for Bus Testing <b>M.H. Haghbayan, Z. Navabi</b> .....	419
Assertion Based Verification in TLM <b>AmirAli Ghofrani, Fatemeh Javaheri, Zainalabedin Navabi</b> .....	424
Flash-memories in Space Applications: Trends and Challenges <b>Maurizio Caramia, Stefano Di Carlo, Michele Fabiano, Paolo Prinetto</b> .....	429
Design Experience with TLM-2.0 Standard: A Case Study of the IP Lookup LC-trie Application of Network Processor <b>Masoomeh Hashemi, Mahshid Sedghi, Morteza Analoui, Zainalabedin Navabi</b> .....	433
Test Strategy in OSCI TLM-2.0 <b>Mina Zolfy, Masoomeh Hashemi, Mahshid Sedghi, Zainalabedin Navabi and Ziaeddin Daeikozekanani</b> .....	438
Synthesizing TLM-2.0 Communication Interfaces <b>Nadereh Hatami, Paolo Prinetto</b> .....	442



Advanced Topics of FSM Design Using FPGA Educational Boards and Web-Based Tools <b>Alexander Sudnitson, Dmitri Mihhailov, and Margus Kruus</b> .....	446
A Mixed HDL/PLI Test Package <b>Nastaran Nemati, Majid Namaki-Shoushtari, Zainalabedin Navabi</b> .....	450
Testing Methodologies on Communication Networks <b>Nadereh Hatami, Paolo Prinetto, Gabriele Tiotto, Paola Elia</b> .....	456
A Novel High Speed Residue to Binary Converter Design Based on the Three-Moduli Set $\{2n, 2n+1+1, 2n+1-1\}$ <b>Muhammad Mehdi Lotfinejad, Mohammad Mosleh and Hamid Noori</b> .....	460
Performance Evaluation of SAT-Based ATPG on Multi-Core Architectures <b>Alejandro Czutro, Bernd Becker, Ilija Poljan</b> .....	463
Intelligent Testbench Automation and Requirements Tracking <b>Ivan Selivanov, Alexey Rabovoluk</b> .....	471
Iterative Sectioning of High Dimensional Banded Matrices <b>Dmytro Fedasyuk, Pavlo Serdyuk, Yuriy Semchyshyn</b> .....	476
Estimating Time Characteristics of Parallel Applications in Technology of Orders Based Transparent Parallelizing <b>Vitalij Pavlenko, Viktor Burdeinyi</b> .....	480
Phase Pictures Properties of Technical Diagnostics Complex Objects <b>Tverdokhlebov V.A.</b> .....	483
Information Technology of Images Compression in Infocommunication Systems <b>Alexander Yudin, Natalie Gulak, Natalie Korolyova</b> .....	486
Technology of Cascade Structural Decoding <b>Leonid Soroka, Vladimir Barannik, Anna Hahanova</b> .....	490
Technology of the Data Processing on the Basis of Adaptive Spectral- Frequency Transformation of Multiadical Presentation of Images <b>Vladimir Barannik, Sergey Sidchenko, Dmitry Vasiliev</b> .....	495
Compression Apertures Method - Color Different Images <b>Konstantin Vasyuta, Dmitry Kalashnik, Stanislav Nikitchenko</b> .....	499
Isotopic Levels Architectural Presentation of Images Relief <b>Vladimir Barannik, Alexander Slobodyanyuk</b> .....	502
Method and Mean of Computer's Memory Reliable Work Monitoring <b>Utkina T.Yu., Ryabtsev V.G.</b> .....	505
Extended Complete Switch as Ideal System Network <b>Mikhail F. Karavay and Victor S. Podlazov</b> .....	513
Image Compression: Comparative Analysis of Basic Algorithms <b>Yevgeniya Sulema, Samira Ebrahimi Kahou</b> .....	517
Networked VLSI and MEMS Designer for GRID <b>Petrenko A.I.</b> .....	521
Path Delay Fault Classification Based on ENF Analysis <b>Matrosova A., Nikolaeva E.</b> .....	526
COMPAS – Advanced Test Compressor <b>Jiří Jeníček, Ondřej Novák</b> .....	532
<b>INVITED TALKS</b> .....	538
<b>AUTHORS INDEX</b> .....	545

# Coverage Method for FPGA Fault Logic Blocks by Spares

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## Abstract

A fault coverage method for digital system-on-chip by means of traversal the logic block matrix to repair the FPGA components is proposed. A method enables to obtain the solution in the form of quasioptimal coverage for all faulty blocks by minimum number of spare tiles. A choice one of two traversal strategies for rows or columns of a logic block matrix on the basis of the structurization criteria, which determine a number of faulty blocks, reduced to the unit modified matrix of rows or columns is realized.

## 1. Introduction

The problem of testing technologies adaptation for new digital system-in-package (SiP), which gradually develops the market of electronic technology [1-6] is considered. SiP forms new challenges of real-time Infrastructure IP for system functionalities, which differs from embedded diagnosis of SoC components essentially.

Yervant Zorian is leading scientist in the field of Design and Test in the world [3] and he said now the main problem of digital system repairing is designing the methods and technologies for on-chip logic repairing although it occupies no more 10% of chip area.

Objective of the research is design of a method for on-chip diagnosis of digital system-on-a-chip on the basis of traversal the rows and columns to increase SiP testability, quality and reliability.

The problems are: 1) design of a matrix model for the FPGA logic blocks in the form of tiles, which contain faults; 2) design of a coverage method for faulty logic blocks by spare tiles in the traversal of matrix rows or columns; 3) testing and verification of the method on examples of logic block matrixes, containing various faulty configurations.

## 2. Galls method for a logic block matrix to cover the faulty FPGA components by spare tiles

Topology of a chip is represented by the tile matrix  $M = |M_{ij}|_{i=1, \overline{p}; j=1, \overline{q}}$  scalable horizontal and vertical by integers  $(p \times q)$ . Every tile  $M_{ij}$  has  $n^2$  logic blocks. The matrix has an arbitrary number of faults, equal to  $k$ . There are less or equal  $n^2$  faulty logic blocks in every tile. An example of a tile matrix with faults is shown in Fig. 1. Here the dimension of tile  $n$  is equal to 3 and matrix dimension in the number of tiles by rows and columns is equal to 5.

The traversal method for a matrix of logic blocks is represented by the steps below. It is designed to repair the FPGA components and enables to get quasioptimal coverage of all faulty blocks by minimum numbers of spare tiles.

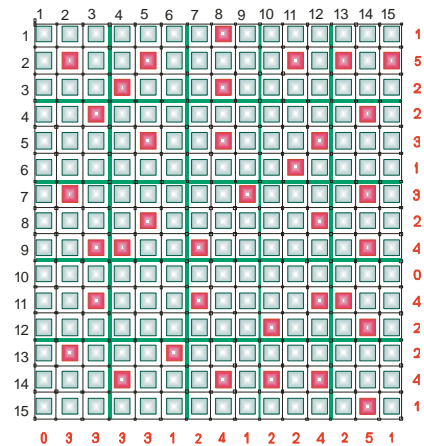


Figure 1. FPGA block matrix in the number of tiles

1. Determination of coordinates for all faulty blocks of the matrix  $M = |M_{ij}^r|$ , specifies the topology of a chip.

2. Construction of binary coverage matrixes for faulty blocks by traversal of the tiles in rows and columns, which dimension is determined by the parameters respectively:

$$M_r = |M_{ij}^r|, i = \overline{1, p/n}; j = \overline{1, q};$$

$$M_c = |M_{ij}^c|, i = \overline{1, p}; j = \overline{1, q/n}.$$

Here every  $n$  coordinates of a row (column) is replaced by one coordinate with value that is determined by  $f^r(f^c)$  function Or of  $n$  coordinates.

$$M_{ij}^c = f^r(f^c) = \begin{cases} 0 \leftarrow (000); \\ 1 \leftarrow (1XX) \vee (X1X) \vee (XX1), X = \{0,1\}. \end{cases}$$

For instance, a procedure for obtaining a row traversal matrix gives the result

$$M = |M_{ij}| = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \xrightarrow{f^r} M_r = |M_{ij}^r| = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 1 \end{bmatrix}$$

Here each column is compressed in the two coordinates on the rules of logical operation Or, because the tile parameter  $n$  is equal to 3 here and below.

Similarly a procedure for obtaining a column traversal matrix gives the result

$$M = |M_{ij}| = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \xrightarrow{f^c} M_c = |M_{ij}^c| = \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ 1 & 1 \\ 1 & 1 \\ 0 & 1 \\ 1 & 1 \end{bmatrix}$$

3. Determination of coverage quality criteria for faulty blocks by using the binary matrixes on the basis of counting the numbers of unit coordinates reduced to the actual unit matrix.

The row coverage criterion faulty blocks is determined by the following expression:

$$Q_r = \sum_{i=1}^{p/n} \left[ \frac{1}{H_i^r - L_i^r + 1} \sum_{j=1}^q M_{ij}^r \right].$$

Here  $H_i^r(L_i^r)$  – maximum (minimum) index of  $j$ -th coordinate for a row of the matrix  $|M_{ij}^r|$ , after (before) which there are only zero coordinates in a row.

Actually  $H_i^r - L_i^r + 1$  is the units spread interval in rows of the matrix  $|M_{ij}^r|$ , which gives the sum of unit row coordinates. Further reduced estimates for all rows are added, which is the criterion of row coverage for faulty blocks.

The column coverage criterion is the following:

$$Q_c = \sum_{j=1}^{q/n} \left[ \frac{1}{H_j^c - L_j^c + 1} \sum_{i=1}^p M_{ij}^c \right].$$

Here  $H_j^c(L_j^c)$  – maximum (minimum) index of  $j$ -th coordinate for a column of the matrix  $|M_{ij}^c|$ , after (before) which there are only zero coordinates in a column. Actually  $H_j^c - L_j^c + 1$  is the units spread interval in columns of the matrix  $|M_{ij}^c|$ , which gives the sum of unit column coordinates. Further reduced estimates for all columns are added, which is the criterion of column coverage for faulty blocks.

4. The decision on the choice of strategy  $S = \{S_r, S_c\}$  for coverage of faulty logic blocks by spares by means of comparing the values of the structurization criteria  $Q_r, Q_c$  for the rows and columns:

$$S = \begin{cases} S_r \leftarrow Q_r < Q_c; \\ S_c \leftarrow Q_r \geq Q_c. \end{cases}$$

In the first case, the faulty blocks coverage strategy is realized by sequential traversal of all tile rows. The second one – the traversal of tile columns is done.

5. The tile traversal strategy by rows is realized by the the modified matrix  $|M_{ij}^r|$ . Each matrix row is represented by the binary vector  $M_i^r = (M_{i1}^r, M_{i2}^r, \dots, M_{ij}^r, \dots, M_{iq}^r)$ . Step 1. Nulling of a zero coordinate counter and a spare tile counter:  $j = 0, Q = 0$ . Step 2. Sequential scanning of the vector elements  $j = j+1 \leftarrow M_{ij}^r = 0$  up to the first “1” encountered  $M_{ij}^r = 1 \rightarrow (Q = Q+1, j = j+n-1)$ . From this “1” it is counted  $n$  tiles, which are covered by the spare tile. The number of spare tiles  $Q$  is increased by 1. Step 3. If the condition  $j \geq q$  is true – the end of row processing. Otherwise – go to step 2. The procedure is applied to all rows of the modified matrix

$\left| M_{ij}^r \right| \left( \left| M_{ij}^c \right| \right)$ , resulting in counter Q will contain the minimum number of spares to cover all faulty blocks. Similarly the tile traversal strategy by columns ( $\left| M_{ij}^c \right|$ ) is performed. In this case the index i is changed instead of j in a traversal procedure.

6. Definition of the coverage quality for obtained solution by means of counting the number of faulty blocks of the matrix, reduced to the minimum number of spares N, covering all faulty blocks:

$$Q_{cr} = \frac{1}{N} \sum_{i=1}^n F_i.$$

7. The end of finding of a quasioptimal cover of faulty blocks by spares.

Example. For FPGA, shown in Fig. 1, according to item 2 of the repair model the construction of two matrixes is performed:

$$M_r = \left| M_{ij}^r \right| = \begin{bmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

$$M_c = \left| M_{ij}^c \right| = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

Further, in accordance with paragraph 3, the calculation of the structurization criteria is performed for the matrix above:

$$Q_r = \sum_{i=1}^{p/n} \left[ \frac{1}{H_i^r - L_i^r + 1} \sum_{j=1}^q M_{ij}^r \right] = \frac{7}{14} + \frac{6}{12} + \frac{8}{13} + \frac{6}{12} + \frac{7}{13} = 2,64 ;$$

$$Q_c = \sum_{j=1}^{q/n} \left[ \frac{1}{H_j^c - L_j^c + 1} \sum_{i=1}^p M_{ij}^c \right] = \frac{6}{12} + \frac{7}{13} + \frac{7}{14} + \frac{7}{13} + \frac{7}{14} = 2,58.$$

As it can be seen from the above-mentioned criteria, the number of faulty coordinates in the columns reduced to the unit matrix is less than in the rows. Therefore, subject to item 4, the strategy for solving the coverage problem by column traversal is chosen:  $S_c \leftarrow (Q_r = 2,64 \geq Q_c = 2,58)$ .

Structural appeal of columns is higher than rows, because the number of faults reduced to the matrix is less than in the first case.

This strategy gives the actual quality of coverage – the number of faulty logic blocks of the matrix (by one spare tile), reduced to the necessary quantity of spares that is equal to:

$$Q_c^* = \frac{1}{N} \sum_{i=1}^n F_i = 36/20 = 1,8.$$

For comparison – the row traversal procedure gives a lower quality:

$$Q_r^* = \frac{1}{N} \sum_{i=1}^n F_i = 36/21 = 1,71.$$

The final coverage of a fault set has one tile more (21) than the solution obtained by the first method (20). So, the choice of coverage strategy on the basis of calculation and comparison the criteria for counting the number of unit coordinates, reduced to the actual unit matrix, confirms their consistency and the subsequent optimality of obtained coverage.

Fig. 2 shows statistics of the processing of different types logic block matrixes with faulty components. It demonstrates correctness of applying the proposed criterion, which shows the optimal and efficient strategy of matrix traversal to obtain minimum coverage of faulty logic blocks by spare tiles in all cases except the last one. In the latest variant the structurization criteria by rows greater than by columns  $Q_r = 1,78 > Q_c = 1,55$  that is the basis of covering the faults by columns. In this case the coverage quality is  $Q_c^* = 1,125$  that corresponds to 16 spare tiles needed to repair all 18 faulty blocks. While the optimal solution is traversal of the matrix by columns, where the coverage quality is  $Q_c^* = 1,2$  that corresponds to 15 spare tiles only.

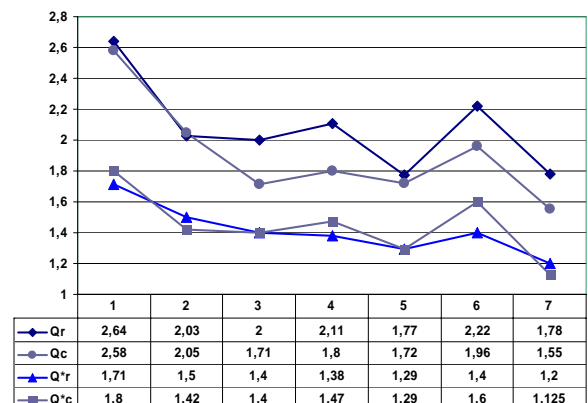


Figure 2. Structurization criteria and coverage quality for the examples

### 3. Software “aGalls” for covering of faulty FPGA components by spare tiles

Software «aGalls» is designed for covering of faulty FPGA components by spare tiles by using the traversal method for logic block matrix.

The initial information is represented by a matrix of tiles  $M = \{M_{ij} | i = \overline{1, p}; j = \overline{1, q}\}$ , the dimension  $p \times q$ , where each tile has  $n \times n$  logic blocks. The initial quantity of faults  $k$  is made to the matrix. The software detects the coordinates of all faults, constructs the binary coverage matrixes for faulty blocks by means of traversing the tiles by columns and rows, and calculates the quality criteria of fault coverage (Fig. 3).

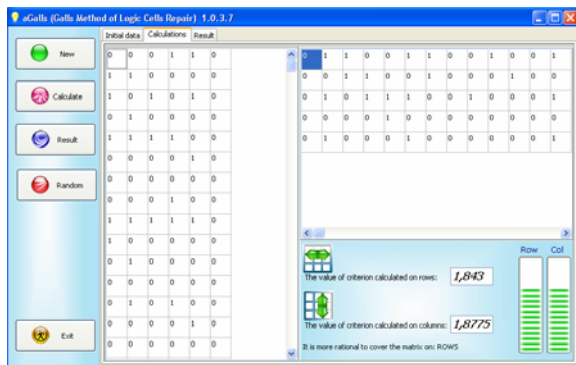


Figure 3. Calculation results

The program provides the opportunity to review the changes of temporary matrixes after covering the faulty blocks both horizontally and vertically. In addition, the actual number of spare tiles needed to cover all faults is displayed; it enables to estimate the correctness of the selected solution on the basis of calculating the criteria (Fig. 4).

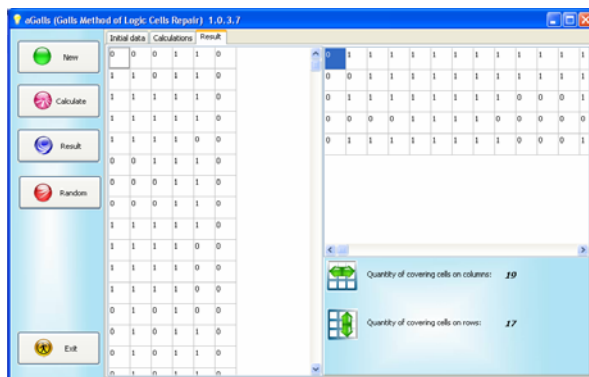


Figure 4. Coverage of a matrix with faults and spares

An algorithm for solving the coverage problem implemented in the software is represented below and in Fig. 5.

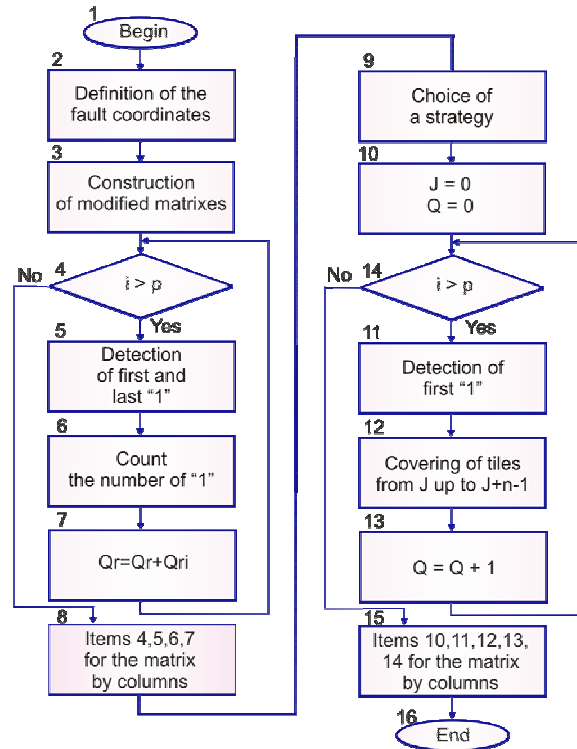


Figure 5. Model of solving the optimal coverage task

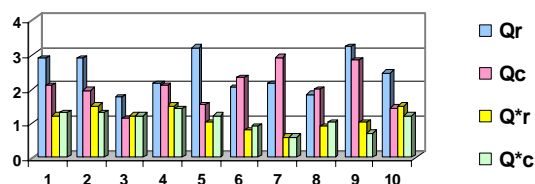
1. Beginning of solving the coverage problem for a logic block matrix by spare tiles.
2. Determination of the coordinates for all faulty blocks of the matrix.
3. Construction of the binary coverage matrixes for faulty blocks to traverse the tiles by rows and columns.
4. Construction the fault coverage for the modified matrix by means of their traversal by rows.
5. Detection the first and last “1”.
6. Counting the number of “1” in a row.
7. Increment number of rows processed.
8. Calculation of the structurization criteria by rows.
9. Implementation of items 4, 5, 6, 7 for columns.
10. The decision on the choice of faulty blocks coverage strategy in the direction corresponding to the lower value of the criterion.
11. Nulling of zero coordinates counter and spare tile counter  $j = 0, Q = 0$ .
12. Sequential scanning of the vector elements  $j = j + 1 \leftarrow M_{ij}^r = 0$  up to the first “1”
13. From this “1” it is counted  $n$  tiles, which are covered by the spare.  $M_{ij}^r = 1 \rightarrow (Q = Q + 1, j = j + n - 1)$  by rows.
14. The value  $Q$  is incremented by 1.
15. If

$j \geq q$  – the end of row proceeding, otherwise – item 11. 16. Implementation of items 10, 11, 12, 13, 14 at traversal by columns. The end of searching the quasioptimal coverage of faulty blocks by spare tiles.

To check the validity of the criteria 200 experiments for the matrix  $M$  was carried out; the dimension of matrix is  $p \times q$ , the number of blocks in the tile is  $n$  horizontally and vertically, and the number of faults is  $k$ , where

$$p = \overline{3,7}; n = \overline{2,5}; q = \overline{3,7}; k = \overline{3, (n \times p \times q)}.$$

As a result, by using the criteria the most efficient way to repair has not been determined in 29% of cases, respectively a positive result – 71%. Fig. 6 presents diagrams showing the values of structurization criteria and coverage quality at the traversal of the modified matrix by rows and columns for the 10 examples. The dimension of the matrix was constant: 4 tiles in the horizontal and 5 ones vertical, the dimension of the tiles was  $3 \times 3$  blocks.



**Figure 6. Structurization criteria and coverage quality**

The software is used to verify and test the method for obtaining the quasioptimal fault coverage by minimum quantity of spare tiles. It can be implemented into a chip as embedded Infrastructure IP component, where the initial information about the topology of a chip has to be memorized during Place and Route process.

#### 4. Conclusion

The traversal method for a logic block matrix is designed to repair the FPGA components by obtainment the solution in the form of quasioptimal coverage for all faulty blocks by minimum number of spare tiles. It is proposed a choice one of two traversal strategies for rows or columns of a logic block matrix on the basis of the structurization criteria, which determine a number of faulty blocks, reduced to the unit modified matrix of rows or columns.

The scientific novelty. The matrix model for FPGA logic blocks in the form of functional tiles, containing faults, is proposed. The model allows repairing of the FPGA components by means of the developed coverage method for faulty logic blocks by spare tiles through traversal of FPGA rows and columns. The method enables to obtain a solution in the form of quasioptimal coverage for a set of faulty blocks by minimum quantity of spare tiles.

The practical significance lies in the attractiveness of the proposed method for the market of electronic technology, which allows determining the minimum number of spares for repair of digital product, implemented into a chip SoC/SiP.

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