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CONTENTS

CO-DESIGN TECHNOLOGY OF SOC BASED ON ACTIVE-HDL 6.2

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It is represented technology of designing and verification of digital systems-on-a-chip (SoC), based on the experience of design of hardware and software components of SoC in one environment. It reflects today situation of variety of available silicon, software and hardware description languages, design tools. There are also presented recommendations and examples.

1. Today's market of design technologies

On today's EDA market there are 3 major target silicon technologies that define computer world today – programmable devices, gate arrays and ASICs. They and relations between them are presented on Fig. 1.

That includes manufacturing technology of silicon chips, hardware and software description languages, design tools, SoC methodology.

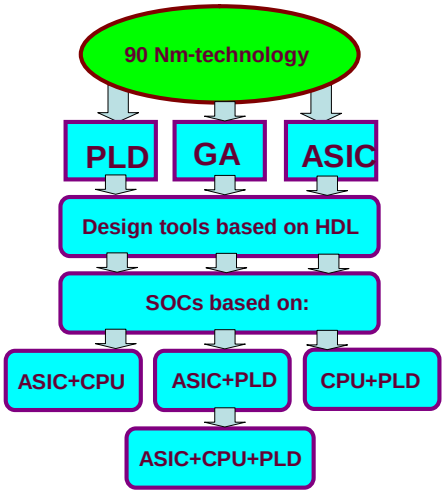

Fig. 1. Cause-effect relation on the EDA market

Practical explanation of presented figure is that because of influence of SoC on ASIC and FPGA (PLD) designs it is started integration between them. On FPGA's started to appear powerful embedded processors such as ARM and PowerPC. For example latest Xilinx Virtex II Pro FPGA is 4 embedded IBM PowerPC processors plus 10 million of programmable gates available for user. Design flows of FPGAs and ASICS also started to merge after announcing by Altera Structured ASIC flow. Where FPGA verified design is transferred to ASIC without any participation of the developer.

That will influence world chip market – that is about $40 billions per year: 1) powerful processors, that are used on servers and working stations; 2) personal computers area, where Intel processors holding the leading place with $20 billions; 3) microcontrollers and signal processes generate to vendors $14 billion revenue every year. The 3rd segment is the most growing one from all three. Hardware development reached stage that number of transistors is growth is 60% per year, but their usage in project growing only 20% per year. That's why we can see today rapid growth of number of SoCs. On that available space on a chip are transferred from the board all buses and peripherals of the developed system. That allows not only increasing productivity of whole digital system and make it with custom functionality, but significantly to reduce energy consumption and decrease physical size of final product. At the same time one of the main requirements of designing complex systems today is to use module approach. Where designer can reuse modules from previous projects or use IP-(Intellectual Property)-core. For SoCs there are bunch of various ready to use processors with peripheral buses and libraries of standard peripherals. With different functionality, sizes, from simple interface to complicated 64bit processors that requires couple of millions transistors.

According to Fig.2 variety of silicon solutions of

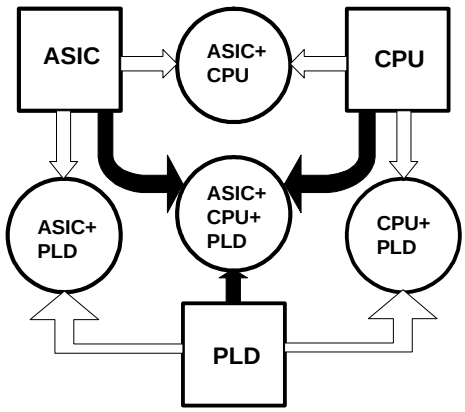

Fig. 2. Types of chips

implementing SoC depends on 3 basic components and all possible combinations between them, that make full set of available on the market components that can satisfy almost every customer. Based on chip technologies available on the microelectronics market the most effective by performance are ASIC: ASIC – Application-Specific Inegrated Circuit – custom IC's, that usually developed by one company for specific need. For example Analog Devices, Infineon, Motorola, Qualcomm, Texas Instruments, EPSON, NEC, others. Such oriented IC's in thousand times are more effective by cost and performance per watt then processors and also significantly reduce board sizes and number of its components. But special-purpose IC's do not have flexibility of reconfiguring. And second disadvantage is the high price of developing and manufacturing ASICs (millions of USD). Reconfigurable PLDs have very high costs per chip but can be purchased in very small volumes. That makes them very attractive for big number of digital systems developers (about 2 billions USD market). Especially when world leading companies in PLD for SoC area Altera and Xilinx enhancing PLDs today with softcore (Xilinx PicoBlaze, MicroBlaze; Altera Nios) and embedded processors as PowerPC and ARM; rocket I/O's, big embedded memory blocks. Latest FPGAs start to be serious alternative to the powerful "fixed" logic. Variety of proposed electronic solutions require proper set of design tools, based on the hardware description languages and software products, that fully or maximally close support IEEE standards. On figure 3 it is presented structure of languages required for system-on-a-chip developer:

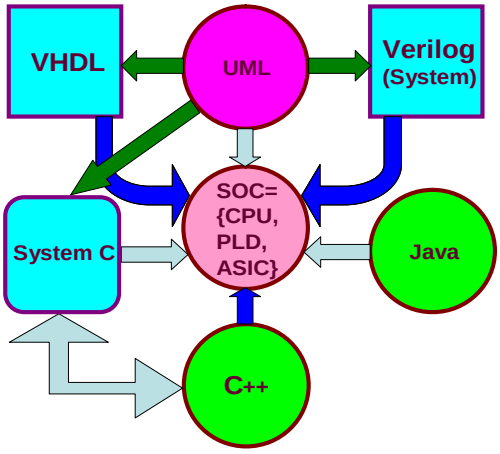

Fig. 3. Language support

Here the dominant group is (Verilog, VHDL, SystemC). They will exist for 5 more years together, competing and supplement each other. Availability of compilers for every of them and also mixed languages simulators allow successfully to use multiple languages blocks in one project together. Such technology is supported by major Electronic Design Automation (EDA) companies (Cadence, Synopsys, Mentor Graphics, Aldec)

Further enhancement receives Unified Modeling language (UML) [7], that is targeted on creation of models and verification of heterogeneous systems. It is enough to say that on 41st DAC'04 whole day was dedicated for discussions to this language in terms of workshop [DAC'04]. Languages C++ and Jawa, oriented on software development for embedded processors of SoC's as ARM, PowerPC, MIPS, others; and on writing modules that participate in logic simulation via programming language interface (PLI) for better and easier debugging and verification.

2. Verification technology of System-on-Chip

Main target – is to create regulated sequence of actions that allows practically utilize software/ hardware co-design solution, presented on figure 4.

To achieve that, 2 main decisions should be made:

1) Creation of the universal model (system level) for design and verification [8,9,10,11] Hardware+Software for SoC, that includes base silicon (PLD, ASIC) and CPU.

2) Configuration of design tools of leading industry vendors that allow finding acceptable SoC or Final System solution by development time, design costs, performance. (see Fig. 4.)

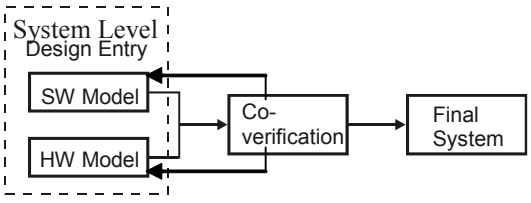

Fig. 4. Model of design process

Following points should be considered as main principles of designing:

1. It is necessary to support several types of specification formalization on the basis of standard hardware description languages.

2. To utilize description method that is more preferable for adequate representation of the project fragment function.

3. To utilize already verified IP-cores blocks

4. To design own logic blocks in way that they can be easily reused in next designs (design reuse)

5. To verify correct functionality by simulation/ emulation whole HW/SW system with embedded processor/processors, IP-cores, user designed blocks, system software in co-simulation environment. Deep HW and SW debug can prevent a lot of further design re-spin cycles and is very important on this stage.

6. To analyze software/hardware behavior components in real time environment.

3. Aldec co-verification technology for ARM based SoCs

In this technology it is used hardcore ARM processor connected to HES-board via AMBA bus [12,13] for purpose of accelerating of logic simulation (Fig. 5) of whole system. HES-board has FPGA chip/chips on it with programmed user logic.

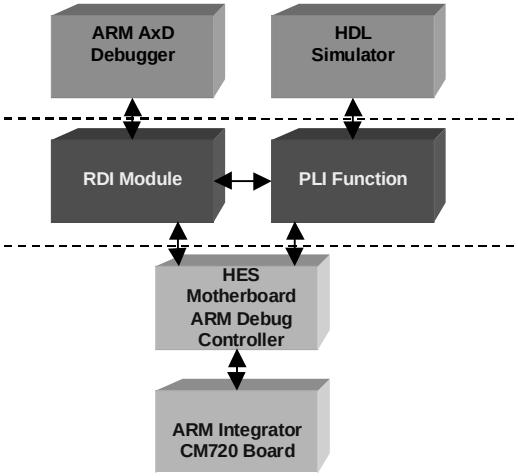

Fig.5. General model of SOC verification process

Here on fig. 5 it is represented general structure of software/hardware components used in design and verification of the system on a chip in Aldec Inc. Four upper blocks are – software products:

1) ARM AxD Debugger for C++/Assembly system software, that works on real time systems and allows to stop simulation on user specified breakpoints, view variables, registers, memory.

2) HDL simulator – in this case it is Active-HDL v.6.2.

3) RDI Module.

4) PLI functions that provide connection and synchronization of the first two blocks and hardware.

5) Hardware Embedded Simulation (HES) board with attached via connectors ARM Integrator CM720 Board. On HES board there is available reconfigurable logic (FPGAs), memory that can be programmed by blocks of user logic and can participate in simulation together with logic simulator. ARM integrated board contains ARM processor that is used in simulation of developed SoC based on ARM processor.

Such configuration significantly increases performance of the debug process of system software (C++/Assembly code) in comparison with methodology of utilizing C-model of ARM processor during logic simulation. So block 1 is oriented on the design entry and verification of the system software. Block 2 is required for design entry and debug of hardware part of the system, described on HDL and representing peripheral modules of the system, that are usually work under control of system software executing on the ARM processor.

Figure 6 illustrates example, where sequence of operations for achieving main goal – hardware implementation of superposition of 2 video streams and their output to the screen.

Conseptual flowgraph of the algorithm (14 states), implemented with the help of Active-HDL v.6.2 [14], is presented on figure 8. Basically it is control machine for the operational unit of the superposition of video streams.

Main functions of designed SoC:

1. Opening of 2 AVI files. One of them is “main animation”, other one is – “background”.

2. Opening 2 frames from opened files.

3. Locating opened frames in the memory on the HES board through peripherals and AMBA bus.

4. Superposition of the frames with the purpose of the uniting images and writing results back to file on a disk.

5. Forming 3 streams of data that deliver 3 video windows with the 2 basic video streams and with result one, after superposition of initial ones. Windows are displayed on workstation through

PLI routines connected to the system under simulation.

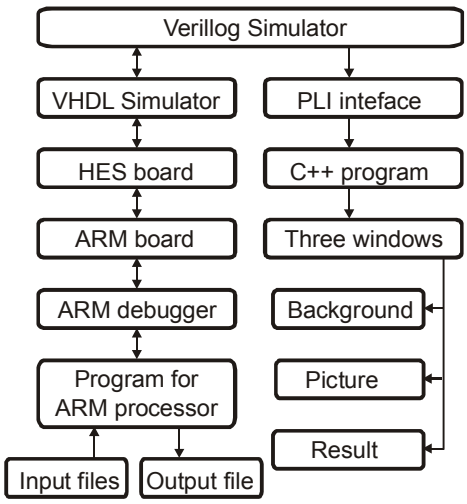

Fig. 6. Model of the design process of the SOC

Following design and verification tools were used: Hardware: HES board 2000; ARM daughter board. Software: Aldec Active-HDL 6.2; ARM Device Suite; Alatek DVM; Xilinx ISE 5.2; Microsoft Visual Studio .NET 2003. PLI interface was used to attach library of functions that were used for nice visualization output results of the system during simulation. For the connection of the peripherals and processor it was used AMBA ASB bus standard. It is 32 bit bus that is widely used in SoC devices based on ARM processor. It provides data flow between processor and peripheral devices.

The system is functioning in the following way: after two AVI files with the same number of frames are opened, the superposition or overlay of their contents is performed and the resulting image is displayed in three separate windows.

It is important to partition functions on software and hardware ones during designing of the system level of the embedded system. In this case it is stimulates to achieve processor controlled system with the high performance at the end of design cycle.

To increase speed of drawing frames on the screen (up to 24 frames per second) it is used RLE8- compression format. This allows to reduce data flow going through AMBA bus, and to make system and visualization to run faster.

In case if there is no available hardware with ARM processor and interface to logic simulator it can be used SystemC model instead. Same system for verification was implemented with Synopsys System C Studio on Solaris OS.

4. Conclusions

Main results that form science and practical meaning for design and verification of system-on-a-chip and should be underlined are:

1. It is presented overview of tools and methods in area of design and verification of digital systems on a chip, including hardware description languages and software products, and also technologies and types of chips available on the electronic technologies market.

2. It is offered technology of designing of software/ hardware tools on the basis of the hardware acceleration that allows to reduce significantly (in 2-10 times) simulation and verification time.

3. It is presented technology of co-verification of hardware and software components of digital system on the basis of utilization together logic simulator, C++/Assembly debugger and hardware accelerator. That allows effectively verify designing digital SoC.

4. It is presented an example of verification of digital device that perform superposition of video streams in one with the output of the result during simulation on the screen through Program Language Interface (PLI) [15]. System is based on the ARM processor, C++ debugger and Active HDL program simulator,

5. It is suggested to utilize video stream as effective test approach to testing of the functions of the autonomously designed digital device. That visually allows seeing “bugs” right on a screen in case if they present in some components of the system and also test all its functions on working frequencies.

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ELECTRICAL TEST IS NOT ENOUGH FOR QUALITY

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Electrical test means Functional Test (FT), In Circuit Test (ICT) or Boundary Scan Test (BST) or even a combination of these technologies. However, with modern technology, like SMD (Surface Mounted Devices) technology, BGA (Ball Grid Array) components and extremely small component dimensions, electrical test alone does not meet the quality requierments.

Electrical test can not identify bad soldering and bad alignment of components, as examples. Missing decoupling capacitors and so on can not be detected because of it is hard to get physical access for testprobes. Do not forget that digital designs contains a lot of analogue devices!

The tutorial will discuss today test technology with equipment for ICT and BST as well as its pros and cons. And as the addition of this, Inspection. Inspection has traditonally been performed manually but this is not realistic today with board crowded by components. Today Inspection is performed by machine vision. Optical technique named Automated Optical Inspection (AOI) and more advanced X-ray inspection (AXI). AOI and AXI is not the future, it is here today.

EMC /EMI is also a growing challenge and some new ideas will be discussed how to test for these phenomenas.

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