KHARKOV NATIONAL UNIVERSITY OF RADIOELECTRONICS

Proceedings of IEEE East-West Design & Test Symposium (EWDTS'09)

SPONSORED BY

IEEE Computer Society Test Technology Technical Council

Moscow, Russia, September 18 – 21, 2009

IEEE EAST-WEST DESIGN AND TEST SYMPOSIUM 2009
ORGANISING COMMITTEE

General Chairs
V. Hahanov – Ukraine
Y. Zorian – USA

General Vice-Chairs
D. Bikov - Russia
R. Ubar – Estonia

Program Chairs
S. Shoukourian – Armenia
D. Speranskiy – Russia

Program Vice-Chairs
M. Renovell – France
Z. Navabi – Iran

Steering Committee
M. Bondarenko – Ukraine
V. Hahanov – Ukraine
R. Ubar – Estonia
Y. Zorian – USA

Publicity Chairs
R.Ubar - Estonia
S. Mosin – Russia

Program Committee
E. Evdokimov – Ukraine
A. Chaterjee – USA
E. Gramatova – Slovakia
S. Hellebrand – Germany
A. Ivanov – Canada
M. Karavay – Russia
V. Kharchenko – Ukraine
K. Kuchukjan – Armenia
A. Matrosova – Russia
V. Melikyan - Armenia
O. Novak – Czech Republic
A. Orailoglu – USA
Z. Peng – Sweden
A. Petrenko – Ukraine
P. Prinetto – Italy
J. Raik – Estonia
A. Romankevich – Ukraine
A. Ryjov – Russia
R. Seinauskas – Lithuania
S. Sharshunov – Russia
A. Singh – USA
J. Skobtsov – Ukraine
A. Stempkovsky – Russia
V. Tverdokhlebov – Russia
V. Vardanian – Armenia
V. Yarmolik – Byelorussia
E. J. Aas – Norway
J. Abraham – USA
M. Adamski – Poland
A . Barkalov – Poland
R. Bazylevych – Ukraine
V. Djigan – Russia
A. Drozd – Ukraine
W. Kuzmicz – Poland

Organizing Committee
S. Chumachenko – Ukraine
N. Kulbakova – Ukraine
V. Obrizan – Ukraine
A. Kamkin – Russia
K.Petrosyanz – Russia
A.Sokolov – Russia
Y.Gubenko – Russia
M.Chupilko – Russia
E. Litvinova – Ukraine
O. Guz – Ukraine
G. Markosyan – Armenia

EWDTS CONTACT INFORMATION

Prof. Vladimir Hahanov
Design Automation Department
Kharkov National University of Radio Electronics,
14 Lenin ave,
Kharkov, 61166, Ukraine.

Tel.: +380 (57)-702-13-26
E-mail: hahanov@kture.kharkov.ua
Web: www.ewdtest.com/conf/

7th IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS 2009)

Moscow, Russia, September 18-21, 2009

The main target of the **IEEE East-West Design & Test Symposium** (EWDTS) is to exchange experiences between scientists and technologies of Eastern and Western Europe, as well as North America and other parts of the world, in the field of design, design automation and test of electronic circuits and systems. The symposium is typically held in countries around the Black Sea, the Baltic Sea and Central Asia region. We cordially invite you to participate and submit your contribution(s) to EWDTS'09 which covers (but is not limited to) the following topics:

- Analog, Mixed-Signal and RF Test
- Analysis and Optimization
- ATPG and High-Level Test
- Built-In Self Test
- Debug and Diagnosis
- Defect/Fault Tolerance and Reliability
- Design for Testability
- Design Verification and Validation
- EDA Tools for Design and Test
- Embedded Software Performance
- Failure Analysis, Defect and Fault
- FPGA Test
- HDL in test and test languages
- High-level Synthesis
- High-Performance Networks and Systems on a Chip
- Low-power Design
- Memory and Processor Test
- Modeling & Fault Simulation
- Network-on-Chip Design & Test
- Modeling and Synthesis of Embedded Systems
- Object-Oriented System Specification and Design
- On-Line Testing
- Power Issues in Design & Test
- Real Time Embedded Systems
- Reliability of Digital Systems
- Scan-Based Techniques
- Self-Repair and Reconfigurable Architectures
- System Level Modeling, Simulation & Test Generation
- System-in-Package and 3D Design & Test
- Using UML for Embedded System Specification
- CAD and EDA Tools, Methods and Algorithms
- Design and Process Engineering
- Logic, Schematic and System Synthesis
- Place and Route
- Thermal, Timing and Electrostatic Analysis of SoCs and Systems on Board
- Wireless and RFID Systems Synthesis
- Digital Satellite Television
- Signal and Information Processing in RF and Communication

The symposium is organized by Kharkov National University of Radio Electronics, in cooperation with Tallinn University of Technology, Institute for System Programming of RAS, and Moscow Institute of Electronics and Mathematics. It is sponsored by the IEEE Computer Society Test Technology Technical Council (TTTC) and financially supported by Cadence, JTAG Technologies, Kaspersky Lab, Synopsys, Mentor Graphics, Tallinn Technical University, Donetsk Institute of Road Transport, Moscow Institute of Electronics and Mathematics, Virage Logic, Echostar, Aldec, Teprocomp, DataArt Lab.

CONTENTS

Algebra-Logical Repair Method for FPGA Logic Blocks

Vladimir Hahanov, Sergey Galagan, Vitaliy Olchovoy, Aleksey Priymak
Computer Engineering Faculty, Kharkov National University of Radioelectronics, Kharkov, Ukraine (e-mail: hahanov@kture.kharkov.ua)

Abstract

An algebra-logical repair method for FPGA functional logic blocks on the basis of solving the coverage problem is proposed. It is focused on implementation into Infrastructure IP for system-on-a chip and system-in-package. A method is designed for providing the operability of FPGA blocks and digital system as a whole. It enables to obtain exact and optimal solution associated with the minimum number of spares needed to repair the FPGA logic components with multiple faults.

1. Introduction

At present there are many scientific publications, which cover SoC/SiP testing, diagnosis and repair problems [1-16, 19-20]. The testing and repair problem for the digital system logic components has a special place, because repair of faulty logic blocks is technologically complicated problem. Existing solutions, which are proposed in published works, can be divided on the following groups:

1. Duplication of logic elements or chip regions to double hardware realization of functionality. When faulty element is detected switching to faultless component by means of a multiplexer is carried out [4]. The FPGA models, proposed by Xilinx, can be applied for repair of Altera FPGA components. At repair the main unit of measure is row or column.
2. Application of genetic algorithms for diagnosis and repair on the basis of off-line FPGA reconfiguration not using external control devices [5]. The fault diagnosis reliability is 99%, repair time is 36 msec instead of 660 sec, required for standard configuration of a project.
3. Time-critical FPGA repairing by means of replacement of local CLBs by redundant spares is proposed in [6,7]. In critically important applications the acceptable integration level for CLB replacement is about 1000 logic blocks.

The repair technologies for digital system logic, implemented on-chip FPGA, are based on existence or introduction of LUT redundancy after place and route procedure execution. Physical faults, which appear in the process of fabrication or operation, become apparent as logical or temporary failure and result in malfunction of a digital system. Faults are tied not only to the gates or LUT components but also to a specified location on a chip. The idea of digital system repairing comes to the removal of a fault element by means of repeated place and route executing after diagnosis. At that two repair technologies are possible: 1) Blockage of a defective area by means of developing the control scripts for long time place and route procedure. But it is not always acceptable for real time digital systems. The approach is oriented to remove the defective areas of any multiplicity. Blockage of the defective areas by means of repeated place and route executing results in repair of a digital system. 2) Place and route executing for repairing of real time digital systems can result in disastrous effects. The technological approach is necessary that allows repairing of the digital system functionality for milliseconds, required for reprogramming FPGA by new bitstream to remove defective areas from chip functionality. The approach is based on preliminary generation of all possible bitstreams for blocking future defective areas by means of their logical relocation to the redundant nonfunctional chip area. The larger a spare area the less a number of bitstreams, which can be generated a priori. Concerning multiple faults, not covered by a spare area, it is necessary to segment a digital project by its decomposition on disjoin parts, which have their own Place and Route maps. In this case a digital system that has n spare segments for n distributed faults can be repaired. The total chip area consists of (n+m) equal parts.

The research objective is to develop a repair method for FPGA logic blocks on the basis of using the redundant chip area.

Problems: 1) Development of an algebra-logical repair method for logic blocks of a digital system on basis of FPGA. 2) Development of a method for logic blocks matrix traversal to cover FPGA faulty components by spare tiles. 3) Analysis of practical results and future research.

2. Algebra-logical repair method for FPGA blocks

The exact repair method for FPGA logic blocks by means of spares is represented. It enables to obtain quasi-optimal solution of coverage problem for faulty cells set by minimum quantity of spares. The method focuses on the implementation of digital system-in-package functionality to the Infrastructure IP. The objective function is minimization of FPGA spares S^t, needed for the repair of faulty blocks in the SiP operation by means of synthesis the disjunctive normal form of fault coverage and subsequent selection of a minimum conjunctive term $(S^t_1, S^t_2, ..., S^t_i, ..., S^t_{m_t}) \in S^t$ that answers the constraints on the number of spares $m_t \le p$, which enter into the logical product:

$$Z = \min_{t=\overline{1,n}}\left(\left|S^t\right|\right)\Big|_{m_t \le p},\ S = (S^1 \vee S^2 \vee ... \vee S^t \vee ... \vee S^n);\ S^* = \{S_1, S_2, ..., S_j, ..., S_p\}.$$

FPGA functionality model is represented by a matrix of logic blocks operating by rows and columns of the structure $M = \left|M_{ij}\right|$. In the process of designing the matrix attached to a spare, consisting of rows and columns, which can be readdressed in the process of structure reconfiguration, when faults are detected.

A model of determining the minimum number of spares (rows and columns), covering all detected faults in a matrix of FPGA logic blocks, comes to the following items:

1. Making a coverage table for detected faulty FPGA blocks by spare rows and columns. To achieve the goal a topological model of testing results for FPGA functionality is considered in the form of matrix, coordinates of which identify detected faults (faultless and faulty blocks):

$$M = \left|M_{ij}\right|, M_{ij} = \begin{cases} 1 \leftarrow T \oplus f = 1; \\ 0 \leftarrow T \oplus f = 0. \end{cases} \quad (1)$$

Here the matrix coordinate is equal to 1 if modulo 2 sum of faultless behaviour for the block f and real test response give 1 value, which corresponds to the defect in a block. After FPGA testing and fixation of all faulty blocks the construction of faults coverage table $Y = \left|Y_{ij}\right|, i = \overline{1,n}; j = \overline{1,m}$ is performed. Here columns correspond to a fault set ("1" coordinates), fixed in the matrix M ($|M| = m$), rows are numbers of columns and rows of FPGA blocks matrix, which cover faults, indicated in columns:

$$Y = \left|Y_{ij}\right|, Y_{ij} = \begin{cases} 1 \leftarrow C_i(R_i) \cap F_j \ne \varnothing; \\ 0 \leftarrow C_i(R_i) \cap F_j = \varnothing. \end{cases} \quad (2)$$

Operating by rows and columns, which contain faults, we can find an optimal solution in the form of fault coverage in the metrics of faulty rows and columns. Then the trivial reassignment procedure is carried out for faulty rows and columns, which replaced by faultless FPGA spare components.

To improve the solution of coverage task one-dimensional vector, concatenated from two sequences C and R by power n = p + q, is used instead of two-dimensional metrics components:

$$X = C*R = (C_1, C_2, ..., C_i, ..., C_p)*(R_1, R_2, ..., R_j, ..., R_q) = X^c * X^r = (X_1, X_2, ..., X_i, ..., X_p, X_{p+1}, X_{p+2}, ..., X_{p+j}, ..., X_{p+q}). \quad (3)$$

At that there is one-to-one correspondence between elements of initial sets (C, R) and resultant vector X that is established in the first column of Y matrix. Transformation $X = C*R$ is carried out for ease of consideration and subsequent construction the disjunctive normal form in the frame of uniformity in the variables, which form the Boolean function. If given procedure is not performed, a function will be defined by variables of two types, which consist rows and columns of a memory matrix.

2. CNF forming by analytic, complete and exact solution of the coverage task. After the forming of a coverage matrix that contains zero and unit coordinates, the synthesis of coverage analytic form by writing CNF for unit coordinates of matrix columns is carried out. A number of conjunctive terms is equal to quantity of table columns, and the length of a disjunctive term is equal to quantity of "1" in the column:

$$Y = \bigwedge_{j=1}^{m} (Y_{pj} \vee Y_{qj})_{\{Y_{pj}, Y_{qj}\}=1} = \bigwedge_{j=1}^{m} (X_{pj} \vee X_{qj}). \quad (4)$$

Last expression shows that every column identifies two variants of fault coverage – rows and columns. So a column has only two coordinates, which have unit value, and numbers of logical products is equal to total quantity of faults m, detected in FPGA matrix.

3. Transformation of CNF to DNF enables to obtain all solutions of the coverage task. For this it is necessary to apply the logical product operation and minimization rules to the conjunctive normal form to get disjunctive normal form:

$$Y = \bigvee_{j=1}^{w} (k_1^j X_1 \wedge k_2^j X_2 \wedge ... \wedge k_i^j X_i \wedge ... \wedge k_n^j X_n), k_i^j = \{0,1\}. \quad (5)$$

The generalize DNF is represented here; a number of terms is equal to $w = 2^n$, n – numbers of rows in the set (C,R) or quantity of variables X in the matrix Y. All possible solutions (fault coverages by spares) are

written by the set of row identifiers for a coverage table. If k_i^j at X_i is equal to zero, X_i is changed to an insignificant variable.

4. Choose the minimum and exact solutions of the coverage task. The procedure involves the determination of minimum length conjunctive terms by Quine in the DNF. Its subsequent transformation to the rows and columns of a memory matrix on basis of earlier correspondence enables to write the minimum coverage (or a set of them) by two-dimensional row and column metrics that satisfies the constraints of the objective function on spare quantity.

5. Realization of reassignment procedure for faulty rows and columns by similar faultless components of FPGA spare.

Example. Fulfills the repair process for FPGA matrix to determine the minimum quantity of spares, covering all faults. The matrix with faults and spares, highlighted by black color [19,20], is shown in Fig. 1.

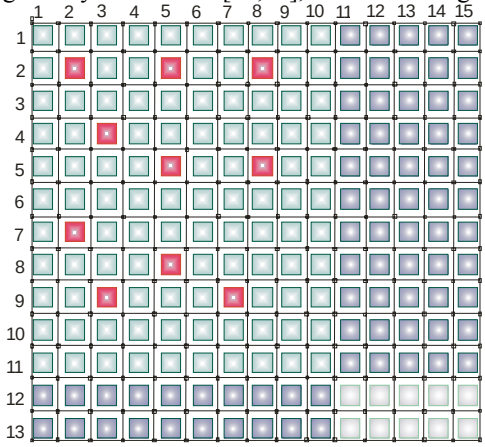

Figure 1. FPGA with faults and spares

The matrix has a spare for diagnosis and repair of faulty cells that is two rows and five columns. According to item 1 of the model for determining the minimum quantity of spares, covering all detected faults of a memory matrix, a coverage table for 10 faults

$$F = (F_{2,2}, F_{2,5}, F_{2,8}, F_{4,3}, F_{5,5}, F_{5,8}, F_{7,2}, F_{8,5}, F_{9,3}, F_{9,7})$$

and eleven rows is formed:

$Y =$

$X_i / F_{i,j}$	$F_{2,2}$	$F_{2,5}$	$F_{2,8}$	$F_{4,3}$	$F_{5,5}$	$F_{5,8}$	$F_{7,2}$	$F_{8,5}$	$F_{9,3}$	$F_{9,7}$
$C_2 \to X_1$	1						1			
$C_3 \to X_2$				1					1	
$C_5 \to X_3$		1			1			1		
$C_7 \to X_4$										1
$C_8 \to X_5$			1			1				
$R_2 \to X_6$	1	1	1							
$R_4 \to X_7$				1						
$R_5 \to X_8$					1	1				
$R_7 \to X_9$							1			
$R_8 \to X_{10}$								1		
$R_9 \to X_{11}$									1	1

(6)

Power or the number of rows in the table is determined by concatenation of columns C and rows R, which are in the one-to-one correspondence with the vector of variables X:

$$C*R = (C_2, C_3, C_5, C_7, C_8)*(R_2, R_4, R_5, R_7, R_8, R_9) \approx \approx X = (X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_9, X_{10}, X_{11}). \quad (7)$$

Construction of CNF is performed by a coverage table by means of writing the terms for unit values of columns:

$$Y = (X_1 \vee X_6)(X_3 \vee X_6)(X_5 \vee X_6)(X_2 \vee X_7)(X_3 \vee X_8) \& \& (X_5 \vee X_8)(X_1 \vee X_9)(X_3 \vee X_{10})(X_2 \vee X_{11})(X_4 \vee X_{11}). \quad (8)$$

Getting of disjunctive normal form is based on the Boolean algebra identities, which allows performing the logical multiplication all ten multiplicands and the subsequent minimization of DNF terms by applying the operator $ab \vee a\bar{b} = a$, absorption axioms and removing the same terms.

The final result is:

$$Y = X_1X_2X_3X_4X_5 \vee X_2X_3X_4X_5X_6X_9 \vee X_1X_2X_3X_4X_6X_8 \vee \vee X_2X_3X_4X_6X_8X_9 \vee X_1X_2X_4X_6X_8X_{10} \vee X_2X_4X_6X_8X_9X_{10} \vee \vee X_1X_4X_6X_7X_8X_{10}X_{11} \vee X_1X_2X_3X_5X_{11} \vee X_2X_3X_5X_6X_9X_{11} \vee \vee X_1X_2X_3X_6X_8X_{11} \vee X_2X_3X_6X_8X_9X_{11} \vee X_1X_2X_6X_8X_{10}X_{11} \vee \vee X_2X_6X_8X_9X_{10}X_{11} \vee X_1X_3X_5X_7X_{11} \vee X_3X_5X_6X_7X_9X_{11} \vee \vee X_1X_3X_6X_7X_8X_{11} \vee X_3X_6X_7X_8X_9X_{11} \vee X_1X_6X_7X_8X_{10}X_{11} \vee \vee X_6X_7X_8X_9X_{10}X_{11}. \quad (9)$$

The choice of minimum length terms with 5 variables in given case determines a set of minimal solutions:

$$Y = X_1X_2X_3X_4X_5 \vee X_1X_2X_3X_5X_{11} \vee X_1X_3X_5X_7X_{11} \quad (10)$$

Transformation of the function to the coverage that contains variables in the form of FPGA rows and columns enables to represent the terms as follows:

$$Y = C_2C_3C_5C_7C_8 \vee C_2C_3C_5C_8R_9 \vee C_2C_5C_8R_4R_9. \quad (11)$$

All minimum solutions satisfy the requirements on quantity of spares, determined by numbers:

$$(|C^r| \le 5) \& (|R^r| \le 2).$$

The subsequent repair technology for faulty FPGA blocks is electrical reprogramming of an address decoder for FPGA column or row. Concerning FPGA shown in Fig. 1 the readdressing of columns with faulty logic blocks to spare columns is realized, for instance, in compliance with first term of (11) that defines the relation:

Faulty column	2	3	5	7	8
Spare column	11	12	13	14	15

.

The computational complexity of an algebra-logical repair method for solving of the coverage task [17,20] is determined by the following expression:

$$Q = 2^{|F|} + |C + R| \times 2^{|F|}, \quad (12)$$

where $2^{|F|}$ – costs related to the synthesis of DNF by means of logical multiplication of two-component disjunctions, the number of which is equal to the quantity of faulty blocks (the fault coordinate is determined by a row or column number); $|C+R|\times 2^{|F|}$ is upper limit of computational cost needed to minimize the DNF on limiting set of variables that is equal to total quantity of rows and columns $|C+R|$.

In the worst case, when the coordinates of all faulty blocks are not correlated by rows and columns (unique), for instance, diagonal faults, computational complexity of the matrix method becomes dependent on the number of faulty cells only, and its analytic form is transformed to the following expression:

$$Q = 2^{|F|} + |C+R|\times 2^{|F|}\Big|_{|C+R|\le 2\times|F|} = \\ = 2^{|F|} + 2\times|F|\times 2^{|F|} = 2^{|F|}\times(1+2\times|F|). \quad (13)$$

If to use the numbers of faults m instead of the power of a fault set the previous expression is represented in simpler form:

$$Q = 2^{m}\times(1+2\times m) = 2^{m}(2m+1). \quad (14)$$

According to the Functional Intellectual Property, an algebra-logical repair method for FPGA logic blocks on the basis of solving the coverage task is implemented into a chip as one of Infrastructure IP components that is designed for support of FPGA blocks and SoC availability.

3. Conclusion

Algebra-logical repair method for FPGA logic blocks on the basis of solving the coverage task is focused on the implementation into a chip as one of Infrastructure IP components. It is designed to repair the FPGA blocks and SiP as a whole.

The method enables to obtain exact and optimal solution associated with the minimum number of spare blocks needed to repair the FPGA logic components with multiple faults.

The technological solutions represented in the survey and proposed methods for diagnosis and repairing of digital system-on-a-chip and system-in-package correlates well with the analytical market research of electronics in 2009 and is formulated in the form of Gartner's Top 10 Strategic Technologies for 2009: 1) Virtualization. 2) Cloud Computing. 3) Servers – Beyond Blades. 4) Web-Oriented Architectures. 5) Enterprise Mashups. 6) Specialized Systems. 7) Social Software and Social Networking. 8) Unified Communications. 9) Business Intelligence. 10) Green IT [http://www.gartner.com/].

As well, the Gartner's Top 10 correlates well with the analytical research of Computer Sciences Corporation (CSC), represented as 7 tendencies: 1) New media. Internet has become a full-fledged framework for creating and using audio, video and text content in a planetary scale. 2) Social software. Social networks attract millions of users, using the common interests. 3) Enhanced Reality. Gradually, but persistently it enters our lives. Virtual reality, where images of the users travel through the virtual worlds, it becomes practical in finding suitable products, services, products without their prior purchase. 4) Transparency of information. It will let you see yourself and the world with a given degree of detail by means of sensors and internet-cameras placed in the office, and throughout the world. The other side of the coin is how to hide and preserve personal space. 5) Wireless innovations. They allow running any application on any device, anywhere in the world. Here we should expect the appearance of conflict related to the division of frequencies between telecommunications operators, radio and television, cable and satellite companies, Internet service providers. It is expected to the integrate solution of the problem on the basis of wireless technologies with mobile Internet-services. 6) New hardware and software platforms. Level of virtualization is increased. The number of applications which function on the same computer under different operating systems is growing exponentially. «Cloud computations», when a consumer pays for the use of computer infrastructure and applications to providers, stored client data on your own servers, significantly alter the entire calculation structure. Prospects of nanotechnologyб molecular, quantum and optical computing become more realistic. Instead of silicon chips lighter and smaller elements: the atoms, DNA, spins of electrons and light will work. 7) Intelligent world. Semantic and networking technologies allow computing devices to interpret the information on the algorithms of natural intelligence, whether text, voice, image, or life situations. Computers will be to teach, give advices, make predictions based on information received from the environment and the individual person. Self-learning semantic retrieval applications is developed in the Internet [http://www.pcweek.ru/].

6. References

[1] Kwang-Ting (Tim) Cheng. The Need for a SiP Design and Test Infrastructure // IEEE Design and Test of Computers.– May–June, 2006.– P. 181.

[2] Fontanelli A. System-in-Package Technology: Opportunities and Challenges // ISQED 2008, 9th International Symposium.– March, 2008.– P. 589 – 593.

[3] Appello D., Bernardi P., Grosso M., Reorda M.S. System-in-package testing: problems and solutions // IEEE Design & Test of Computers.– Vol. 23, Issue 3.– May-June, 2006.– P. 203 – 211.

[4] Subhasish M.; Huang W.-J., Saxena N.R., Yu S.-Y., McCluskey E.J. Reconfigurable architecture for autonomous self-repair // IEEE Design & Test of Computers.– Volume 21, Issue 3.– May-June, 2004.– P. 228-240.

[5] Ross R., Hall R. A FPGA Simulation Using Asexual Genetic Algorithms for Integrated Self-Repair // First NASA/ESA Conference on Volume.– Issue 15-18 June 2006.– P. 301 – 304.

[6] Habermann S., Kothe R., Vierhaus H.T. Built-in self repair by reconfiguration of FPGAs // Proceedings of the 12th IEEE International Symposium on On-Line Testing.– 2006.– P. 187-188.

[7] S. Pontarelli, M. Ottavi, V. Vankamamidi, A. Salsano, F. Lombardi. Reliability Evaluation of Repairable/Reconfigurable FPGAs // 21st IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT'06) .– October, 2006.– P. 227-235.

[8] Koal T., Vierhaus H. T. Basic Architecture for Logic Self Repair // 14th IEEE International On-Line Testing Symposium.– 2008.– P. 177–178.

[9] Kothe R., Vierhaus H.T., Coym T., Vermeiren W., Straube B. Embedded Self Repair by Transistor and Gate Level Reconfiguration // IEEE Design and Diagnostics of Electronic Circuits and Systems.– 2006.– P. 208–213.

[10] Mange D., Sipper M., Stauffer A., Tempesti G. Toward self-repairing and self-replicating hardware: the Embryonics approach // Evolvable Hardware, Proceedings of the Second NASA/DoD Workshop.– 2000.– P. 205-214.

[11] Miclea L., Szilard E., Benso A. Intelligent agents and BIST/BISR – working together in distributed systems // Proceedings of the Test Conference.– 2002.– P. 940-946.

[12] Rashad S. Oreifej, Carthik A. Sharma, Ronald F. DeMara. Expediting GA-Based Evolution Using Group Testing Techniques for Reconfigurable Hardware // Reconfigurable Computing and FPGA's, 2006.– Sept., 2006.– P. 1-8.

[13] Anand D., Cowan B., Farnsworth O., Jakobsen P., Oakland S., Ouellette M.R., Wheater D.L. An on-chip self-repair calculation and fusing methodology // IEEE Design & Test of Computers.– Volume 20, Issue 5.– Sept.-Oct., 2003.– P. 67-75.

[14] Wang S.-J., Tsai T.-M. Test and diagnosis of faulty logic blocks in FPGAs // IEEE Proceedings Computers and Digital Techniques.– Vol. 146, Issue 2.– March, 1999.– P.100 – 106.

[15] Pontarelli S., Cardarilli G.C., Malvoni A,. Ottavi M., Re M., Salsano A. System-on-chip oriented faulttolerant sequential systems implementation methodology // IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems.– Oct., 2001.– P. 455 – 460.

[16] Peter Rickert, William Krenik. Cell Phone Integration: SiP, SoC, and PoP // IEEE Design and Test of Computers.– May–June, 2006.– P. 188-195.

[17] Rossen K. Discrete Mathematics and its Applications, McGraw Hill, 2003. 824p.

[18] IEEE 1500 Web Site. http://grouper.ieee.org/groups/1500/.

[19] Hahanov V., Hahanova A., Chumachenko S., Galagan S. Diagnosis and repair method of SoC memory // WSEAS transactions on circuits and systems.– Vol.7.– 2008.– P. 698-707.

[20] Hahanov V., Obrizan V., Litvinova E., Ka Lok Man. Algebra-logical diagnosis model for SoC F-IP // WSEAS transactions on circuits and systems.– Vol. 7.– 2008.– P. 708-717.

Camera-ready was prepared in Kharkov National University of Radio Electronics
by Dr. Svetlana Chumachenko
Lenin ave, 14, KNURE, Kharkov, 61166, Ukraine

Approved for publication: 31.08.2009. Format 60×841/8.
Relative printer's sheets: . Circulation: 150 copies.
Published by SPD FL Stepanov V.V.
Ukraine, 61168, Kharkov, Ak. Pavlova st., 311

Матеріали симпозіуму «Схід-Захід Проектування та Діагностування – 2009»
Макет підготовлено у Харківському національному університеті радіоелектроніки
Редактори: Володимир Хаханов, Світлана Чумаченко
Пр. Леніна, 14, ХНУРЕ, Харків, 61166, Україна

Підписано до публікації: 31.08.2009. Формат 60×84$^{1}/_{8}$.
Умов. друк. арк. . Тираж: 150 прим.
Видано: СПД ФЛ Степанов В.В.
Вул. Ак. Павлова, 311, Харків, 61168, Україна