Optimization Factors in Modeling and Testing Hardware and Semiconductor Defects by Dynamic Discrete Event Simulation

Jack H. Arabian

***Index Terms* — Optimization, Semiconductors, Production, Testing, Process, Mapping, Modeling, Simulation, System of Systems, Six Sigma, Estimation.**

I. Introduction

TESTING of Hardware and Product in the Semiconductor Production Process presented a challenge to the collection of data to resolve cost and production issues. As described in reference [1], it has been shown that the Process can be modeled and run with respect to maximizing the output of the model for typical parameters of cost, time, and resources.

It remained, however to optimize the human resources with respect to maximizing the output of the model. This paper describes an optimizing technique/tool, which can be used for a manufacturing test process identifying defects to predict/estimate and optimize costs, scheduling and needed resources.

II. Requirements

Given the model described in [1], the following steps were taken:

1. Determine the parameters to be optimized
2. Install the parameters in the model
3. Run the optimization tool [ProcessModel™, Provo, UT 84601]

III. Procedure

1. After the mapping of the Semiconductor Manufacturing and Test process, (Figure 1 below), we used a commercial process mapping application, and its built-in optimizer called SimRunner™. In the dynamic model, we wanted to maximize the output of the two different wafer slices (called Dice_1 and Dice_2) after reaching the Dicing step. The Test and Burn-in step was used for costing analysis, but it can be seen that a similar series of steps using the Pass/Reject and Re-Do steps can be used wherever a testing step, e.g., Wafer Test, needs to be performed.

2. For purposes of this paper, the optimizing of the human resources to maximize output suffices to simplify the concept.

3. In [1], we used three scenarios of parameters for Fig. 1. The mapping application conveniently ran the scenarios and automatically calculated the cost and other results. Fig. 1 was reduced in scale to fit on the page, but it can be expanded electronically.

4. Note that for this paper, a human resource pool icon (named "Worker Pool), was added, and each of the process steps were connected to the icon. The metric "S" was designated the variable to be optimized (and minimized) for maximum output as explained above. The SimRunner table shown in Figure 2 demonstrates the inputs required for the optimizer.

5. The simulator was then run several times by the SimRunner optimizer in its search for the parameters which met the requirement. A mathematical equation within SimRunner describing an Objective Function provides the parameter which, when calculated and plotted, provides the insight to the optimum process. The plot of the Objective Function against the eight runs needed to converge on the optimum is shown in Fig. 3.

6. After the run of quantity eight (8) experiments, the optimizer converges on the best solution. Experiment 1 shows the best solution of Minimum quantity four (4) workers from the Worker Pool, and the Maximum NumberOfDice_1=1400.000 and Maximum NumberOfDice_2=1000.000, as shown in Fig. 4.

IV. Conclusion

Process Mapping and Dynamic Time Simulation is very useful for a manufacturing test process identifying defects to predict/estimate costs, scheduling and needed resources.

Reference [1] showed the previous outcome of metrics, and this paper shows how to optimize the human resources with the process output. This is another compelling argument for QA engineers to justify up-front costs of JTAG (Joint Test Action Group for boundary scan) or BIST (Built-in Self Test) circuitry in design phases.

In addition, there are other advantages to modeling a process, viz.

1. Additional parameters are listed after each simulation run in a longer and detailed comprehensive report (6 pages), which is automatically generated.

2. Additional bar graphs, pie charts, cost summaries, and plots are automatically generated using this technique.

3. Model parameters are exported to a spreadsheet, and global changes can be made as needed in the spreadsheet. Changes are then successfully imported directly into the model to create a new scenario to generate new estimates.

4. This technique becomes immediately extendable to appended systems to create a system of systems (SoS) model, by escalating upwards to a higher architectural level.

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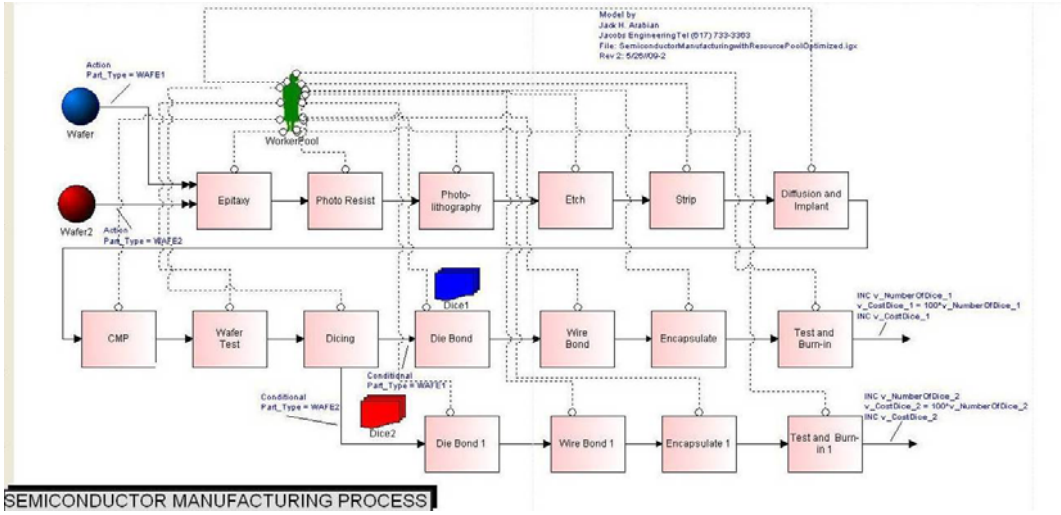

Fig. 1. Model of the Semiconductor Manufacturing and Testing Process

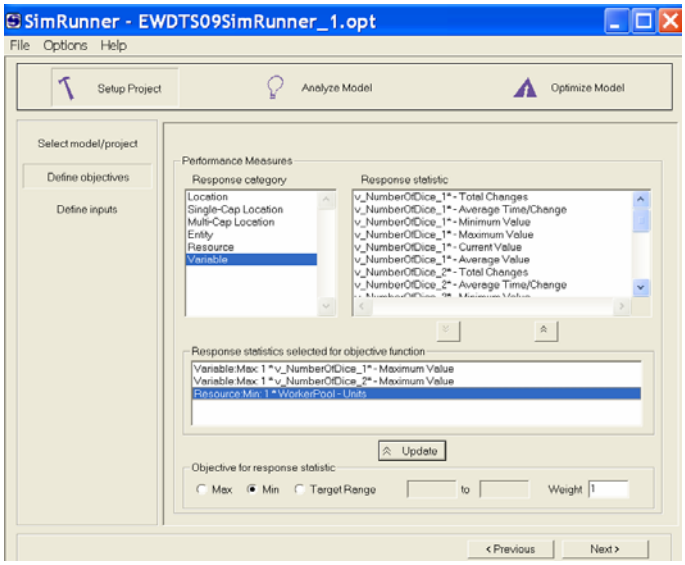

Fig. 2. SimRunner Table for Optimizer Inputs

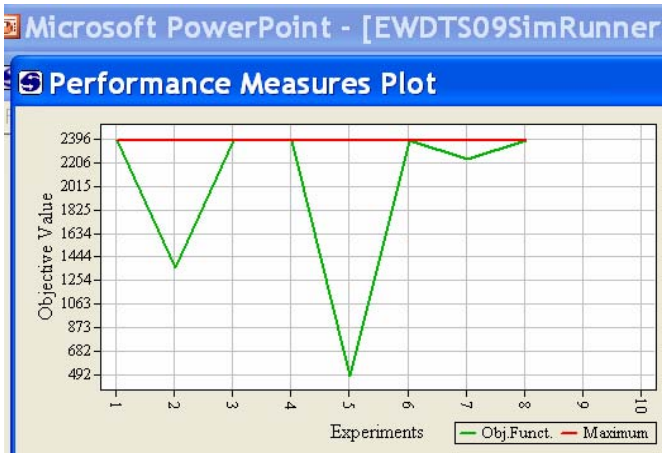

Fig. 3. Plot of Objective Function vs. Simulator Runs (Experiments)

V. Live Demo

For this presentation, a 10-minute live demonstration of SimRunner™ optimizer shows dynamic, graphic animation of the test runs automatically generated until the optimizer's Objective Function converges on the best solution

VI. Future Work

This model is generic to many manufacturing and test processes in which defects can occur, as, e.g., hardware defects found in testing on a manufacturing production line. Many other aspects need to be shown, such as importing of global parameters from a spreadsheet instead of tedious insertion of parameters in each step of a long process. Process mapping and dynamic time simulation will also lead to future work in creating a true System of Systems (SoS) model through the ability to connect multiple processes and raise levels of abstraction, which are otherwise not easy to achieve.

In conjunction with Quality Assurance and Six Sigma practices, other processes can be similarly treated such as in business (order process, Help desk), finance (transactions), healthcare (claims processing), aerospace (radar tracking, checklist, countdown, communications, command and control) and shipbuilding (welding, supply chain).

Acknowledgment

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References

[1] Selected Cost Factors in Modeling and Testing Hardware and Semiconductor Defects by Dynamic Discrete Event Simulation; IEEE Proceedings East-West Design and Test Symposium 2008, Lvov, Ukraine, September 2008. By Jack H. Arabian, Engineering Specialist, Jacobs Engineering & Technology Division, Bedford, MA 01731

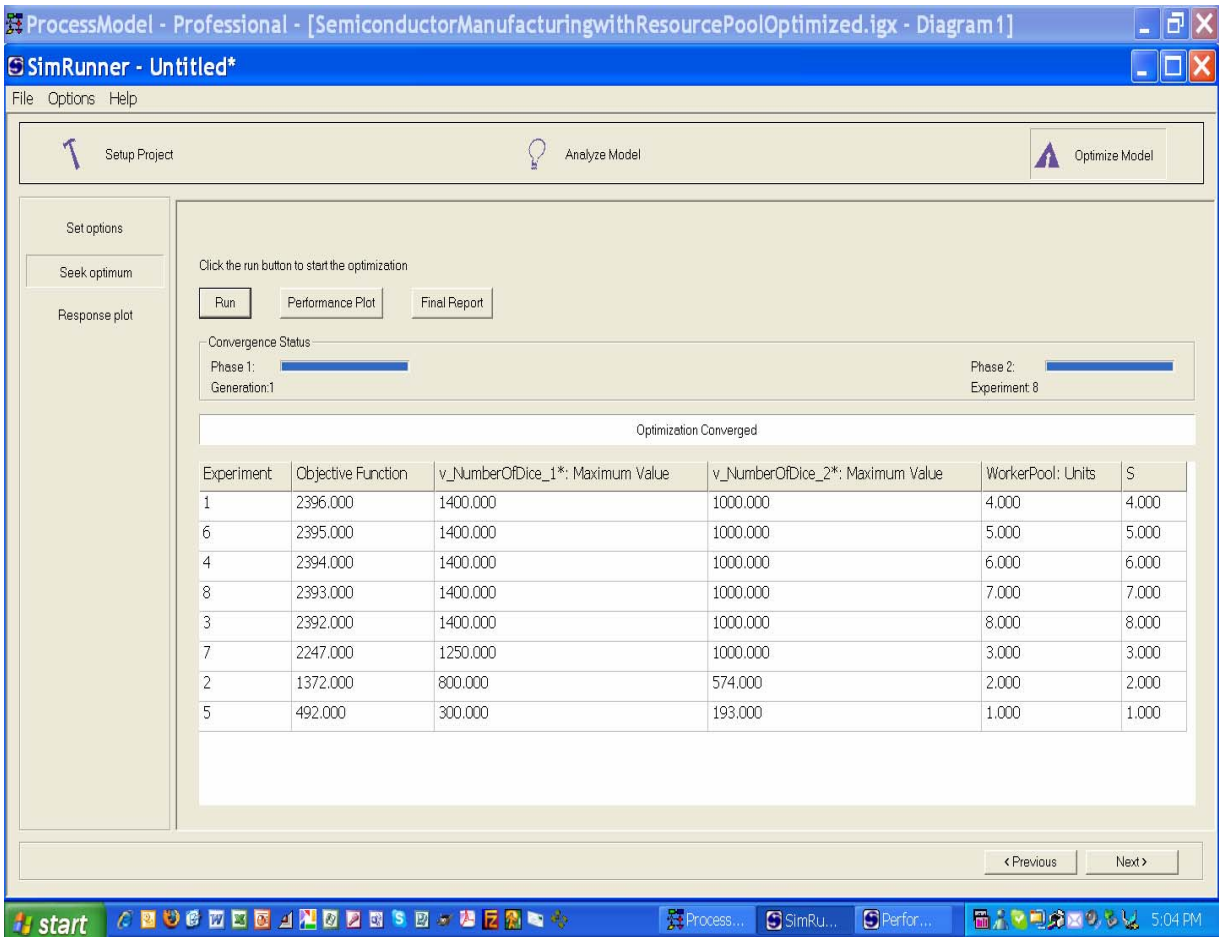

Fig. 4. SimRunner Optimizer Converging on Best Solution

As founder of Comparative Management Associates, LLC **Jack Arabian** provides process mapping, modeling and simulation on a contract, consulting basis. He has trained many corporate groups on the topics of process improvement, process mapping and simulation, software and hardware defect detection and correction, engineering design and applications, manufacturing, & finance.

His forthcoming book, Process Modeling & Simulation for All Organizations, will be his fourth, including Computer Integrated Electronics Manufacturing and Testing, and Concurrent and Comparative Discrete Event Simulation, the standard references for manufacturing engineers and designers of automated factories.

In a distinguished career with such innovative companies as Westinghouse, Polaroid, Foxboro Company, and Digital Equipment Corporation, Jack led the design and development of highly successful hardware and software products in the aerospace systems industry. He has built, led, and mentored high performance design and engineering teams, and taken technology from the laboratory to the customer, with consistently high levels of success in terms of both product quality and profitability.

At the MIT Instrumentation Laboratory, Jack played a key leadership role in solving the problem of gyroscope drift in space navigation. The results proved critical to the success of the lunar landing program, including the safe return of Apollo 13 after a crippling explosion, and later to the development of commercial aircraft inertial navigation systems.

At both Foxboro Company and Polaroid, Jack developed innovative automated test equipment that allowed the restructuring of complex factory production lines, doubling both production and quality while decreasing time to market by as much as 30%.

While at Digital, Jack was instrumental in testing computers through modeling and simulation programs, a technique that developed a reputation and a book on the subject. This technique is now used to enhance and accelerate process development and reengineering.

A graduate of Harvard University (B.A., Engineering Sciences and Applied Physics) and Massachusetts Institute of Technology (M.S., Instrumentation), Jack has extensive global experience. He is proficient in five languages, including Armenian, Japanese, Spanish, and French.

In addition to his four books, Jack is the author of numerous papers on a wide variety of technical and managerial topics, a frequent after-dinner speaker, and a presenter at leading international conferences, such as the IEEE International Test Conference, and symposia.