Research digital devices by means of modelling system on the basis of *K*-Value differential calculus

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***Abstract* – Given article is devoted to the description of new system's of simulation, which based on the mathematical device of *K*-Value differential calculus, possibilities. This system intend for research the complex high-speed devices constructed with usage of modern technologies.**

***Index Terms* – CAD, elements models, equations with delay, fuzzy fronts, *K*-Value differential calculation, simulation, switching capacity.**

I. Introduction

Now computer simulation of digital devices behavior is an integral part of automation's systems of their designing and verification. By means of simulation in systems of electronic devices computer-aided design solve such tasks as definition of installation's chains signals of digital devices and their subsequent logical operation, optimization of synchronization's chains parameters and time characteristics of switching, the analysis of signals competitions, definitions of signals distribution's time and their delays, constructions of checking tests and checks of their entirety [1 – 3]. Thus complexity of modern electronic devices, high frequency of their operation demand appropriate new methods of the analysis of their operation correctness with usage of quantitative and qualitative characteristics of possibility of failures appearance in them

Complexity of modern digital single-crystal systems (System On Chip – SOC) and necessity of rise of their simulation's reliability have led to necessity of many-valued alphabets usage instead of traditional binary. The least labor-consuming is simulation by means of the three-value Eihelberger's alphabet [2] using three characters ("unit", "zero" and "uncertainty" (X)). This alphabet allows considering two steady states at simulation, and the others it represents all as uncertainty. Some extension of three-value simulation is five-digit which in addition uses the characters, enabling to distinguish smooth transitions from competitions of signals.

Fantozi alphabet [3] contains nine characters and allows to differentiate already at simulation static and dynamic risks of failures as to three characters of Eihelberger's alphabet such states as smooth transition from "0" in "1" (*E*), smooth transition from "1" in "0" (H) are added, static risk of failure in "0" (*P*), static risk of failure in "1" (*V*), dynamic risk of failure from "0" in "1" (*F*), dynamic risk of failure from "1" in "0" (*L*). Introduction of four more characters: O (transition from uncertainty in "0"), I (transition from uncertainty in "1"), *A* (transition from "0" in uncertainty) and *B* (transition from "1" in uncertainty), has allowed to distinguish phases of uncertainty and stability [4]. Application of logical many-valued operators enables to differentiate risks of failures, races and competitions of signals that are rather essential to combinative devices where it is necessary to find critical places (structural components) with a view of their subsequent modification and elimination of competitions [5].

At the same time, in known systems simulation of a new class processes and physical faults which are caused by usage of high frequencies of units operation is complicated and are linked to essential increase of a role of signals distribution on explorers of digital devices time parameters. Besides in similar systems there is no possibility to parse influence of increase quantitative parameters and recession of logical signals which are defined by power of switching.

The purpose of article is the description of the new automated system of the complex high-speed devices constructed with usage of modern technologies verification, which basis the mathematical device of *K*-value differential calculus [6, 7]

II. Formation of *K*-value computer elements models

The developed system is based on the mathematical device of *K*-Value differential calculus. This method is development on idea of Boolean differential calculus [1], but, as against it, allows taking into account dynamics of fronts of switching logic signals. The mathematical apparatus of the system of automated designing on the basis

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of *K*-Value differential calculus is guided by use of *K*-Value functions, i.e. the functions accepting values from set of integers {0, 1, …, *K*–1} during the discrete moments of time t_i = 0, 1, …, *N*. In this case logic signals quantize on amplitude and receive corresponding values of the whole *K*-Value numbers. Processing of these values is conducted on the basis of use of *K*-Value derivatives which can be entered as follows:

$$\frac{dF^{\Delta}(t_i)}{dt_i} = \frac{F(t_i + \Delta t)\langle - \rangle_k F(t_i - \Delta t)}{2\Delta t};$$

$$\frac{dF^{-}(t_i)}{dt_i} = \frac{F(t_i)\langle - \rangle_k F(t_i - \Delta t)}{\Delta t};$$

$$\frac{dF^{+}(t_i)}{dt_i} = \frac{F(t_i + \Delta t)\langle - \rangle_k F(t_i)}{\Delta t},$$

where $\langle - \rangle_k$ – operation of subtraction on module *K*; $F(t_i)$ – the function, accepting value from set [0, 1, …, *K*–1] during the discrete moments of time t_i = 0, 1, …, *N*; Δt = 1 – the minimal increment of an independent variable t_i.

From the entered definitions of derivative of *K*-Value functions in practice is used only such reception of *K*-Value derivatives, when values of *K*-Value functions during the current and previous moments of time are known. With the help of such *K*-Value differential operator any element digital computing can be described. Basic logic *K*-Value operations above *K*-Value operands are entered according to tables Kelly [2]. Besides the use of *K*-Value derivatives there is an opportunity to make calculation only at the moment of switching entrance signals that is at the moment of time when the *K*-Value derivative is not equal to zero. It allows reducing considerably time expenses at simulation devices of the big complexity.

Any element of digital computers in developed CAD is described by system of the *K*-Value differential equations with the late argument, looking like:

$$\begin{cases} \dfrac{dU_{\text{out}1}(t_i)}{dt_i} = f(U_{\text{out}1}(t_i - 1), U'_{\text{out}1}(t_i - D_1), \\ \qquad U'_{\text{inp}11}(t_i - D_1), U'_{\text{inp}12}(t_i - D_1), \cdots, \\ \qquad U'_{\text{inp}1N_1}(t_i - D_1), t_i), \ t_i \ge t_0; \\ \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\ \dfrac{dU_{\text{out}M}(t_i)}{dt_i} = f(U_{\text{out}M}(t_i - 1), U'_{\text{out}M}(t_i - D_M), \\ \qquad U'_{\text{out}M1}(t_i - D_1), U'_{\text{out}M2}(t_i - D_M), \cdots, \\ \qquad U'_{\text{out}MN_M}(t_i - D_M), t_i), \ t_i \ge t_0, \end{cases}$$

where $\dfrac{dU_{\text{out}j}(t_i)}{dt_i}$ – value of derivative of unknown target signal $U_{\text{out}j}(t_i)$ *j*'s internal logic block at the moment of time t_i; $j = \overline{1, M}$; *M* – quantity of outputs of an element; $U'_{\text{out}j}(t_i - D_j)$ and $U'_{\text{inp}jw}(t_i - D_j)$ – the modified values of *j*'s target signal $U_{\text{out}j}(t_i - D_j)$ and *jw*'s input signal $U'_{\text{inp}jw}(t_i - D_j)$ logic element at a moment of time $(t_i - D_j)$; $jw = \overline{11,\ MN_M}$; $j = \overline{1, M}$; $w = \overline{1,\ N_M}$.

D_j – delay of *j*'s logic block of the device, $j = \overline{1, M}$.

Presence of late argument gives an opportunity to description and simulation elements with feedback, such, for example, as elements with memory. Thus the size of delay not necessarily should have some unique value. For various internal logic units of an element it can accept various values. These values, in turn, also can vary in limits from minimal up to the maximal size of delay of element. It provides simulation an element with floating delays of its internal units.

As arguments of the *K*-Value differential equations making system, their switching modified in view of capacity, value of entrance, intermediate and target signals of an element are entered. This updating is carried out according to expression:

$$U'_{\text{out}j}(t_i - D_j) = \begin{cases} U_{\text{out}j}(t_i - D_j), \text{if } \widetilde{E}^{j}_{\text{out}}(t_i - D_j) < \widetilde{E}_p, \\ \qquad j = \overline{1, M}; \\ K - 1, \text{if } (\widetilde{E}^{j}_{\text{out}}(t_i - D_j) \ge \widetilde{E}_p), \\ \qquad U_{st\_\text{в}j}(t_i - D_j) = 0, \ j = \overline{1, M}; \\ 0, \text{if } (\widetilde{E}^{j}_{\text{out}}(t_i - D_j) \ge \widetilde{E}_p), \\ \qquad U_{st\_\text{в}j}(t_i - D_j) = K - 1, \ j = \overline{1, M}; \end{cases}$$

$$U'_{\text{inp}jw}(t_i - D_j) = \begin{cases} U_{\text{inp}jw}(t_i - D_j), \text{if } \widetilde{E}^{j}_{w}(t_i - D) < \widetilde{E}_p, \\ \qquad w = \overline{1, N_j}; \\ K - 1, \text{if } (\widetilde{E}^{j}_{w}(t_i - D_j) \ge \widetilde{E}_p), \\ \qquad U^{j}_{stw}(t_i - D_j) = 0, \ w = \overline{1, N_j}; \\ 0, \text{if } (\widetilde{E}^{j}_{w}(t_i - D_j) \ge \widetilde{E}_p), \\ \qquad U^{j}_{stw}(t_i - D_j) = K - 1, \ w = \overline{1, N_j}, \end{cases}$$

where $\widetilde{E}^{j}_{\text{out}}(t_i - D_j)$ and $\widetilde{E}^{j}_{w}(t_i - D_j)$ – the saved up value of capacity of switching *j*'s output and *jw*'s input signal on moment of time $(t_i - D_j)$; $\widetilde{E}_p$ – Discrete analogue of threshold power of switching; $U_{st\_\text{в}j}(t_i - D_j)$ and

$U^{j}_{stw}(t_i - D_j)$ – the saved up value of *j*'s output and *jw*'s input signal, fixed before the beginning of transient process.

Saved up by the moment of time $(t_i - D_j)$ capacities of signals are defined according to the following expressions:

$$\widetilde{E}^{j}_{\text{out}}(t_i - D_j) = \begin{cases} 0, \ U_{\text{out}\,j}(t_i - D_j) \in \{0, K-1\}, \\ \qquad\qquad t_i > 0; \\ \sum\limits_{t_k = t_{s\_\text{в}\,j}}^{t_i - D_j} [U_{\text{out}\,j}(t_k)(\widetilde{U}_{\max} - \widetilde{U}_{\min}) + \\ \qquad + \widetilde{U}_{\min} \times (K-1)]^2, \\ \quad U_{\text{out}\,j}(t_i - D_j) \notin \{0, K-1\}, \\ \quad t_i > 0; \\ 0, \ \text{if} \quad t_i = 0, \end{cases}$$

where $\widetilde{U}_{\min}$, $\widetilde{U}_{\max}$ – integer analogues of levels the voltage corresponding logic unit and logic zero; $t_{s\_\text{в}\,j}$ – the moment of the beginning of transient of switching *j*'s target signal from one steady condition in another:

$$t_{s\_\text{в}\,j} = \begin{cases} (t_i - D_j), \ U_{\text{вых}\,j}(t_i - D_j) \in \{0, K-1\}, t_i > 0; \\ t_{s\_\text{в}\,j}, \ U_{\text{вых}\,j}(t_i - D_j) \notin \{0, K-1\}, t_i > 0; \\ -D_j, t_i = 0; \end{cases}$$

The size of delay D_j *j*'s internal logic unit of an element accepts the value from set T_{zj} possible sizes of delays of unit. Unit T_{zj} depends on values of typical, minimal and maximal delays of an element and can be set by function $f_T(t_{\text{z\_opt}}, t_{\text{z\_min}}, t_{\text{z\_max}}, Ctrl\_T)$. Signal $Ctrl\_T$ represents the managing signal determining a way of the task of this set:

– if $Ctrl\_T = 0$, then set of all values of delays is reduced to a typical delay of an element ($T_{z_j} = \{t_{\text{z\_opt}}\}$);

– if $Ctrl\_T = 1$, then set contains typical, minimal and maximal sizes of a delay ($T_{z_j} = \{t_{\text{z\_min}}, t_{\text{z\_opt}}, t_{\text{z\_max}}\}$);

– if $Ctrl\_T = 2$ or $Ctrl\_T = 3$, then set T_{z_j} contains possible values of a delay which are defined in conformity by the law of distribution of the random variable describing a deviation of a delay from its typical value. This random variable has the normal law of distribution which parameters are defined by the minimal, maximal and typical sizes of a delay of logic unit.

– if $Ctrl\_T = 4$, then set T_{z_j} contains except for typical value also the delays of an element deviating from $t_{\text{z\_opt}}$ on size τ, equal to duration of its transitive process of switching from one steady condition in another ($T_{z_j} = \{\text{Round}(t_{\text{z\_opt}} - \tau), t_{\text{z\_opt}}, \text{Round}(t_{\text{z\_opt}} + \tau)\}$).

In the developed system of the automated designing on the basis of *K*-Value differential calculus general model of an element of digital computers which can contain in structure *M* of logic internal units, each of which has one exit and N_j entrances ($j = \overline{1, M}$), is set by the structure resulted on the fig. 1.

The mainframe of the given structure is the block 1 which is intended for the decision system of the *K*-Value differential equations with late argument. The structure of an element also includes the block 4 which are carrying out initialization of an element which consists in definition of the sizes of buffers at their initial filling. Before signals, which are removed from buffer elements will arrive on the solving block of system of the *K*-Value differential equations (the block 1), their values can be changed with depending on power of switching of elements. This analysis is carried out in the block 5 which is intended for calculation of power of entrance and target signals. On an input of this block are act signals, which are removed from entrance and target buffer elements. And their values are removed from an output of this block with the account of power analysis already.

The signal *Ctrl* define the stage of initialization or a stage of modelling is carried out. And if the stage of modelling is defines, can be two variants – calculation values of a target signal with modeling or updating of buffer elements gets out.

For maintenance of simulation with floating delays the structure resulted on fig. 1, includes the block 7 which are carrying out formation of sets of allowable sizes of delays of logic unit of an element. Thus required accuracy of the analysis is defined by signal *Ctrl_T* according to which the specified set is formed.

Besides the above described blocks, structure of the generalized structure (fig. 1) contains also the block 6 intended for switching of entrance signals of an element and target signals of internal logic units. Thus this block forms sets of entrance signals for each internal element.

Depending on features of functioning of the projected device and the requirements showed to the spent analysis of their serviceability in developed system on the basis of *K*-Value differential calculus it is possible to use both full model of an element, and its separate individual kinds. Use of these models is defined by the chosen mode of simulation.

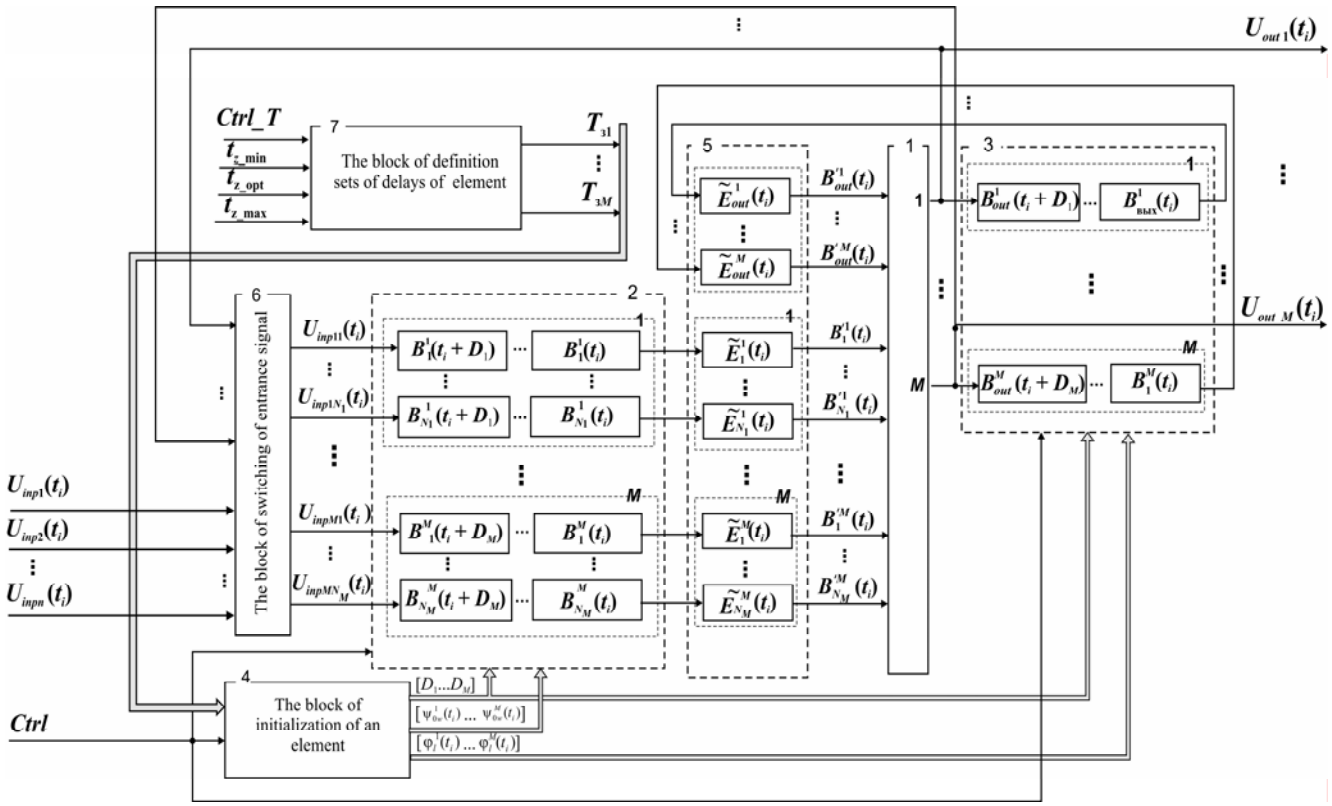

Fig. 1. Structure of general model of an element of digital computers on the basis of *K*-Value differential calculus

In developed system it is allocated four basic modes of simulation:

Mode of modeling 1. It is connected to the description of functioning of elements the *K*-Value differential equations with delay. At a choice of the first mode in the structure of an element resulted on fig. 2 block of power analysis works as the transfer buffer. Thus values of the signals, acting on its input without change are transferred to the block 1. Besides on an output of the block of formation of delays of internal logic units of an element of set T_{z_j} contain only typical values.

Mode of modeling 2. This mode corresponds to the description of functioning of elements *the K*-Value differential equations with delay in view of capacity of switching of entrance and target signals. In this mode on structure of an element the block of power analysis completely functions. It allows to execute simulation of an element in view of capacity of switching of entrance and target signals. In this case as delays of elements their typical values are used only.

Mode of modeling 3. This mode corresponds to simulation with "floating" delays at use the description of functioning of elements by the *K*-Value differential equations with delay.

In this case the element is represented by full structure in which the block 5 of power analysis, however, does not function, i.e. signals on an output of this block fully comply with signals on its input

Mode of modeling 4. This mode represents a mode of simulation with "floating" delays and the account of capacity of switching of entrance and target signals at use of the description of functioning of elements by the *K*-Value differential equations with delay. At a choice of the fourth mode of simulation all blocks which are included in structure of an element are in working order that allows executing the complex analysis of serviceability of the device with use of all opportunities incorporated in developed system.

III. Research of failures risks with use of modelling on the basis of *K*-value differential calculus

Now development of new and perspective devices is fulfilled on the basis of usage of CMOS-technology. However with implantation in process of CMOS-technology's production there was a new class of physical faults which appear in change of signals distribution time [8]. Correct operation of the digital device in this case is possible only when times of signals distribution along explorers of the logic circuit lay in the certain limits. When time of a signal's distribution quits for these limits speak that the fault of type change of delay of a signal takes place. Simulation of such devices can be fulfilled in system of simulation on the basis of *K*-value representation of signals and the computers base units operation's description on the basis of the *K*-value differential equations.

The offered system of simulation allows represent if necessary explorers of digital devices as the long lines

connecting transmitters and signals receivers, by means of *K*-value differential or functional models [9]. The system of simulation allows research also computers operation in view of power of switching processes that enables to determine a static noise stability of projected devices. At the same time, the offered system of simulation allows to model and all processes in the digital devices, enumerated earlier, and received at usage known thirteen-value alphabets. As an example we shall consider simulation of the device resulted operation on fig. 2.

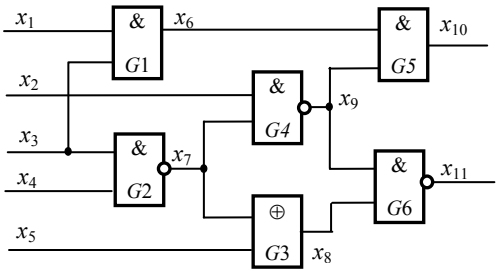

Fig. 2. The device with presence of failure risks

The main component of such device is two-input a logical unit "And" which table of states in the 13-value alphabet looks like:

&	0	1	*X*	*E*	*H*	*P*	*V*	*F*	*L*	*O*	*I*	*A*	*B*
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	*X*	*E*	*H*	*P*	*V*	*F*	*L*	*O*	*I*	*A*	*B*
X	0	*X*	*X*	*A*	*O*	*P*	*X*	*A*	*O*	*O*	*X*	*A*	*X*
E	0	*E*	*A*	*E*	*P*	*P*	*F*	*F*	*P*	***P***	*F*	*A*	*A*
H	0	*H*	*O*	*P*	*H*	*P*	*P*	*P*	*L*	*O*	*O*	*P*	*L*
P	0	*P*	*P*	*P*	*P*	*P*	*P*	*P*	*P*	*P*	*P*	*P*	*P*
V	0	*V*	*X*	***F***	*P*	*P*	*V*	*F*	*L*	*O*	*I*	*A*	*B*
F	0	*F*	*A*	*F*	*P*	*P*	*F*	*F*	*P*	*P*	*F*	*A*	*A*
L	0	*L*	*O*	*P*	*L*	*P*	*L*	*P*	*L*	*O*	*O*	*P*	*L*
O	0	*O*	*O*	*P*	*O*	*P*	*O*	*P*	*O*	*O*	*O*	*P*	*O*
I	0	*I*	*X*	*F*	*O*	*P*	*I*	*F*	*O*	*O*	*I*	*A*	*X*
A	0	*A*	*A*	*A*	*P*	*P*	*A*	*A*	*P*	*P*	*A*	*A*	*A*
B	0	*B*	*X*	*A*	*L*	*P*	*B*	*A*	*L*	*O*	*X*	*A*	*B*

For the beginning it is possible to consider situation, when on inputs of a logical unit "And" there are signals *E* (smooth transition from "0" in "1") and *O* (transition from uncertainty in "0"). It corresponds to output signal *P* which is on an intersection of the fifth line and the eleventh column of the table. Such output signal is static risk of failure in "0" (*P*). On fig. 3 results of logical unit simulation are resulted "And" at the specified entry signals (signals *A* and *B* accordingly) in system on the basis of *K*-value differential calculus at $K = 7$.

In this case in system of simulation logical "0" coincides with zero, and logical "1" corresponds to value "6" - accordingly the minimum and maximum values at seven-element representation of signals.

On an output of a unit signal *C* which really corresponds to static risk of failure in "0" is observed, thus its amplitude is equal "3" (half from maximum value at seven-element representation of logical signals).

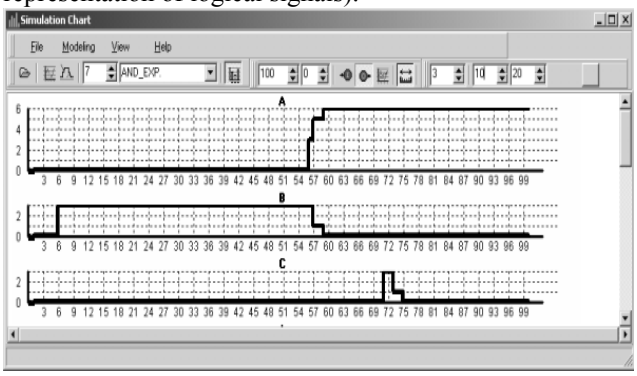

Fig. 3. Static risk of failure in "0"

According to tab. the dynamic risk of failure from "0" in "1" (*F*) on an output of a logical unit "And" takes place, when on its inputs there are signals *V* (static risk of failure in "1") and *E* (smooth transition from "0" in "1"). It corresponds to an intersection of the eighth line and the fifth column of the table. On fig. 4 are resulted results of simulation of this case where signals *A* and *B* correspond to specified entry signals *V* and *E*, and signal *C* shows presence of dynamic risk of failure at transition from "0" in "1".

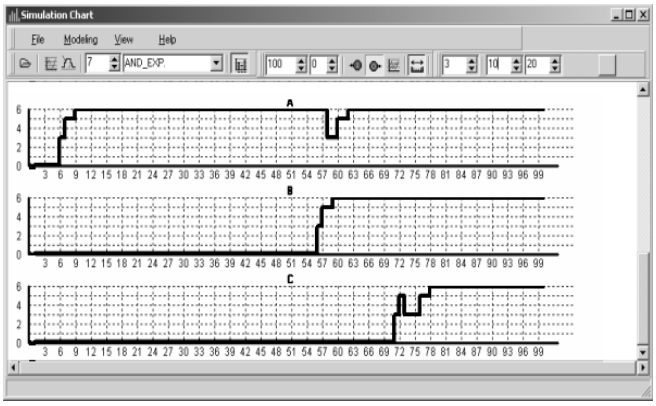

Fig. 4. Dynamic risk of failure from "0" in "1"

For an example it is possible to consider operation of more complex device (fig. 3) at which there are faults of type "delay of signal's distribution". Sort of this device in system of computer-aided design on the basis of *K*-value differential calculus is presented on fig. 5.

On inputs x_1 and x_3 this device difference of a logical signal from "1" in "0", on inputs x_2 and x_4 – a level of a constant "1", and on an input x_5 – a logic zero level moves. Thus on an output x_{11} "failure" of an output logical signal concerning a level logical "1" is observed. It corresponds to a situation of static risk of failure in "1" (fig. 6). Thus any unit of the circuit can to be in any of thirteen states.

The system of *K*-value simulation allows parsing also devices with usage power the analysis of switching signals.

On fig. 7 time diagrams of operation of the device (fig. 3) in view of power of switching of entry signals are resulted.

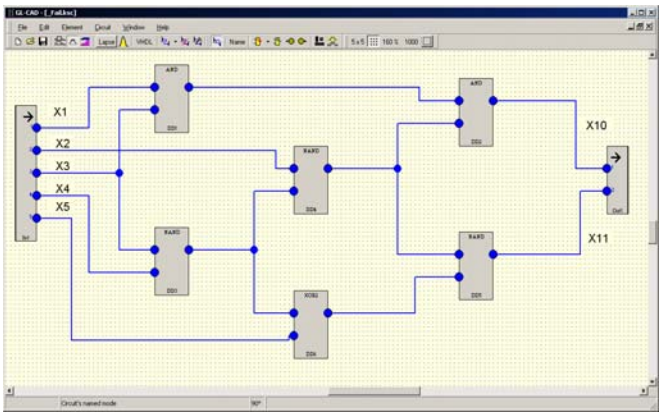

Fig. 5. Structure of the device in system of *K*-Value modeling

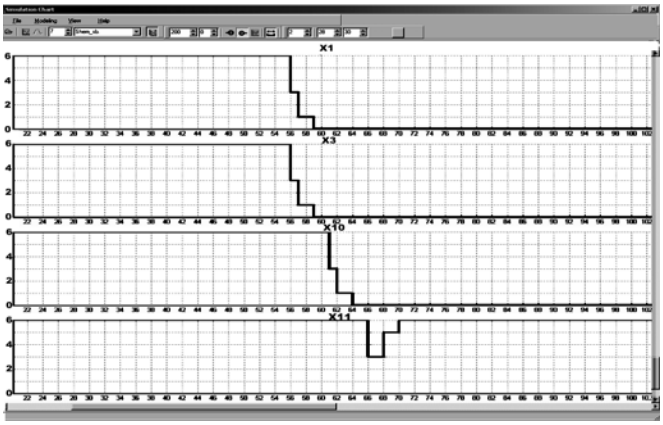

Fig. 6. Static risk of failure

On fig. 8 time diagrams of this device operation in a base mode (without the analysis of logical signals switching power) in that case when on two its inputs x_1 and x_3 signals which are encoded as *O* (see the table), and on inputs x_2, x_4 act are resulted and x_5 are submitted logical "1", "1" and "0" accordingly.

Apparently from a figure on outputs x_{10} and x_{11} during a working time slice (about 15 nanoseconds on 66 nanoseconds) keeps a level of logical uncertainty (K = 3), that is defined by logic of separate logical units operation according to truth tables [6]. Similar results turn out at usage of other methods and systems of many-valued simulation.

At activation in system of *K*-Value modelling process in the account of power switching on entrance signals, there is an opportunity of its account at modelling device, in particular, on outputs x_6 and x_7 on a working interval time signals reach steady logic levels (fig. 6), unlike a level of uncertainty which could be observed in the previous case (fig. 5).

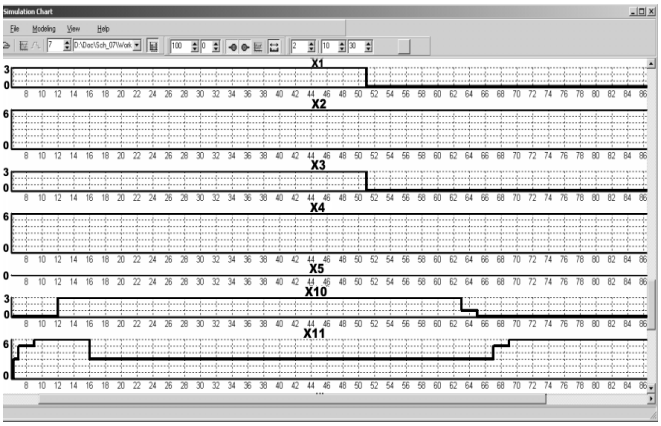

Fig. 7. Time diagrams of the device functioning in base mode

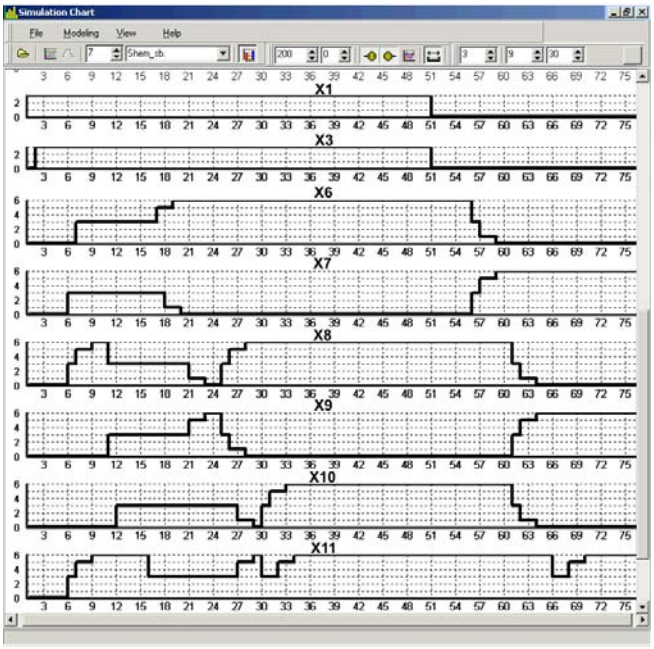

Fig. 8. Time diagrams of functioning the device in view of power switching on entrance signals

Similarly, the account of power switching of entrance logic signals leads to a deviation from level K = 3 values on all other intermediate circuits of the designed device. All this causes that on an output x_{10} in an interval of time 27 – 30 nanoseconds are observed error condition in the form of "failure" of a target voltage from a level of uncertainty up to a level of logic zero, and on an output x_{11} – "failure" of a logic signal on an output from a level of logic "unit" up to a level of uncertainty.

The received results speak about an opportunity in designing devices and research their working capacity by means of system on the basis of *K*-Value differential calculus to receive more exact quantitative and qualitative analysis error situations in designed devices.

IV. CONCLUSION

Use of system of modelling on the basis of *K*-Value differential calculus allows to receive fuller qualitative and quantitative characteristics of failures in comparison with other existing systems of multiple-valued modelling in which there is no opportunity to represent quantized on amplitude a logic signal in the *K*-Value alphabet. Besides its use enables to consider research of such failures a real steepness of signals fronts on synchronization and data. All this opens prospect of use of system of *K*-Value modelling at designing complex and difficult computers.

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