Statistical Properties of Spread Spectrum Signals Synchronization System

Inna O. Tkalich, Helen V. Kharchenko and Yegor I. Vdovychenko

Abstract—**In this paper the method of digital spread spectrum signals (DSSS) processing concluding digital matched filtration, synchronization and decision making about transmitted signals, FPGA-usage orientated from different vendors is presented. Special attention is attended to the research of synchronization algorithms in the non-Gaussian and nonstationary noise influence conditions. The system synchronization probability-timing characteristics are obtained.**

Index Terms— **Density of distribution, digital recirculator, DSSS, FPGA, synchronization system**

I. Introduction

During receiving signals with long base, one of the main problems is providing high quality characteristics for the synchronization system [1]. It is known that decreasing locking in synchronism time is possible using spread spectrum signals and two-step procedure of synchronization [1]. At once, in the first stage clocking synchronization is provided which consists in determination signal elements convolution monitoring meaning moments, which are the signals either with base [2]

$$B_{EL} = \tau_{EL} \cdot \Delta F_{EL,}$$

where τ_{EL} – element duration, sec; ΔF_{EL} – effective element spectrum bandwidth.

In the second stage the spread spectrum signal matched filtration is performed using signal samples which had been taken in the points of time corresponding signal elements meaning moments. Then, the spread spectrum signal beginning (ending) corresponding meaning moments are determined – i.e. frame synchronization is performed.

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II. DSSS synchronization

In the actual communication systems the synchronization subsystem is functioning in the conditions of a prior uncertainty, relatively to the receiving signal parameters, non-Gaussian and nonstationary noise influences, and that's essentially limits the possibility of providing. In the connection with this, it is necessary to use synchronization algorithms efficiency of those would not be dependent on receiving signal intensity and also faintly dependent on kind of noise distribution density parameters for the complex influence, i.e. – on rabastic algorithm.

Clocking synchronization procedure concludes, firstly, in the strong correlation zone determination of spread spectrum signal receiving element and, secondly, in the timing position estimation for the maximum element of convolution, where the maximum signal-to-noise ratio level is detected. For the strong correlation zone determination the following algorithm is offered. The signal clocking interval is divided by L subintervals, each one of them has its own number (address) (see fig.1): a – conditional beginning of signal interval, b – conditional beginning of the next signal interval.
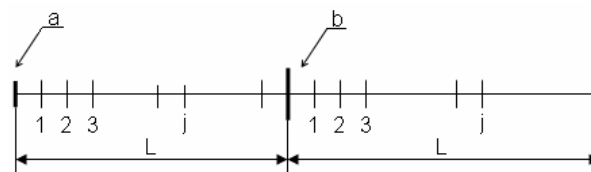

Fig. 1. The conditional partition of signal interval

It is determined and remembered the address of jth subinterval where the observed process maximum value is situated. If to suppose that the signal convolution element is detected in the jth subinterval, then with probabilities q exactly in this subinterval will be found the observed process maximum value. For the given trustworthiness providing of a sound decision about subinterval address, where the element convolution is presented, the procedure is repeated as long as the address of jth subinterval (or any others subinterval) is repeated m times. Once, the probability of the false synchronization is equal to

$$P_{fs} = \left(\frac{1}{L}\right)^m, \tag{1}$$

the composite probability of strong correlation interval determination for k intervals is defined by the expression [1]:

$$P_\Sigma(k) = \begin{cases} 0 & k < m; \\ q^m + (k-m)Q & m \le k \le 2m; \\ q^m + (k-m)Q - Q\sum_{j=1}^{k-2m} P_\Sigma(m-1+j) & k > 2m, \end{cases} \quad (2)$$

where $Q = q^m(1-q)$;

q – is a probability of a sound decision about meaning moment position in the jth interval.

Obviously, the signal energy to power noise spectral density ratio, in the moment of signal element convolution maximum is not high, as far as for the signal receiving in general it is supposed following matched filtration and for the fast and reliable j^{th} subinterval detection is necessary to take steps providing rising element energy ratio to power noise spectral density N_0

$$\eta_{EL} = \frac{E_{EL}}{N_0}.$$

At the same time it is necessary to create conditions for the frame synchronization. For this purpose, it is proposed to use the device with structural schema presented in figure 2, where: MF"1" – the filter matched with signal element corresponding transmitted logical "1"; MF"0" – the filter matched with signal element corresponding transmitted logical "0"; SLD – square-law detector of envelope.
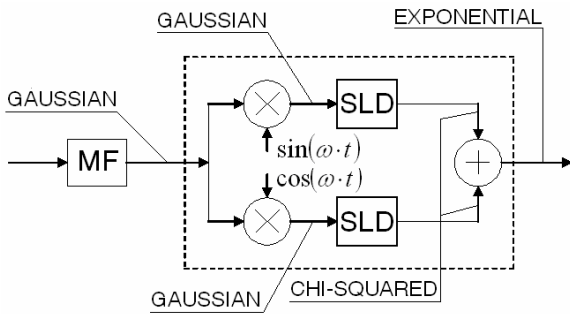

Fig. 2. Square-law detector of a signal envelope

In the absence of a signal in the output of the matched filter (see fig. 2) [6] instant values of observable process are distributed by the normal law [5] with a variance $\sigma^2 = N_0 \cdot E_{EL}$

$$W(x) = \frac{1}{\sqrt{2\pi}\sigma} \ e^{-\frac{x^2}{2\sigma^2}} \quad (3)$$

In the output of the square-law detector the density of distribution of a signal envelope in the reference moments of time t_i is distributed by the exponential law,

$$W(U = x^2) = \frac{1}{2\sigma^2} \ e^{-\frac{U}{2\sigma^2}}, \quad (4)$$

and the difference of exponentially distributed random values (see fig. 3) is distributed according to Laplace's law (double exponential distribution)

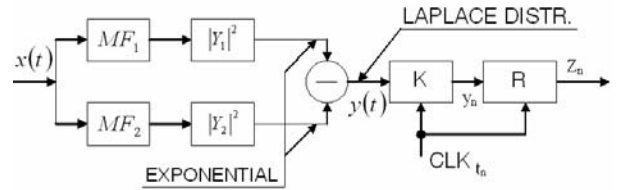$$W(y = U_2 - U_2) = \frac{1}{4\sigma^2} \ e^{-\frac{|y|}{2\sigma^2}}, \quad (5)$$

Fig. 3. Differential channel of synchronization

the cumulative function, in the absence of a signal, equals [4]

$$\Psi(t) = -\ln \ (1 + \beta^2 \cdot t^2), \quad (6)$$

where $\beta = 2\sigma_2$.

Cumulants of the i-order, calculated according to expression (6) may be defined as [4]

$$\chi_k = \begin{cases} \chi_1 = 0; \\ \chi_2 = 2\beta^2; \\ \chi_{2n-1} = 0; \\ \chi_{2n} = \frac{(2n)!}{n}\beta^{2n}, \end{cases} \quad (7)$$

where $n = 1, 2, \dots$.

Cumulants possess two important properties, which allowing executing calculation of cumulants any order for the sum of independent random variables with any weighting factors [9]:

1) The cumulant of a k-order for the multiplication of a random variable y by a constant a is equal to

$$\chi_k(ay) = a^k \chi_k(y) \quad (8)$$

2) The cumulant of an independent random variables sum is defined by expression

$$\chi_k(\sum_{n=1}^{N} y_n) = \sum_{n=1}^{N} \chi_k(y_n) \quad (9)$$

If random variables y_i are identically distributed

$$\chi_k(\sum_{n=1}^{N} y_n) = N\chi_k(y_i) \quad (10)$$

In consideration of specified above, it is simple to obtain cumulants of any order in the output of memory device with exponential weight function (recirculation system)

$$Z_{III} = \sum_{l=0}^{\infty} d^l y_l, \quad (11)$$

and according to expressions (7) - (9) and (11) the cumulants will be equal

$$\chi_{2n} = \sum_{l=0}^{\infty} d^l \frac{(2n)!}{n}\beta^{2n} = \frac{(2n)!}{n} \cdot \beta^{2n} \cdot \sum_{l=0}^{\infty} d^l \quad (12)$$

when $d < 1$

$$\sum_{l=0}^{\infty} d^l = 1 + d + d^2 + \dots = \frac{1}{1-d}$$

and

$$\chi_{2n} = \frac{1}{1-d} \cdot \frac{(2n)!}{n} \cdot \beta^{2n}, \quad (13)$$

where $n = 1, 2, \dots$.

Under central limit theorem, the distribution of a sum of independent random variables converges to the normal law of distribution. The degree of convergence can be appreciated by coefficient of skewness

$$k = \frac{\chi_3}{(\chi_2)^{3/2}} \qquad (14)$$

and by kurtosis

$$\gamma = \frac{\chi_4}{(\chi_2)^2} \qquad (15)$$

For random variable Z, under (7), (14) and (15) follows

$$\begin{cases} k_Z = 0; \\ \gamma_Z = 3 \ (1-d). \end{cases} \qquad (16)$$

From expression (16) follows, that at $0.97 \leq d < 1$ coefficient of kurtosis $\gamma_Z < 0.1$, and coefficient of skewness k_Z. It allows to use as an approximation of distribution for random variables in the output of recirculation system the law with normal distribution and parameters $m_Z = 0$,

$$D_Z = \frac{2\beta^2}{1-d} = \frac{8}{1-d}\sigma^4 .$$

In the presence of a signal in one of the receiving channels, it is possible to show [5],[2], that in the output of the signal envelope square-law detector $m_y = E_c^2$, and the variance is equal

$$D_y = 4\sigma^4 + \frac{E^2}{\sigma^2}, \qquad (17)$$

where

$$\sigma^2 = \frac{E_s N_0}{2} . \qquad (18)$$

In the output of the subtracting device (in the input of recirculation system)

$$m_Z = E^2$$

$$D_Z = 4\sigma^4(2 + \frac{E^2}{\sigma^2}) \qquad (19)$$

or under (18)

$$D_Z = 4\sigma^4(2 + q^2) , \qquad (20)$$

where

$$q^2 = \left(\frac{2E_{EL}}{N_0}\right)^2 . \qquad (21)$$

And in the output of recirculation system, respectively,

$$m_Z = \frac{E^2}{1-d} , \qquad (22)$$

$$D_Z = \frac{4\sigma^4}{1-d} \ (2 + q^2) , \qquad (23)$$

or

$$D_Z = \frac{E^2 N_0^2}{1-d} \ (2 + q^2) . \qquad (24)$$

Setting normalization $Z_L = \dfrac{Z}{\sqrt{P}}$, we will receive the density of probability distribution of a random variable in the output of recirculation system as

$$W(Z_L) = \frac{1}{\sqrt{2\pi}} \ e^{-\frac{(Z_L - q_L)^2}{2}} , \qquad (25)$$

where

$$q_L = \sqrt{\frac{q^2}{1-d} \cdot \frac{q^2}{4(2+q^2)}} \qquad (26)$$

The second factor under a radical of expression (26) characterizes losses during non-coherent accumulation subject to signal-to-noise ratio in the input of the square-law detector of envelope.

Dividing a clock interval by L subintervals of integration, and taking into account, that quantity of the independent samples providing sufficient accuracy of a target process representation is approximately equal

$$N \cong B_{EL} = \tau_{EL} \cdot \Delta F_{EL} , \qquad (27)$$

we obtain, that the quantity of independent samples of the noise, getting in the interval of integration, is equal

$$N_{int} = \frac{B_{EL}}{L} , \qquad (28)$$

During an integration of the input process within limits of an interval, it is easy to show, that

$$D_Z = 4\sigma^4 \ (2\frac{B_{EL}}{L} + q^2) . \qquad (29)$$

Respectively the signal-to-noise ratio in the output of recirculation system may be defined

$$q_L^2 = \frac{q^2}{1-d} \cdot \frac{q^2}{4 \ (2\frac{B_{EL}}{L} + q^2)} . \qquad (30)$$

The probability of an error during decision-making about actually convolution maximum detection in the subintervals is defined by the formula [3], [5]

$$P_{rec} = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} e^{-\frac{(Z-q_L)^2}{2}} \ [F(Z)]^{L-1} \ dZ , \qquad (31)$$

where

$$F(x) = \int_{-\infty}^{x} e^{-\frac{y^2}{2}} \ dy \text{ - probability integral.} \qquad (32)$$

III. FPGA-BASED SYNCHRONIZATION SYSTEM

Synchronization system realizing worded above method is made in terms of FPGA, using hardware description language VHDL. The VHDL-model is implemented in the crystals of microchips from different vendors such as ALTERA [7], XILINX [8] and others. Fig. 4 presents a schema of the synchronizing system in the registry transfer level implemented in FPGA ALTERA CYCLONE II EP2C70F672C6 using CAD QUARTUS [7].

The system consists of: DD1, DD2 – signal energy storage systems (SESS); DD3 – phase-locked loop system (PLL); DD4 – differential synchronization channel (DSC); DD5 – the block of m-multiple maximum value same address repeatance searching, and synchronization reset when there is no confirmation according to criterion k of n (SYNCH) [13]; DD6 – exact frequency tuning system (EFTS); DD7 – decision support system (DSS).
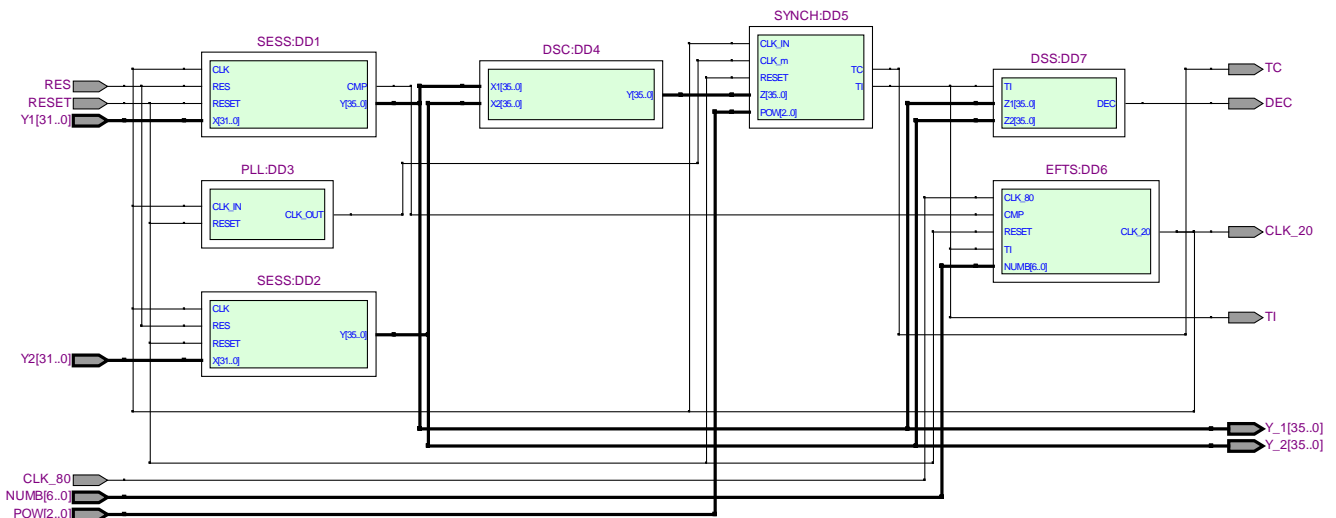
Fig. 4. Synchronization system schema in the RTL level

In the input of synchronizing system during functioning in the consistence of the DSSS processing model device the signals from PDMF channels outputs [6] are followed and in the signal energy stored systems m (m=16) samples located in each subinterval are summarized. On purpose to output the signal for exact frequency tuning the clocking interval is divided by two subintervals in accordance with m/2 (m/2=8) samples correspondingly. Signal predominance in the one of subintervals part selects a direction of frequency tuning.

From the output of differential synchronization channel DD5 the absolute value of accumulated values is followed in the input of digital recirculator based in the module DD5 on CLK_OUT signal falling edge of DD3 module. When projecting using VHDL the digital recirculator may be presented in several ways [11]: as distinct, parameterized data type (array) - MEMORY is array (0 to 127) of signed (5*N+1 down to 0); either using random access memory library component lpm_ram_dp. In the VHDL-model synthesis result of the synchronization system, in the second case required significantly less logic elements quantity (<1%) comparatively with the first case (≈40%) when the digit capacitances are the equivalents.

The recirculator writing address is formed inside of block DD5. The address corresponded to maximum value detection in the clocking interval is remembered and when m-multiple maximum repentance is detected the signal "Synchronization detected" is formed in the output of this block. This signal enables exact frequency tuning system and allows passing clocking impulses in the decision support system DD7.

If the m-multiple address repentance is detected (signal "Synchronization detected" is formed), address monitoring is not stopping. This is necessary for the false synchronization or system failure excluding aroused during functioning. If the signal in the input of the receiver is absent the m-multiple address repentance corresponds to arising of false synchronization which should be canceled. This state detected if among n selections the monitoring address has been repeated less then k times. The probability of false synchronization arising is defined by the formula

$$P_{fs} = 1 - \left(1 - P_j\right)^L = 1 - \left(1 - \sum_{i=k}^{n} C_n^i P^i \left(1-P\right)^{n-i}\right)^L, \quad (33)$$

where $P = \dfrac{1}{L}$ – probability of jth address detection, P_j – probability when j^{th} subinterval address will be repeating k times or more. At once synchronization system transferring in the initial state is performed. The probability of false synchronization occurrence is presented in the table 1.

TABLE 1
THE PROBABILITY OF FALSE SYNCHRONIZATION OCCURRENCE WHEN USEFUL SIGNAL IS ABSENT AND THE VALUES n=32 AND L=128

	k=2	k=4	k=8	k=16
P_{fs}	$9.65\cdot10^{-1}$	$1.43\cdot10^{-2}$	$1.58\cdot10^{-8}$	0

During useful signal presence in the input of the receiver and the k-multiple address repentance absence among n observations the false synchronization reset will be performed of the correctly detected subinterval. The probability of such an event is defined by expression

$$P_{fr} = 1 - \sum_{i=k}^{n} C_n^i P^i \left(1-P\right)^{n-i}, \quad (34)$$

where P is defined by formula (31).

TABLE 2
THE PROBABILITY OF FALSE SYNCHRONIZATION RESET IN THE ABSENCE OF USEFUL SIGNAL AND THE VALUES n=32 AND L=128

h^2	P_{fr}	k=2	k=4	k=8
2	0.4	$6.86\cdot10^{-7}$	$6.1\cdot10^{-5}$	$1.48\cdot10^{-2}$
2.5	0.6	$1.99\cdot10^{-12}$	$8.52\cdot10^{-10}$	$4.54\cdot10^{-6}$
3	0.7	0	0	$1.09\cdot10^{-11}$
3.5	0.8	0	0	0

TABLE 3
THE PROBABILITY OF FALSE SYNCHRONIZATION RESET IN THE ABSENCE OF USEFUL SIGNAL AND THE VALUES n=16 AND L=128

h^2	P_{fr}	k=2	k=4	k=8
2	0.41	$2.12\cdot10^{-3}$	$4.8\cdot10^{-2}$	$6.6\cdot10^{-1}$
3	0.78	$1.07\cdot10^{-9}$	$5.36\cdot10^{-7}$	$2.35\cdot10^{-3}$
3.5	0.89	$1.84\cdot10^{-14}$	$5.09\cdot10^{-11}$	$6.74\cdot10^{-6}$
4	0.95	0	0	$3.19\cdot10^{-9}$

The exact frequency tuning system is meant for the correlation function maximum position regulation in the accumulated samples subinterval middle. For this purpose period addition and subtraction from clocking frequency is performed correspondingly with indication of the frequency tuning direction. Exact frequency tuning system is included in the module DD6 in one clocking frequency f_{out} (f_{out}=20 MHz) is formed by dividing the input frequency f_{in} (f_{in}=80 MHz) by 4. Relative frequency of exact frequency tuning is set according to signal-to-noise ratio level and also according to degree of basic generators instability in the transmitting and receiving side pieces and is controlled using reversible counter.

When reversible counter is zerozied period subtraction is performed as it is shown in the figure 5. When the counter overflowed the period addition is performed as in the figure 6 is shown.
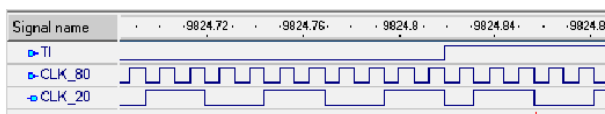

Fig. 5. Period subtraction

Fig. 6. Period addition

Fig. 4 presents phase-locked loop system DD3 meant for frequency synthesizing of a clock signal that is based on a reference clock by the way of dividing input frequency by division factor m. Frequency division by integral factor implementation is quite simple. Fractional division factor can be obtained in several ways [10], simplest is to sequence division factors n and n+1 periodically based on the specified program. Synthesized oscillation spectral purity depends on how rationally the sequence order of the division factors is chosen. Frequency synthesis is presented in [12].

From the output of DD3 signal is clocking module DD5. The decision support system compares samples values which leave accumulations (DD1, DD2) at the falling edge of module DD5 clock pulse moment and gives out the decision about accepted signal.

IV. CONCLUSION

In this paper the method of spread spectrum signals digital processing which concludes digital matched filtration, synchronization and decision making about transmitted signals, orientated on using FPGA different vendor firms. Digital matched filtration is sufficiently explored and the methods of its realization using FPGA are known [6]. At the same time the large base signals for the systems that act in the non-Gausse and nonstationary noise synchronization methods are insufficiently investigated, and their probability-temporary characteristics practically are not researched. The offered in the paper algorithms of synchronization well implemented to the FPGA crystals. Given above some synchronization system descriptions allow speaking about system parameters optimi-

zation opportunities and expediency of its use in telecommunication systems with the code signals division.

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