Variants of Topology Editing Strategy in the Subsystem of Printed Circuit Boards Manufacturability Improvement

Roman Panchak, Konstantyn Kolesnyk, Marian Lobur

Abstract — **This paper focuses on the variants of printed circuit boards topology editing strategies implemented in the subsystem of automatic printed circuit boards topology editing. Depending on the requirements for printed circuit board topology, a subsystem user can create variants of editing strategies in order to minimize the amount of the technologically justified places with a minimum clearance between the elements of the topology.**

Index Terms — **printed circuit board topology, printed circuit board manufacturability.**

I. Introduction

The characteristic of topology of modern printed circuits board (PCB) is usages of diverse electronic components with conclusions fulfilled in miscellaneous systems of measurement (metric and inch) and usage at implementation of technological places of these units of a fair quantity miscellaneous under the shape and sizes of types of bonding contact pads. The modern technologies of making of PCB allow successfully to realize explorers in relation to a small width (0,075-0,15)mm. The programs of automatic trace [1-3] routine creations of the strategies of tracing, in which one the diverse criteria will be used. Traditional criteria for modern tracers is forming of dropwise form of blivets from the side of connecting to them of explorers, narrowing of wide explorers at connected to the blivets, straightening of explorers with the purpose of minimization of number of bends of explorers, round explorers in the. An attempt with the purpose of compression of topology to set minimum possible width of explorers for this class of PCB, generates after realization of topology the necessity of its editing with the purpose of diminishing of amount technologically unjustified bottlenecks. This procedure in modern systems of projection of topology [1]-[3] partly decides by the hand editing or by the use of certain iteration procedures in the interactive mode. For improvement of manufacturability of a figure on the factories, which one are engaged in serial manufacture PCB, on the stages of technological preparation of production will use some specialized systems [4],[5] Nevertheless it is necessary to recognize, that the editing of topology without participation of its developer sometimes loss results of capacity of PCB. Especially often it happens for PCB, on which one the topology will be realized, in which one the analog-digital signals on relation high measure frequencies (50-100) MHz and above are treated, and also it is necessary strictly to maintain topology with low levels of high frequency analog signals, for handling which one of coordinate of a feature placement and charting of explorers in strict correspondence with recommendations of firms of manufacturers electronic component.

It should be noted that for today the known system which decided an analogical task for the topologies of PCBS with substantial limits on types and amount of width of explorers, and also shape and sizes of bonding contact pads. For the indicated system essential limitation was step of a grid chart of topology PSB, besides the system operated under DOS, which became not actual today [6].

The subsystem of the automatic editing of topology of PCB, which one will be used after completion of development of topology and will be used for minimization of an amount of the technologically justified „narrow" places. An amount of widths of explorers, and also types and shapes of bonding contact pads, which one are treated by a system, is practically unreserved. The step of planning of a grid arbitrary. The subsystem will be used in a CAD system „Electron" has a library of translators for the transmission of topology from a few systems of planning.

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As the stage of printed circuit board (PCB) topology design in the current systems has been completed, the pre-production stage is on its way. At this stage within design systems the control programs, which form PCB layers reflectance and drill the holes, are produced.

In order to improve manufacturability of the PCB picture in the Electron computer-aided design system, the subsystem of PCB topology technological editing has been implemented [7]-[9].

After the topology has been included into the editing subsystem, automatic increase of the sizes of contact pads and widths of the conductors to the values that are technologically justified for a given PCB accuracy class can be seen in the first stage of the system operation under the relevant settings in the system database

The second stage deals with searching for a "bottleneck" (a place where the clearance between elements of the topology is not proper for the given PCB accuracy class), if such a "bottleneck" has appeared at all after the first stage.
In the third stage the elements of topology are edited, in order to eliminate the bottleneck.

In the fourth stage the PCB layers topology is formed in the format, required by users.

The experience of using PCB topology editing subsystem revealed the necessity for the development of various editing strategies for the elements of topology, depending on the requirements for the topology and taking into account the PCB accuracy class.

This paper considers the variants of PCB topology editing strategies implemented in the subsystem of technological processing.

II. THE REALIZED PROCEDURES OF AUTOMATIC EDITING OF TOPOLOGY

After translation of the got topology forming of its internal form, the database of project is created and built mathematical model the structure of which is presented in [7]. At construction of model the increase of width of an explorer and increase of diameter of a bonding contact pad (CP) is carried out to the size which is set in a database for this class of PCB.

During scanning model appear „narrow" in topology and the optimization procedures on handling topology in a following sequence are executed:

1) The procedure of a rectification of explorers will be realized at enlarged width of explorers and diameters CP.

2) The procedure of rounding of the found obstacle an explorer is carried out, without the change of width of explorer, if such possibility exists. The adjacent explorers in local area of editing can test also changes. If available space allows on PCB, they shift on magnitude of an admissible clearance without change of width, if available space in the area of editing not, the explorers are narrowed to magnitude of a value of minimum width in a local place in topology.

3) If rounding of explorer is impossible, is executed cutting of explorer in local area of bottleneck to the width, which one is admissible for PCB of the given class. The cutting of explorer can be carried out discretely on the size of cutting, which one is set by the user.

4) In a case not of observance of a clearance between an explorer and bonding contact pad even at execution cutting of explorer, the cutting bonding contact pad (CP). The cutting of CP can be carried out discretely on a size which is set by a user, or at once on a maximally possible size but to the size of warranty belt of CP for this class of PCB.

5) The cutting of the form and sizes of PCB can take place as at the decision of conflict type „ CP - explorer" so at a conflict „CP-CP".

Such strategy of the technological editing of topology of PCB allows sharply to decrease a narrow seating capacity, provides optimization of topology after the criterion of maximal reliability of node in exploitation and minimization of shortage in a mass production.

III. PCB TOPOLOGY EDITING STRATEGIES

According to the national standard, there are five accuracy classes of structural elements (conductors, contact pads, holes, etc.) and limit deviations, as well as minimum nominal sizes for the bottleneck of the structural elements. Taking into account different accuracy classes of PCBs, the following variants of editing strategies can be used.

Third class PCBs

In PCB topologies of this class relatively wide conductors (0,6 ÷ 0,3 mm) and contact pads with diameters 1,2 ÷ 1,5 mm are used; relatively unsaturated topologies are implemented. To perform technological transformations for such PCBs in the editing subsystem one should use a strategy, which contains procedures of deep rounding of conductors, rounding of conductors involving narrowing and contact pads cutting procedure.

Unsaturated PCBs of the fourth and fifth classes

In the topologies of such PCBs the conductors with a small width (0,2 ÷ 0,25 mm) are used; the diameter of contact pads is 0,8 ÷ 1,0 mm; components with a small lead pitch, chips in packages with planar leads, circles with the frequency of signals up to 0.5 GHz are used.

The topology of such PCBs is moderately saturated and the width of conductors can be increased. If the structural constraints are absent, it is allowed, when editing, to round the contact pads with the conductors without narrowing the conductors to the technologically justified PCBs for the given accuracy class. If it is impossible to round the contact pad with the conductor without narrowing the conductors, the conductor has to be narrowed, and if it is not enough to ensure that the clearance is proper, the contact pad has to be cut.

To perform technological transformations for such printed circuit boards, a strategy, which contains functions of conductors rounding, conductors and contact pads cutting, has to be used.

Saturated digital and digital analog PCBs of the fourth and fifth accuracy classes

A characteristic feature of the PCBs of this class is high saturation of topology with conductors with small width (0,1 ÷ 0,15 mm). Contact pads diameter is 0,5 ÷ 0,8 mm. Components with a small lead pitch, chips in packages with solder balls, circles with the frequency of signals more than 1 GHz are used.

Editing strategy of such PCBs is largely determined by frequency characteristics of signals that pass through the conductors. In recent years the usage of differential pairs (identical information transmission through two adjacent conductors on the PCB with the phase difference of 180 degrees) for digital high-frequency equipment design in the PCB topology has considerably increased. Installation of conductors which transmit such signals to PCB imposes certain structural constraints on the topology elements of both the conductors, which transmit signals of differential pairs, and adjacent elements of the topology. Such circles are marked in the subsystem as fixed, which automatically means no possibility of editing at all.

Every day the leading firms-developers impose more and more strict requirements to the topology of the conductors that implement specific circles and parameters of the conductors (width, length) for the chips. When the possibility and parameters of such conductors are changed, the characteristics of signals are changed too, and sometimes PCB may become unworkable.

Taking into account frequency and structural constraints on the topology of conductors for such PCBs in the topology editing subsystem the strategy of cutting the contact pads is used.

In the editing subsystem user can also optionally create mixed topology editing strategies depending on the technological needs of the PCBs manufacturer.

The fact that there are a few variants of strategies of technological editing of PCB topologies allows to drastically reduce the number of bottlenecks, provides topology optimization by the criterion of maximum reliability of the node in operation and minimize rejects in serial production.

IV. Results

The developed subsystem of technological editing of PCB topology is being used as a part of the Electron CADS at the Electron OJSC in Lviv. Figure 1 shows the photo of the fragment of PCB topology before and after technological editing with different variants of the technological editing strategy.

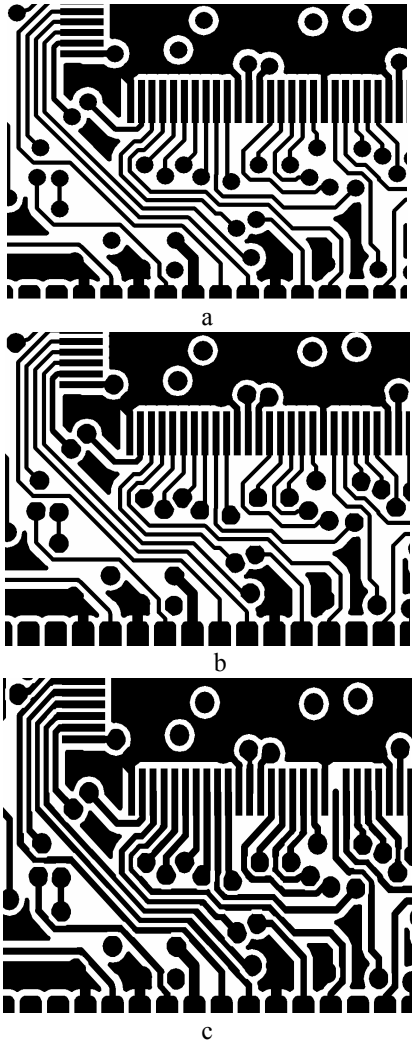

Fig. 1. The photos of the fragment of PCB topology:
a – topology before editing; b – contact pads cutting;
c – conductors and contact pads cutting

On Fig.2 the resulted picture of fragment of topology of DP is after treatment of the technological editing a subsystem. The system is exploited on a computer with the following configuration:

– Processor of AMD AthlonX2 5600+ (clock rate of a core 2,81GHz);
– RAM Patriot of 2x1Gb 6400 (800MHz);
– Hard disk of Samsung 320 Gb SATA2 16Mb of Cash;
– System board of Asus M2N-E nForce 570 Ultra;
– Descriptions of topology of PCB:
– A file size of description of topology is 72347 byte
– Amount of graphics primitives of topology – 12476

Expenses of processor time:

– Translation of file of topology in an internal form – 370 ms;
– Construction of mathematical model – 2485 ms;
– Editing of topology– 12796 ms;
– Saving of file – 267 ms;

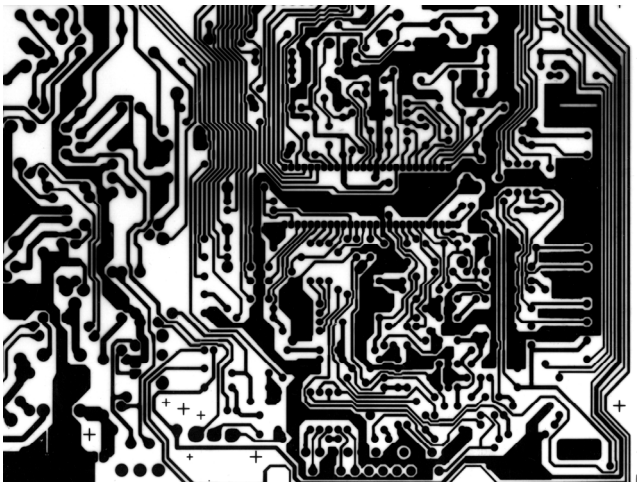

Fig.2. Picture to the fragment of topology of a PCB after handling by the subsystem of the technological editing of topology

IV. Conclusion

The subsystem of technological editing of PCB topology allows effective editing of topology elements using different strategies providing high manufacturability.

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